Who should attend ?

... those graduate students planning to learn low-voltage IC design considerations and techniques, so as to improve their **already acquired** knowledge and/or experience in *bipolar and MOS analog integrated circuit design.*

Who should NOT attend ?

... those who DON'T have a sufficient background about analog integrated circuit design.

The student is expected to be **closely familiar** with each of the topics listed below.

- BJT and MOS device physics
- BJT and MOS I/V characteristics
- Second-order effects and parasitics
- Device models
- Basic microelectronic amplifier stages
- Small-signal and large-signal analysis/behavior of amplifiers
- Current mirrors
- DC and high-frequency response of amplifiers
- Operational amplifiers
- Feedback, stability and compensation
- Sampled-data and continuous-time filters
- BJT/CMOS/BiCMOS processing Technologies
- Layout considerations and techniques

Outline (*subject to modification*)

- Why *analog* ?
- Why *integrated* analog circuits ?
- Why *low-voltage* analog ICs ?
- Low voltage limitations for MOSFETs and BJTs
- Solutions to obtain rail-to-rail amplification
  - Stability issues
  - Constant-g_m rail-to-rail input stages
  - Rail-to-rail output stages
- Compensation of low-voltage multistage opamps
- Other low-voltage analog building blocks and techniques
  - Low-voltage current mirrors
  - Low-voltage transconductors
  - Low-voltage analog multipliers
- Current-mode techniques for low-voltage operation
- Other low voltage design techniques
  (e.g. differential approach, log-domain filters, etc.)

REFERENCES

- **Edgar Sanchez-Sinencio & Andreas G. Andreou (Editors)**, "Low-voltage/low-power integrated circuits and systems: low-voltage mixed-signal circuits", IEEE Press, New York, 1999.

- **Klaas-Jan de Langen & Johan H. Huijsing**, "Compact low-voltage and high-speed CMOS, BiCMOS, and bipolar operational amplifiers", Kluwer Academic Publishers, Boston, 1999.

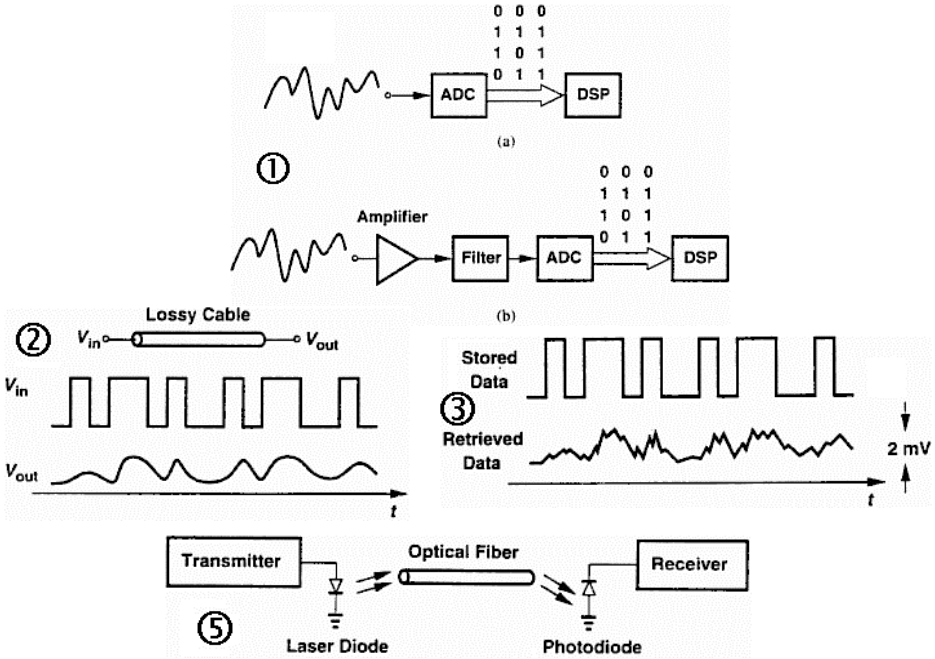
- **Satoshi Sakurai & Mohammed Ismail**, "Low-voltage CMOS operational amplifiers: theory, design, and implementation", Kluwer Academic Publishers, Boston, 1995.

- **Johan Huijsing, Rudy van de Plassche & Willy Sansen (editors)**, "Analog circuit design: volt electronics, mixed-mode systems, low-noise and RF power amplifiers for telecommunication", Kluwer Academic Publishers, Boston, 1999.

Why Analog?

Analog circuits are fundamentally necessary for

① *processing of natural signals*
② *digital communications*
③ *disk-drive electronics*
④ *wireless receivers*
⑤ *optical receivers*
⑥ *sensors*
⑦ *microprocessors and memories*



Analog design is much more difficult with respect to digital design, because

- *multidimensional trade-off considerations*
  (unlike digital design wherein one primary trade-off is dealed with)
- *analog signals are much more sensitive to noise, crosstalk and other interferers*
- *2nd order effects influence performance much more heavily*
- *design automation is not easy* (almost every device hand-crafted)
- *modeling and simulation of many effects bring difficulties*
  (evaluation of simulation results requires experience & intuition)
- *analog circuits fabricated in a digital (low-cost) process show low performance* (proposal of novel structures is required)

Why ***integrated*** analog circuits?

Great improvement in integration density and speed !

	1960	**2000**
Min. feature size:	25μm →	0.18μm

The complexity of ***on-chip*** analog circuits/systems can **no longer** be achieved by ***discrete*** analog circuits/systems.

There is a large demand for analog ICs for discrete use
(close to logic IC demand)

A large portion of the total IC market is occupied by *expensive* analog ICs.

Why *low-voltage* analog ICs ?

- power consumption of CMOS digital ICs proportional to $\mathbf{V_{DD}^2}$
  → **V_{DD} lowered to reduce power consumption**

- Diminishing device geometries
  → a thinner "thin oxide" has a lower breakdown voltage
  → **V_{DD} lowered**

  → ☹ *in mixed-mode ICs, performance of analog circuits degrade !*
  (limited voltage headroom to operate properly or even to "operate")

- Portable devices (e.g. medical devices, telemetry systems) supplied from 1V-1.5V (**low-voltage** + ***low-power*** techniques)

Alternative analog blocks and design methods required !

- Bipolar transistors are much more suitable for low-voltage operation (V_{BE}~0.6V), **but**
  ☹ bipolar digital circuits draw much current
  ☹ bipolar transistors are not good switches (*SC filters !*)
- BiCMOS seems to be a better choice, **but**
  ☹ BiCMOS processes are costly. Also, typically npn transistors are worth to be utilized
- How about CMOS ? Well, standart CMOS processes are more economical, **but**
  ☹ V_{GS} starts from above the threshold (~0.8V) for low currents and may tend to ***several volts*** for large currents.

OPTIMISTIC: "Let's lower the thresholds (*down to zero* ☺) ! Then we can supply significant headroom for the MOSFETs."
PESSIMISTIC: "Digital circuits require some non-zero thresholds to be able to decide on TRUEs and FALSEs. Moreover, a **very low V_{Th}** means a large *subthreshold leakage*, increasing the *standby* power consumption of digital circuits."

• Nevertheless, dual-threshold (or multi-threshold) CMOS processes do exist (high-speed/low-leakage • low-speed/high-leakage), though costly.

→ Special techniques are being developed to get rid of the leakage in digital circuits utilizing low-V_{Th} MOSFETs (Search the literature using the keywords ***MTCMOS***, ***DTCMOS*** and ***VTCMOS***).

OPTIMISTIC: "By the way... Don't we have the opportunity to operate the MOSFETs in subthreshold ? That can help."
PESSIMISTIC: "Right ! That IS done for **low-voltage low-power** (**LV-LP**) applications. Actually, **"LV-LP-LS"** would be a much better abbreviation (LS: Low-speed). I'm sorry !"

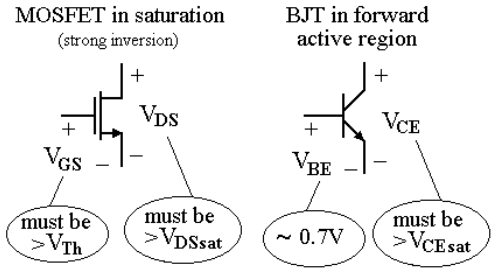
LV-LP techniques can find application in integrated systems which process *slow-changing* analog signals (e.g. heart beat → portable medical devices). For the sake of speed, **LP techniques** (i.e. subthreshol operation) will be kept **out of scope** of this course.

Low voltage limitations for MOSFETs and BJTs

In amplifiers, the transistors normally must achieve a large $\mathbf{r_o}$, a large $\mathbf{r_i}$ and a large $\mathbf{g_m}$.

MOSFETs → saturation

BJTs → forward active region



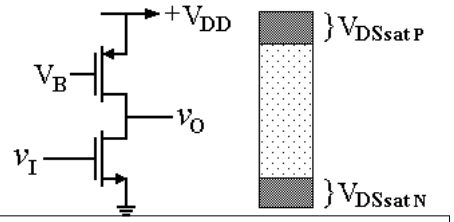
A MOSFET in saturation	**A BJT in forward active region**
$V_{GS} > V_{Th}$ & $V_{DS} > V_{GS}-V_{Th}$	$V_{BE} > 0$ (~0.7V) & $V_{CE} > V_{CEsat}$

BJT : $V_{BE} < 1V$, $V_{CEsat} < 0.5V$, even for large current levels.

MOSFET: V_{GS} may take values up to *several volts* for large currents. Then $\mathbf{V_{DSsat}}$ will also be large.

→ Therefore, **BJT**s are much more suitable for **LV** analog ICs.

The output swing of a CMOS active-loaded common-source gain stage can be almost ***rail-to-rail***, if the transistors have large enough **W/L** ratios.

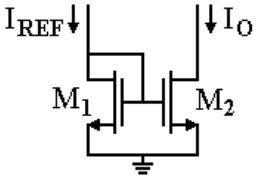


$I_D = \frac{1}{2}(W/L)\mu_n C_{ox} \cdot (V_{GS}-V_{Th})^2$

➔ $W/L = 2I_D/(\mu_n C_{ox} \cdot V_{DSsat}^2)$

i.e. For a *REAL* **rail-to-rail** output swing, we must use large MOSFETs

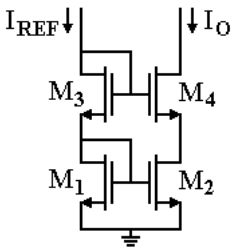
Nevertheless, this stage is suitable to be used as a **rail-to-rail** output stage.



A basic MOS current mirror also have some limitations.

- $\mathbf{V_{OUT}}$ should not drop below $\mathbf{V_{DSsat2}}$
  - $\mathbf{V_{IN}}=\mathbf{V_{GS1}} > V_{Th1}$. This voltage drop limits the output voltage swing of the preceding stage.

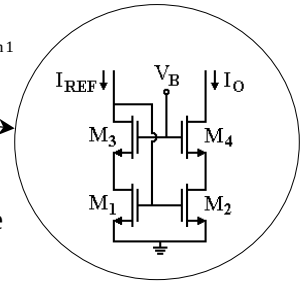
(much worse topologies exist – **e.g.** *cascodes*)



A cascode current mirror of this type consumes a lot of voltage headroom.

- $\mathbf{V_{IN}}=\mathbf{V_{GS3}}+\mathbf{V_{GS1}} > 2V_{Th1}$
- $\mathbf{V_{OUTmin}} = \mathbf{V_{DSsat4}} + \mathbf{V_{GS2}} > V_{Th1}$

Happily, good alternatives exist



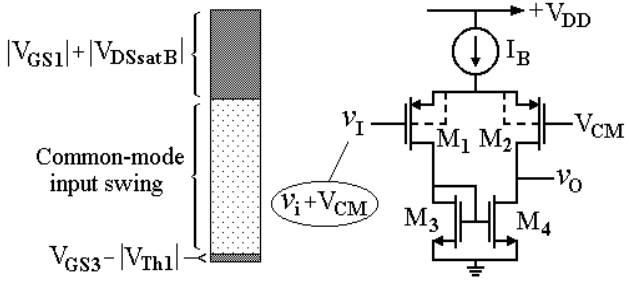
This "*low-voltage cascode current mirror*" → has an input voltage drop equal to that of the basic current mirror ($\mathbf{V_{IN}}=\mathbf{V_{GS1}}$). ☺

Output voltage limitation ($\mathbf{V_{OUTmin}}$) can be adjusted down to **2** $\mathbf{V_{DSsat}}$

The bias voltage $\mathbf{V_B}$ can also be adjusted *automatically* so as to achieve $\mathbf{V_{OUTmin}}$ • **2** $\mathbf{V_{DSsat}}$ for ***any*** current level.

HOMEWORK #1 : Carry out a literature search about "***automatic biasing of cascode stages or current mirrors***". Find **at least 5**, summarize the operation and mention significant advantages and drawbacks of **3** of them.

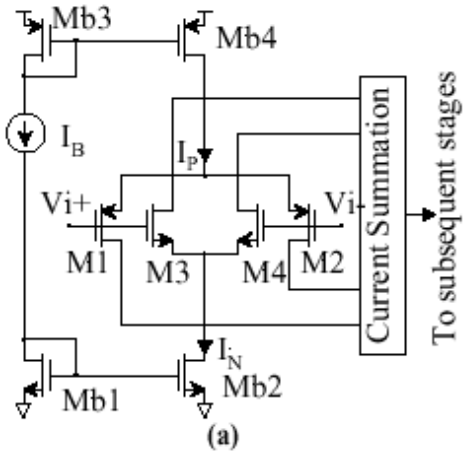
Common-mode input voltage swing of the differential pair is very good in one direction, but poor in the other direction.



Widening this range is vital for low-voltage operational amplifiers whose input stage is a differential pair.

Also, transconductance stages (transconductors) which are utilized in continuous-time $\mathbf{G_m}$-**C** filters require a wide voltage swing at the input.

☺ Combining one pMOS-input and one nMOS-input differential pair helps obtaining an almost *rail-to-rail* input common-mode voltage swing. ☹ However, this inserts additional difficulties to the design of the operational amplifier; as will be obvious shortly.



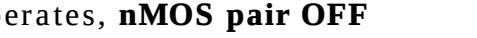
In the figure above, in **(a)**, it is shown how the pMOS-input and nMOS-input differential pairs must be connected. In **(b)**, combination of two common-mode input ranges are shown. It is obvious that a *rail-to-rail* common-mode swing is achieved.

V_{CM} close to **GND** : **pMOS** pair operates, **nMOS pair OFF**
V_{CM} close to V_{DD}: **nMOS** pair operates, **pMOS pair OFF**
V_{CM} close to $\frac{1}{2}V_{DD}$: **both** pairs operate

Therefore, there are **3** regions along which small-signal transconductance (G_m) of such a differential input stage takes **3** different values.

This is a **critical problem** since it means that, the **gain-bandwidth** (thus **speed**, and moreover, **stability**) of the opamp is *strongly dependent* on the common-mode input level.

"Constant-g_m rail-to-rail input stages" come as a solution for this problem. There are several different techniques trying to "*regulate*" the transconductance of such an input stage along the *rail-to-rail* input common-mode range. Those techniques will occupy an important part of this course. SOON !..



It may seem as if we are NOT taking into consideration bipolar transistors. **This not true**.

The investigations so far focused mainly on CMOS because,

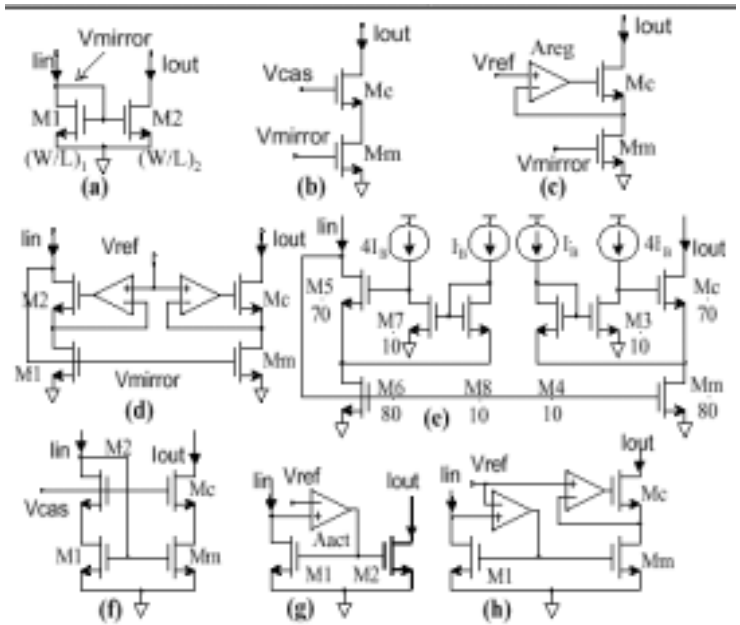
- CMOS is a standardized technology which avails cheaper production; therefore precedence is given to MOSFETs.
- MOSFETs degrade the low-voltage performance much worse with respect to BJTs; therefore MOSFETs deserve more care.

Later on, we will focus on BiCMOS **LV** techniques, but we must first cover some of the techniques devoted to CMOS.

It would be better starting with "**low-voltage current mirrors**" since they are extensively employed in integrated analog circuits.

Widely-used Current Mirrors

a: basic CM
b: cascode stage
c: regulated cascode stage
d: regulated cascodeCM
e: a low-voltage implementation of **(d)**
f: low-voltage cascode CM
g: active-input CM
h: regulated cascode active-input CM



Some of the above current mirrors are only conceptual. Those suitable for **LV** operation are **(a)**, **(e)** and **(g)**. Also, combining **(e)** and **(g)** could supply a **LV** version for the conceptual CM given in **(h)**.

The circuits on the right are very good examples for low-voltage current mirrors.

Analysis and design issues of these CMs would be helpful.