***Bipolar* and *BiCMOS* techniques for low-voltage operation**

Although upon this point dominantly **MOS-based** approaches have been presented for low voltage operation, a large percentage of those approaches are directly applicable to ***bipolar*** and ***BiCMOS*** circuits with minor modifications. Therefore, we didn't miss much !

Of course, those techniques utilizing special behavioral properties of the **MOSFET**s not possessed by the **BJT**s (***e.g.*** *square law, body effect, triode operation, etc.*) cannot be directly applied to bipolar circuits.

Also, there exist several high-performance **bipolar/BiCMOS** LV techniques (*special to BJTs*) that cannot be generalized (*at least with a sufficient performance*) to MOS-only circuits (***e.g.*** *log-domain filters*).

In this section, after revealing that most of the MOS-based LV techniques are directly applicable to **bipolar/BiCMOS** circuits, some advantages of ***BJT usage*** will be described and several **bipolar/BiCMOS** low-voltage circuit examples will be supplied. Also, some LV design approaches designed especially for bipolar transistor will be described in brief and some ***bipolar/BiCMOS*** examples will be supplied.

Comparison of *bipolar*, *CMOS* and *BiCMOS* technologies

In the table below, comparison of bipolar, CMOS and BiCMOS technologies is summarized.

Available features	Bipolar	CMOS	BiCMOS
Minimum current drain			X
High input impedance		X	X
Automatically scalable for low and medium speed digital control logic		X	X
Greater than 1GHz toggle frequency	X		X
Low 1/F noise	X		X
High dc gain	X		X
Low input offset for differential pair	X		X
Zero offset analog switches		X	X
High gain-bandwidth product			X
Good voltage reference	X		X

It is obvious that, availability of **MOSFET**s and **BJT**s in the same process (***BiCMOS***) makes it possible to combine their advantages.

Although the "performance" aspects of bipolar and CMOS circuits is apparent from the table above, comparing them from "LV suitability" point of view would be appreciated more.

Bipolar transistors have the following **advantages** over **MOSFET**s (*the origin(s) for some item sets may be same or correlated*) :

- The $\mathbf{V_{BE}}$ drop is usually smaller *wrt* to the $\mathbf{V_{GS}}$ drop of a MOSFET
- A large increase in current causes only a slight increase in $\mathbf{V_{BE}}$
- The collector-emitter saturation voltage is low
- Much better driving capability (*thus, much better speed*)

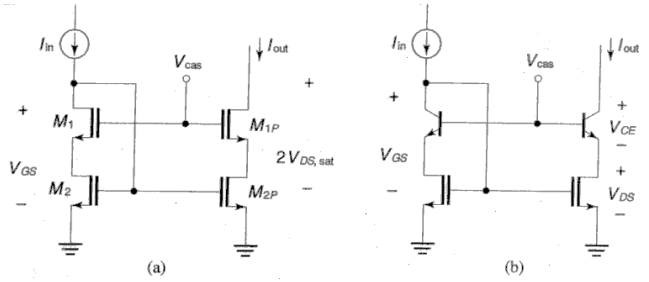
Beside advantages, **bipolar** transistors have some drawbacks :

- There is a non-zero base current
- The **pnp** transistor in a bipolar proces is usually low-performance
- "*Only-bipolar*" digital circuits consume to much power
- Bipolar switches are low-quality

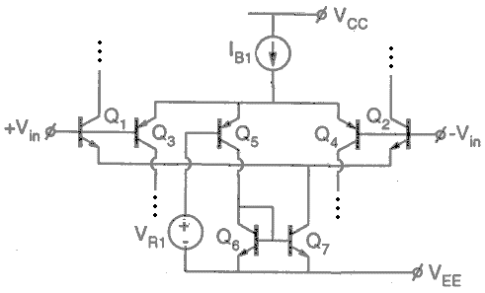
BiCMOS process seems to be the **ideal** process to work with but it is costly. "Plain" CMOS processes are much cheaper.

Let's first of all, by giving some examples, show that most of the LV design approaches used for CMOS are directly applicable to bipolar and/or BiCMOS technologies.

On the right, in **(a)**, a MOS LV cascode current mirror is shown. By replacin cascode MOSFETs with BJTs (see **(b)**), we can set equality of $\mathbf{V_{DS}}$ of $\mathbf{M_2}$ and $\mathbf{M_{2P}}$ better. Furthermore, the output swing is –typically- improved, since usually $\mathbf{V_{CEsat}}<\mathbf{V_{DSsat}}$ ☺. The *little* drawback is that, the **dc** voltage source $\mathbf{V_{cas}}$ must be able to supply the base currents (*this is a marginal drawback*). The lower MOSFETs also could be replaced with BJTs (*a bipolar **LV** cascode current mirror !*), but the base currents would cause errors.

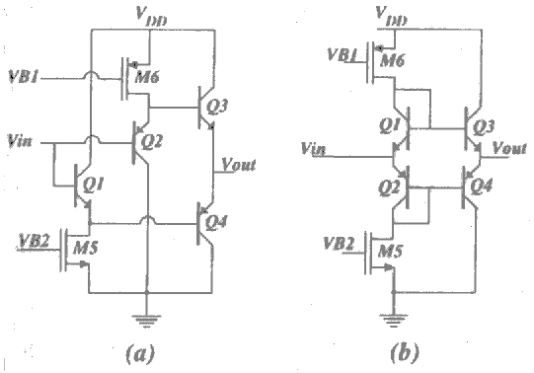


As a second example, on the right, a **bipolar** *constant-g_m rail-to-rail input stage* is shown. The operation is based on the **1:1** current mirror **Q_6-Q_7** . They are taking over the role of the well-known **1:3** MOS current mirrors of the CMOS *constant-g_m rail-to-rail input stage* shown on page **46** of the handouts. **Q_5** is a *current switch*, getting **ON** or **OFF** depending on the input CM voltage. In this way, ***only one*** inputr pair recives the bias current **I_{B1}**.



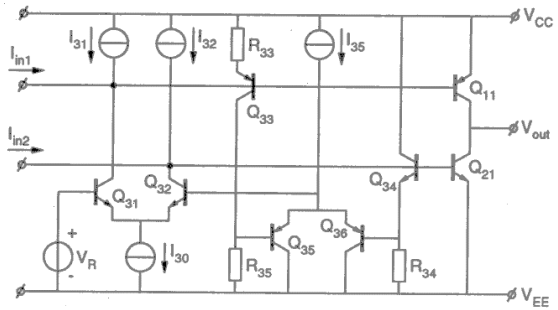
<u>The nice property:</u> Because **Q_5** can get **ON** and **OFF** much sharply with respect to a MOSFET, the region wherein both pairs are ON does not exist (*practically a very narrow region*). Even if this region exists, because the **$g_m=I_C/V_T$** for BJTs (*<u>linearly</u> dependent on **dc** current and independent of the type, geometry, etc. of the BJT*), it can have only a slight effect on flatness of the **g_m-$V_{i,CM}$** curve. ☺

On the right, two *class-AB* BiCMOS *emitter-follower* output stages (*buffers*) are given. The app-roaches are very similar to those mentioned elsewhere (*not explained in the handouts*) for CMOS design.



The adantage of these circuits over CMOS counterparts are, the better driving capability of bipolar transistors and much "*closer*" values of ***pnp*** and ***npn*** **V_{BE}** voltages, supplying a much better large signal linearity with respect to equivalent CMOS circuits.

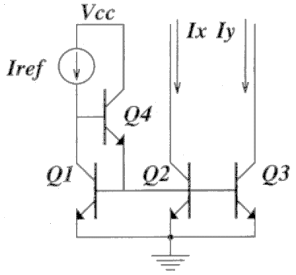
The figure below shows a bipolar ***class-AB*** rail-to-rail output stage with quiescent current control (*also supplying a non-zero* **I_{min}**). It is not difficult to notice that the circuit is very similar to the CMOS ***class-AB*** rail-to-rail output stage given on page **82** of the handouts.



So, if possible, we can use bipolar transistors to obtain better LV characteristics with a higher speed.

Low **V_{BE}** drops, low **V_{CEsat}**, linear dependency of **g_m** on **I_C** and better driving ability (*thanks to the larger **g_m** for the same current*) are good reasons to make use of BJTs in LV analog circuits.

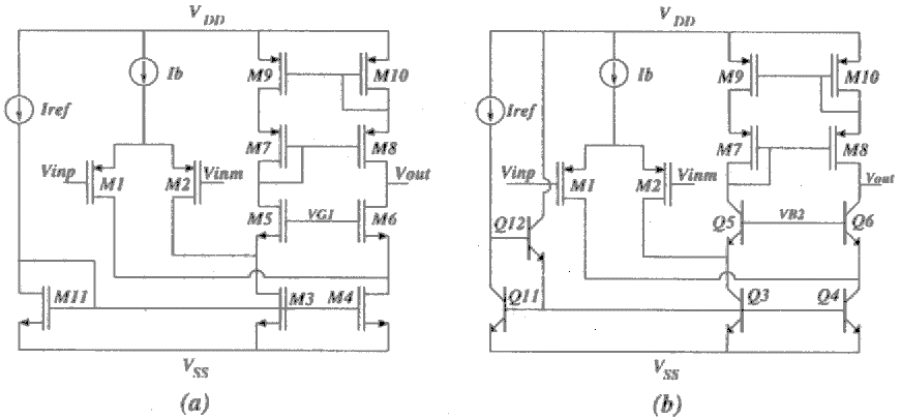
The drawbacks (*like the non-zero base current*), can be overcome as in the bipolar current mirror on the right. Using bipolar current mirrors is adanmtageous for low voltage operation, accuracy (*better matching*) and speed.



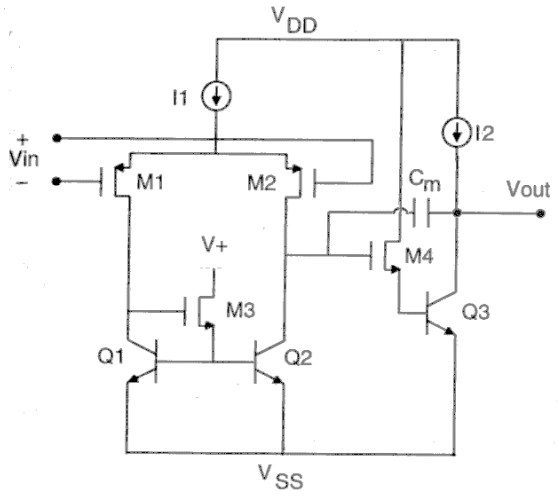
MOSFETs can be used as *high-input-impedance* devices (*this is possible in **BiCMOS***) and BJTs can

be used as *high-drive-capability* (***large-g_m***) devices. The BiCMOS folded cascode operational amplifier in **(b)** of the figure below is a good example. Notice how the CMOS version in (a) is converted to the BiCMOS version in **(b)**.

(**<u>note:</u>** ***pnp*** *BJTs are not used along signal paths, because of their poor performance characteristtics in standart BiCMOS*)



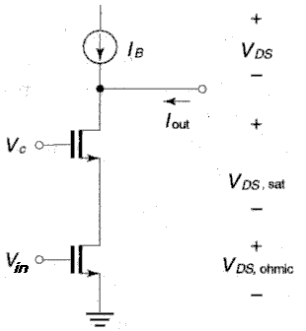
Another BiCMOS opamp example is given on the right. Notice how **MOSFET**s were used when *high-input-impedance* levels are needed and **BJT**s were preferred where *high drive capability / high speed / low voltage drop / good matching* are required.



The driving capability of BJTs can be very helpful in stabilizing (*regulating*) a node voltage. In low-voltage ***triode transconductors***, such an ability is required.

Below, a MOS triode transconductor is shown. Such circuits are used in filter design; they are expected to be **tunable**.

The lower transistor is forced to operate in triode region (*to behave like a resistor*) by the upper transistor. Assuming $\boldsymbol{v_{GS}}$ (corresponding to $i_D=I_B+i_{out}$) of the upper (*cascode*) transistor fixed at the **dc** level $\mathbf{V_{GS}}$ (corresponding to $i_D=I_B$), the small-signal transconductance can be given as $\mathbf{G_m=\beta_{triode}V_{DS,triode}=\beta_{triode}(V_c-V_{GS,casc})}$.



Thus, linear tuning of the $\mathbf{G_m}$ is possible via $\mathbf{V_c}$ and the $\mathbf{G_m}$ is independent of $\boldsymbol{i_{out}}$.

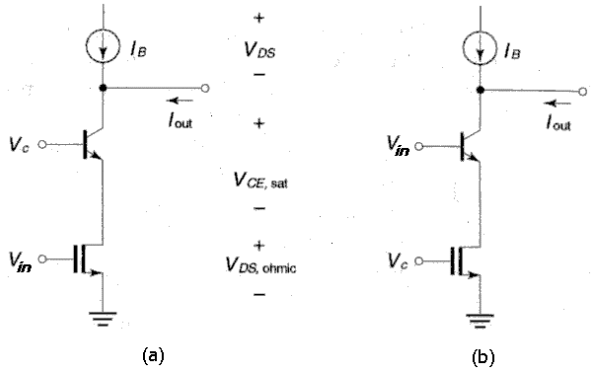
The cascode transistor must be chosen large enough for keeping $\mathbf{V_{GS,casc}}$ (thus $\mathbf{V_{DS,triode}}$). This in turn increases the consumed area and parasitic capacitances. ☺

Replacing the cascode MOSFET with an **npn BJT** improves the behavior (*See **(a)** in the figure below*). The exponential dependency of current on V_{BE} avails this.

Note that the output voltage swing will be even better, thanks to the low $\mathbf{V_{CEsat}}$ value.

In **(b)**, an alternative *tunable* transconductor is obtained by *interchanging* the **input** and **tuning** terminals. Actually, this is a source degenerated common-source stage with small-signal transconductance

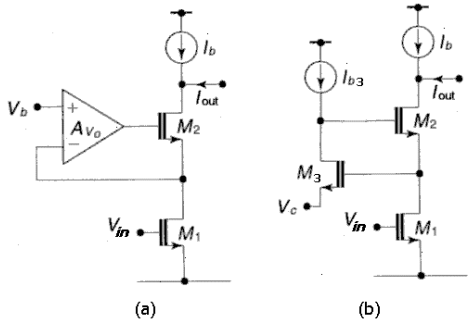
$$\mathbf{G_m=g_{mQ}/(1+g_{mQ}R_{on})}$$



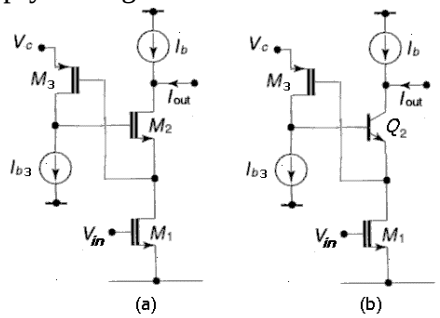
where $\mathbf{g_{mQ}}$ is the small-signal transcondcutance of the BJT and $\mathbf{R_{on}}$ is the **on-resistance** of the triode MOSFET: $\mathbf{R_{on}=[\beta_{triode}(V_c-V_{TH})]^{-1}}$

$\mathbf{G_m=1/R_{on}=\beta_{triode}(V_c-V_{TH})}$ can be obtained if $\mathbf{g_{mQ}R_{on}>>1}$ (***i.e.*** $\mathbf{g_{mQ}}$ is large enough *wrt* the aimed $\mathbf{G_m}$). Thus, a tunable (*via* $\boldsymbol{V_c}$) transconductance is once again obtained.

Active feedback can be used to regulate the drain node of the triode MOSFET. The copceptual circuit is given in **(a)** on the left. An efficient solution is supplied in **(b)**. In this circuit, unfortunately, $\mathbf{V_{DS,triode}}$ cannot be forced below one $\mathbf{V_{TH}}$ (*limited by* $\boldsymbol{V_{GS3}}$). Therefore, tuning range is narrow for low supply voltages.

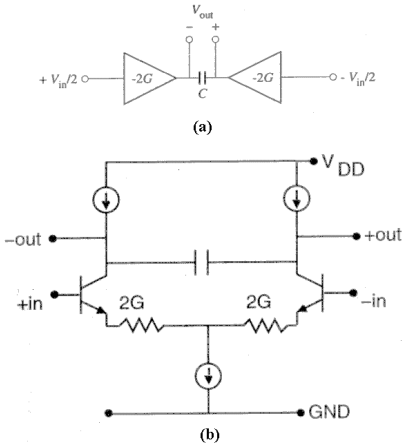


The ***nMOS*** $\mathbf{M_3}$ can be a ***pMOS*** transistor, but in this case, proper operation of M_2 and M_3 becomes very critical (*even impossible for some CMOS processes*). In **(a)** on the right, such a circuit is given. Assuming M_1 in triode and M_2-M_3 in saturation, it is obvious that $\mathbf{V_{DS,triode}}$ can be adjusted

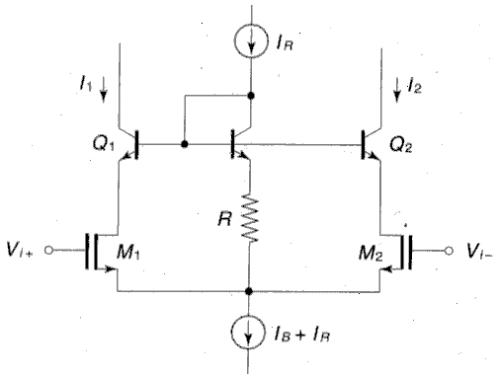


down to the ground level via $\mathbf{V_c}$. Therefore, the tuning range is wide enough. In order to keep M_3 in saturation, however, $\mathbf{V_{GS2}<|V_{THp}|}$ must be supplied, which is not easy for many CMOS processes.

Replacing M_2 with an npn BJT *(possible for BiCMOS)*, as in **(b)** of the figure above, relaxes the design largely, since, for typical processes, " $\mathbf{V_{BE}<|V_{THp}|}$ " is an easier condition to satisfy.



Not only *triode* MOSFETs, but **bipolar** transistors (*sometimes together with resistors to improve linearity*) can be used to obtain tunable transconductors, like the one the right (*the differential connection helps increasing the output swing, as well as linearizing the behavior*). The tail current can be used to tune the $\mathbf{G_m}$. The exponential behavior of the BJT supplies a vey wide tuning range (up to **4 decades !** is achievable). ☺



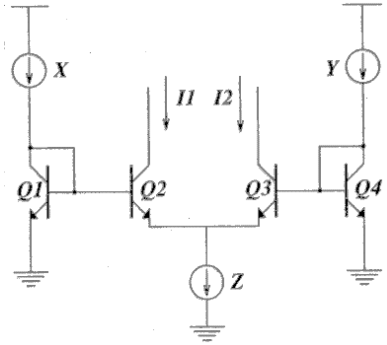
In the circuit on the left, notice how, the BJTs, triode MOSFETs, a resistor and a current source are used together to obtain a current-tunable triode transconductor. ☺

The exponential behavior helps the bipolar transistors be an ideal device for signal compression, like in the "companding (or ***log-domain***) filters". The signal is first companded, then processed (*using special functions*) and finally expanded once agin. The result is a " *linearly filtered* " version of the original signal.

In current-mode continuous-time filters (*or, to be more general,* ***analog signal processors***), BJTs are very suitable since they can achieve the required ***low-impedance nodes*** with less power and area consumption *wrt* MOSFETs.

It is worth mentioning that, also MOSFETs can be employed in companding (*square-roor-domain*) filters and current-mode *analog signal processors*, however, their performance is significantly worse with respect to bipolar versions.

The **translinearity principle** is a very interesting start point to obtain **linear** operations from nonlinear devices. It makes use of *translinear loops*. The nonlinear device can be a BJT in forward active reagion or a MOSFET in saturation. Of course, BJT is much more suitable.



A translinear circuit is shown in the figure on the right. The $\mathbf{V_{BE}}$ voltage drops of the transistors form a translinear loop, such that,

$$-V_{BE1}+V_{BE2}-V_{BE3}+V_{BE4} = 0 \quad \rightarrow \quad \mathbf{V_{BE2}+V_{BE4}=V_{BE1}+V_{BE3}}$$

By using $V_{BE}=V_T\, ln\,(I_C/I_S)$, one can obtain

$$V_T\, ln\,(I_1/I_S) + V_T\, ln\,(I_y/I_S) = V_T\, ln\,(I_x/I_S) + V_T\, ln\,(I_2/I_S)$$
$$ln\,(I_1 I_y/I_S^2) = ln\,(I_x I_2/I_S^2)$$

Finally, we obtain, $\mathbf{I_1 I_y = I_x I_2}$. Because the tail current mandates $I_2+I_3=I_z$, we finally obtain the difference of the output currents as

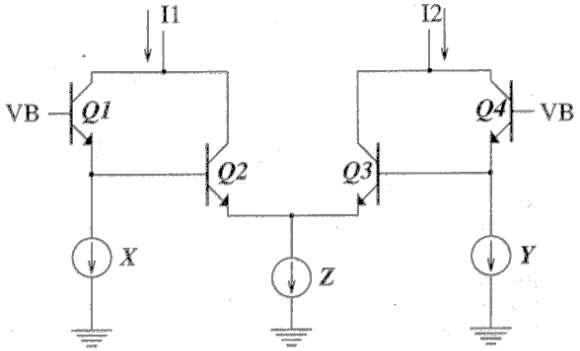
$$\mathbf{I_1 - I_2 = z\,(x-y)/\,(x+y)}$$

This is a very flexible function which can be converted into useful functions if proper inputs are applied.

For instance, if x and y signals are opposite parts of a differential signal (***i.e.*** $\mathbf{I_x=I+}i$ and $\mathbf{I_y=I-}i$) and z is a controlled dc current (such that $\mathbf{I_z=kI}$), then we obtain $\mathbf{I_1 - I_2 = k}i$. So, this becomes a <u>*linear*</u> ***variable-gain*** **current amplifier**; gain controlled by $\mathbf{I_z}$.

If $\mathbf{I_z}$ is taken as another signal input ($\mathbf{I_z}=i_z>0$), then the circuit becomes a ***2-quadrant*** **analog multiplier** (*2-quadrant, because* ***i*** *can be negative and positive, whereas* I_z *must be positive*): $\mathbf{I_1 - I_2 = i_z}\,i\,/\mathbf{I}$. ($i_z>0$)

Although there are numerous translinear circuits, only a second translinear circuit example will be supplied; given on the right.



It can be shown that, this circuit satisfies a function

$\mathbf{I_1 - I_2 = (x - y)\,[\,1 - z/(x+y)\,]}$

It is nor hard to find out that, for $\mathbf{I_x = I + i}$, $\mathbf{I_y = I - i}$ and $\mathbf{I_y = 2I - i_z}$, the circuit behaves like a ***4-quadrant* analog multiplier**: $\mathbf{I_1 - I_2 = i_z\, i\ /I}$. ($i_z$ and i can be positive or negative ☺).

By using circuits like these, current-mode linear or piecewise-linear functions, like, multiplication, division, square-root, absolute value, maximum or minimum value (*among multiple inputs*), etc. can be obtained.

References used for the **"*Bipolar* and *BiCMOS* techniques for low-voltage operation"** section

- Sanchez-Sinencio, E. and Andreou, A.G. (Editors), "*Low-voltage/low-power integrated circuits and systems: low-voltage mixed-signal circuits*," IEEE Press, New York, 1999.

- van de Plaasche, R.J., Sansen W.M.C. and Huijsing, J.H. (Editors), "*Analog Circuit Design : Low- power/low-voltage, integrated filters, and smart power*, " Kluwer Academic Publishers, Dordrecht, 1995.

- Ismail, M., and Fiez, T., "*Analog VLSI signal and information processing*," McGraw-Hill, Singapore, 1994.