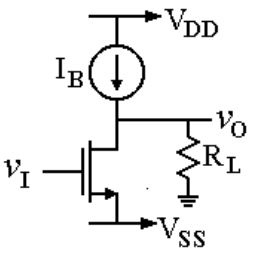
The common-source (**CS**) stage is a good alternative since its output swing can be extented from rail to rail. Also body effect does not exist.☺




A conventional ***class-A*** **CS** stage (*see the figure on the right*) will be sufficient in applications like ***switched-capacitor filters***, where the loads are small capacitors (*easy-to-drive*).

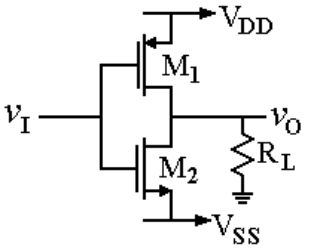
However, when the load is a *low-impedance* one (***e.g.*** an *off-chip* ohmic load like an ***earphone*** , or an *off-chip* large capacitive load ), the large-signal driving capability will be limited; particularly because of the fixed bias current $\mathbf{I_B}$ (*max. value of the current outwards will be* $\boldsymbol{I_B}$). So as to obtain a good driving capability and/or *slew-rate*, $\mathbf{I_B}$ must be chosen large enough; yielding a large quiescent current, thus a large quiescent power consumption (*the quiescent current* $\boldsymbol{I_Q}$ *is equal to* $\boldsymbol{I_B}$ *for this case*).

☝ The output stage is the most **power consuming** part of an opamp. Therefore, special care must be taken to obtain a *power-efficient* operation, while keeping other performance characteristics within acceptable limits.



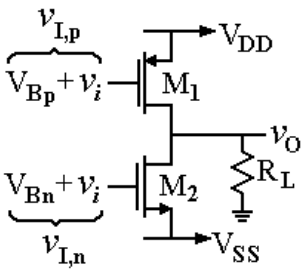
As integration density gets larger, dissipating large power on devices becomes a more critical problem. Trying to keep the power consumption as low as possible is important fom this point of view as well.

The **class-B** output stage is a very efficient configuration, but possesses a ***dead region*** along which both transistors are **OFF**. Unfortunately, this region is usually located around the quiescent (bias) point (*That is why the quiescent power is* ***ZERO****; enhancing the power efficiency* ☹ ). In opamps, we **cannot** tolerate the distortion level caused by such a stage.




☝ The output stage must be able to drive the load impedance without degrading the *unloaded* performance and without introducing intolerable distortion.

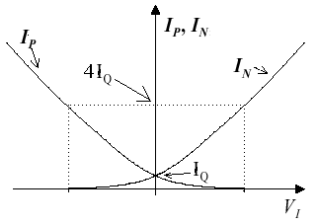





By allowing some current flow over the MOSFETs for the quiescent condition, we can avoid the dead region. Then, the quiescent power consumption is ***not zero*** ☹ but **low enough** ☺; and the output current can be increased for large signal operation (*as in class-B*). This operation is called the ***class-AB*** *operation*. The efficientcy is still large enough.

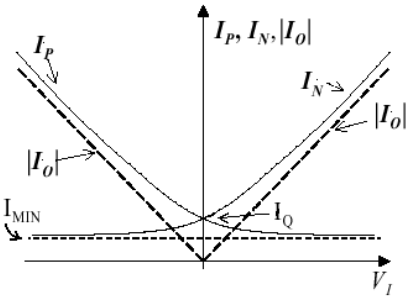
The control of the quiescent current $\mathbf{I_Q}$ is important since it must guarantee that both transistors are ON for quiescent condition, besides determining the small-signal behavior of the amplifier.

It is obvious that, as long as the bias voltages $\mathbf{V_{Bn}}$ and $\mathbf{V_{Bp}}$ are **fixed**, one of the MOSFETs will go **OFF** as $\boldsymbol{v_i}$ travels towards one of the rails. When MOSFETs are employed, it can be shown that when one MOSFET reaches the current level $\mathbf{4I_q}$ the other one goes **OFF** ($\boldsymbol{\beta_n=\beta_p}$ *and* $\boldsymbol{V_{THn}=|V_{THp}|}$ *assumed*). (***see the curve***)






Because of the delay caused by ***ON-OFF*** *transitions* of the MOSFETs, for the sake of **speed**, both transistors must be kept **ON** for all cases (*at least, a small amount of* ***minimum*** *current* $\boldsymbol{I_{MIN}}$ *must flow along, otherwise, a large* ***crossover distortion*** *is observed for high-frequency large signals*).




The desired curve is given on the right.

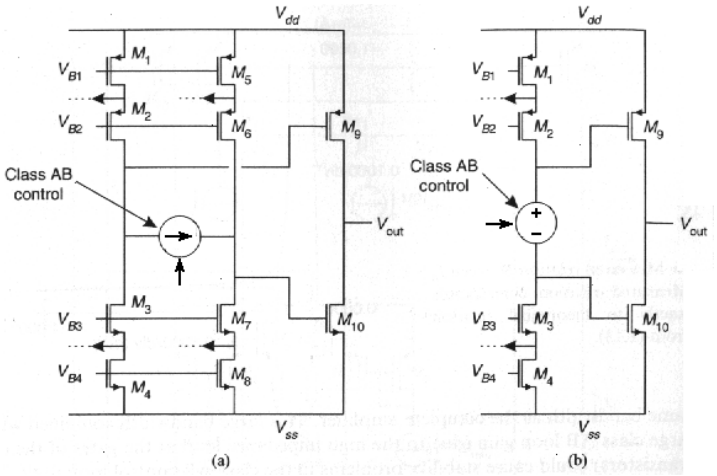
Trying to keep both transistors allways **ON** requires continuous adjustment (***class-AB control*** ) of $\mathbf{V_{Bn}}$ and $\mathbf{V_{Bp}}$.

***example case:*** When $\boldsymbol{v_{I,n}}$ tends to $\mathbf{V_{DD}}$ , $|\boldsymbol{v_{GS1}}|$ will tend to **zero** for a fixed $\mathbf{V_{Bp}}$ . However, reducing $\mathbf{V_{Bp}}$ accordingly will help keeping $\mathbf{M_1}$ **ON**).

The **class-AB control** of the current $\mathbf{I_Q}$ (*and* $\boldsymbol{I_{MIN}}$) can be performed by accordingly controlling one or two voltage sources or current sources, as depicted in the figure below. This control may be performed by using *samples* of the input signal or the output signal.

In other words, the **class-AB control** can be performed via

- ***feedforward*** techniques
- ***feedback*** techniques

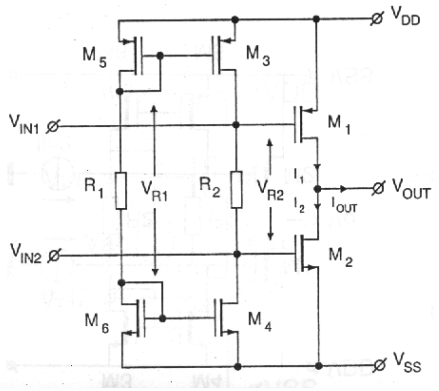



The ***feedback*** technique is usually better in achieving an accurate **quiescent current control** while enabling operation for lower supply voltages.

The ***feedforward*** technique, on the other hand, is **faster** (the ***feedback*** technique slows down the output stage; furthermore some ***stability precautions*** may be required ).



A simple ***feedforward*** structure is shown in the figure on the right (*The input voltages* $\mathbf{V_{IN1}}$ *and* $\mathbf{V_{IN2}}$ *are not necessarily voltage sources; they can be formed with aid of input currents*). Although resistors are used to obtain a fixed voltage $\mathbf{V_{R2}}$, transistors could also be used (*An example for such a circuit will also be supplied shortly*).




$\mathbf{M_3}$-$\mathbf{M_5}$, $\mathbf{M_4}$-$\mathbf{M_6}$ and $\mathbf{R_1}$-$\mathbf{R_2}$ pairs are assumed matched. The quiescent current can be obtained as follows:

$$V_{GS1} + V_{GS2} + V_{R2} = V_{GS5} + V_{GS6} + V_{R1}$$

$$\sqrt{I_1} + \sqrt{I_2} = 2 \cdot \sqrt{I_q}$$

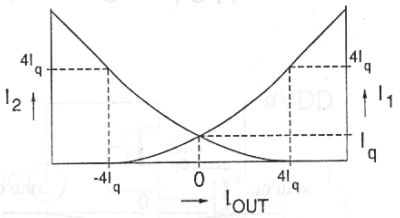
$$I_q = \left(\frac{W}{L}\right)_1 \left(\frac{L}{W}\right)_5 \cdot \frac{V_{R2}}{R_2}$$

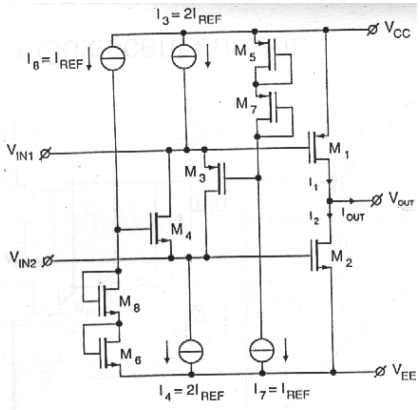
Unfortunately, the quiescent current is dependent on $\mathbf{V_{DD}}$ via $\mathbf{V_{R2}}$. Furthermore, for large signals, one of the output transistors will be **OFF** ($\mathbf{I_{MIN}}$**=0A**) (see the curve given on the



right). This limits the large signal speed.

The top and bottom current sources guarantees large input impedances at the input nodes (*required to obtain a large voltage gain*).




The circuit on the left, wherein current sources and transistors are employed, is more advantageous since the voltage difference $\mathbf{V_{IN1}}$-$\mathbf{V_{IN2}}$ can be kept independent of $\mathbf{V_{DD}}$ as long as $\mathbf{I_{REF}}$ is *supply-independent*.

The increased number of **series** $\mathbf{V_{GS}}$ **drops** in this *all-MOSFET* version may limit the minimum supply voltage. ☹

The quiescent and minimum currents ($\mathbf{I_{MIN}}$ is <u>not</u> zero ☺) for this circuit are obtained below:



$$\sqrt{I_1 \frac{L_1}{W_1}} + \sqrt{I_3 \frac{L_3}{W_3}} = \left(\sqrt{\frac{L_5}{W_5}} + \sqrt{\frac{L_7}{W_7}}\right)\sqrt{I_{REF}}$$

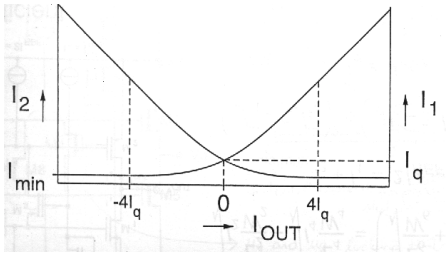
$$\sqrt{I_2 \frac{L_2}{W_2}} + \sqrt{I_4 \frac{L_4}{W_4}} = \left(\sqrt{\frac{L_6}{W_6}} + \sqrt{\frac{L_8}{W_8}}\right)\sqrt{I_{REF}}$$

$$I_3 + I_4 = 2I_{REF}$$

$$\left(\sqrt{I_1} - 2\sqrt{I_q}\right)^2 + \left(\sqrt{I_2} - 2\sqrt{I_q}\right)^2 = 2I_q$$

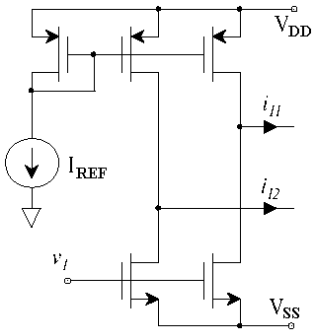
$$I_q = I_{REF}$$

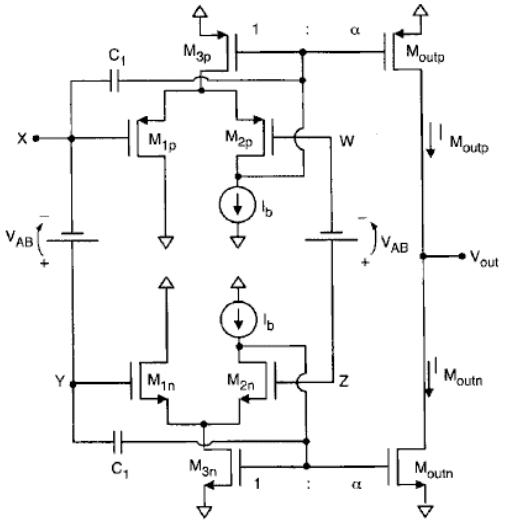
$$I_{min} = (2 - \sqrt{2})^2 I_q \approx 0.34 I_q$$




This circuit is widely used as output stage of **LV** opamps.

The input currents can be the "**summed up**" currents of the ***p***- and ***n***-type input pairs. Alternatively, if the input signal is in *voltage mode*, a simple *double-output* transconductor (*an example given on the right*) can be used to obtain these current signals.






Another output stage example for the *feedforward approach* is shown on the left. Here, the minimum supply voltage is not limited by several $V_{GS}$ drops ☺. This is made possible with help of the $\mathbf{V_{AB}}$ voltage difference (such that, $\mathbf{V_X<V_Y}$ for LV operation. When large $\mathbf{V_{DD}}$ values are used, it is wiser to satisfy $\mathbf{V_X>V_Y}$).

The circuit can be operated from a supply voltage slightly greater than the threshold voltage of the transistors.

The quiescent current is well-defined at a value, $\mathbf{I_Q=2\alpha I_b}$ . The additional advantage is that, unlike the previaous examples, $\mathbf{I_{MIN}}$ is also well-controlled via an expression, as simple as that of the quiescent current: $\mathbf{I_{MIN}=\alpha I_b}$ . ☺



So as to avail a <u>proper</u> ***LV*** operation, $\mathbf{V_{AB}=V_Y-V_X}$ must be chosen such that, the transistors $\mathbf{M_{1p}}$ , $\mathbf{M_{2p}}$ , $\mathbf{M_{3p}}$ , $\mathbf{M_{1n}}$ , $\mathbf{M_{2n}}$ , $\mathbf{M_{3n}}$ all operate in (***but*** *close to the limit of*) saturation. Suitable values for $\mathbf{V_X}$ and $\mathbf{V_Y}$ can be

$$\mathbf{V_X=V_{DD}-|V_{GS1p,Q}|-|V_{DSsat3p}|-\Delta V} \quad , \quad \mathbf{V_Y=V_{GS1n,Q}-V_{DSsat3n}+\Delta V}$$

where $\mathbf{\Delta V}$ is a small margin (**e.g.** 50mV) to guarantee saturation. Then, the appropriate value for $\mathbf{V_{AB}}$ is obtained as

$$\mathbf{V_{AB}=V_{GS1n,Q}+|V_{GS1p,Q}|-2V_{DSsat}-V_{DD}+2\Delta V}$$

Then, $\mathbf{V_{AB}+V_{DD}}$ can be kept less than **2V** for typical processes (***e.g.*** $\mathbf{V_{TH}=0.8V}$) and large enough transistors.

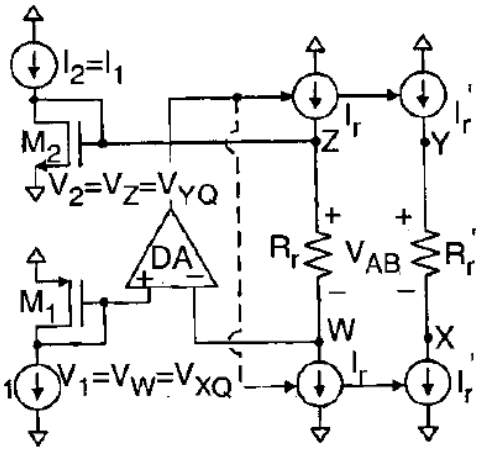
Since a $\mathbf{V_{AB}}$ larger than $\mathbf{V_{DD}}$ <u>**cannot**</u> be supplied (unless a ***charge pump*** is used), $\mathbf{V_{AB}<V_{DD}}$ must be satisfied. Then we obtain the limitation for $\mathbf{V_{DD}}$ as " $\mathbf{V_{DD}>1V}$ ". This is a much better result with respect to previous *feedforward-based* output stages.

The capacitors are used to guarantee a stable feedback since the utilized amplifiers may supply large gain (<u>**important:**</u> this feedback is



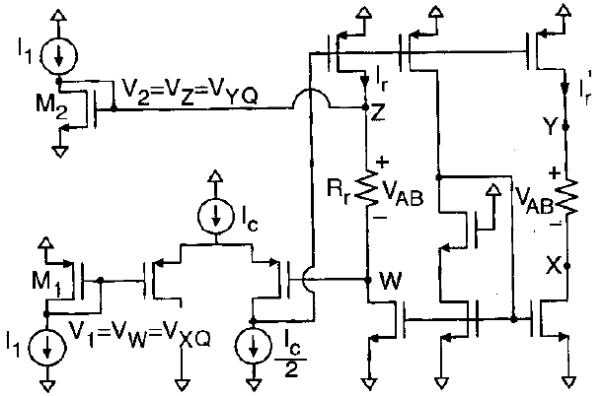
<u>**not**</u> using a copy of the current/voltage of the output transistors; it is used *intensively* for proper operation of the feedforward circuitry)

On the right, a conceptual circuit is given which can be utilized to obtain the $\mathbf{V_{AB}}$ voltage. The differential amplifier (**DA**) controlling the matched current $\mathbf{I_r}$ , together with the resistor $\mathbf{R_r}$ form the voltage $\mathbf{V_{AB}=I_rR_r}$ across the nodes **Z** and **W**. With aid of the $\mathbf{I_r'}$ currents ($\mathbf{I_r'=I_r}$) and the resistor $\mathbf{R_r'}$ ($\mathbf{R_r'=R_r}$), the desired *floating* $\mathbf{V_{AB}}$ voltage is achieved across the nodes **Y** and **X**. Using currents $\mathbf{I_2=I_1}$ the quiescent voltage values for $\mathbf{V_X}$ and $\mathbf{V_Y}$ ($\mathbf{V_{XQ}}$ and $\mathbf{V_{YQ}}$) are supplied.




Below is a practical realization of this circuit.



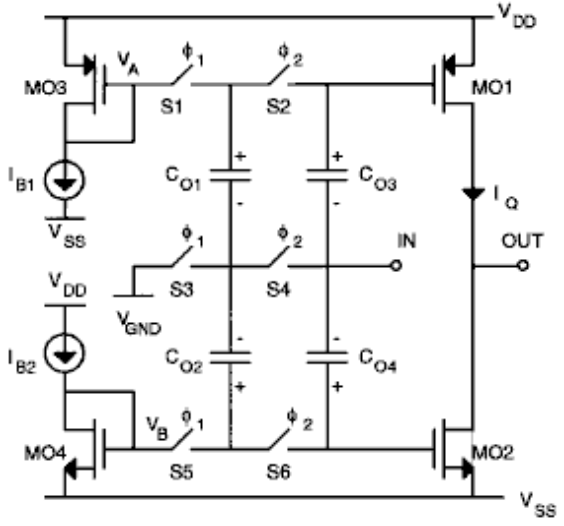



Provided that the bias currents are supply-independent, as long as the $\mathbf{V_{AB}}$ voltage is positive, it remains *independent* of the supply voltage $\mathbf{V_{DD}}$.

This is an appreciated feature since it enhances the **PSRR**.

As $\mathbf{V_{DD}}$ supply increases above **2V** (*for the above limit example*), $\mathbf{V_{AB}}$ must be negative (**i.e.** $\mathbf{V_X>V_Y}$ *must be satisfied*). For such larger $\mathbf{V_{DD}}$ values, the above circuit can still be used by just interchanging the **X** and **Y** nodes.

Another interesting *feedforward-based* circuit for obtaining a *well-defined* $\mathbf{I_Q}$ is shown below. This circuit uses "*dynamic biasing*" with aid of switches and capacitors, so as to achieve the required




quiescent voltages of the nodes **A** and **B** (*respective gate voltages of the **pMOS** and **nMOS** output transistors*). $\phi_1$ and $\phi_1$ are non-overlapping clock phases.

- **When $\phi_1$ is "1":**
  **S1**, **S3** and **S5** are closed (*others open*) ; thus the required $V_A$ voltage is obtained across $C_{O1}$ and $V_B$ voltage is obtained over $C_{O2}$.
- **When $\phi_2$ is "1":**
  **S2**, **S4** and **S6** are closed (*others open*); thus the required voltage difference $V_{AB}$ is obtained across $C_{O3}$ and $C_{O4}$ -*in series*. (**note:** *Actually, this equalization process will require several clock periods to settle, since the function is a damped **SC** integration*).



If we choose $I_{B1}=I_{B2}=I_B$ and achieve a *ratioed* matching among the transistors, such that $\beta_{O1}/\beta_{O3}=\beta_{O2}/\beta_{O4}=\alpha$, then, for the steady-state (*quiescent*) case for which $I_{DO1}=I_{DO2}$ (*equal to $I_Q$, by definition*), the output transistors are forced to be **ON** with a well-controlled quiescent current: $I_Q=\alpha I_B$.

This design focuses on obtaining a *well-controlled* $I_Q$ but unfortunately does not supply a non-zero $I_{MIN}$. ☹

$C_{O3}$ and $C_{O4}$ must be chosen large enough compared to $C_{GSO1}$ and $C_{GSO2}$ , so as to avoid the charge loss during large-signal transients, as far as possible.

Due to a large input drive, $V_{GO1}$ and $V_{GO2}$ may be pulled beyond $V_{SS}$ and above $V_{DD}$ , respectively. This swing is limited by the forward biasing of the switch bulk junctions (*the forward-biased junctions rapidly discharges the capacitances $C_{O3}$ and $C_{O4}$*)

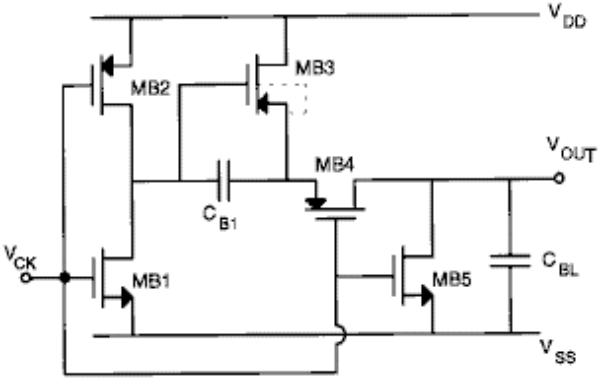
Note that the switches **S3** and **S4** -*even for steady-state*- will have their sources/drains connected to the mid-rail. Assuming that **"1"**



and **"0"** levels are corresponding to $V_{DD}$ and $V_{SS}$, and considering a typical threshold of $V_{TH}$**=0.8V**, we find that, the minimum power supply requirement ($V_{DD}+|V_{SS}|$ *for this example*) is *typically* limited by **1.5V**.

If we could have supplied a larger ($>V_{DD}$) gate voltage for the switch transistors, we could have coped with this limitation.

As a solution, a ***clock booster*** can be used. An example is given in the figure on the right. Such a circuit can supply **"1"** levels which are $>V_{DD}$. It is more convenient for such circuits if the *driving point impedance* is **high** (*drawing small currents*).





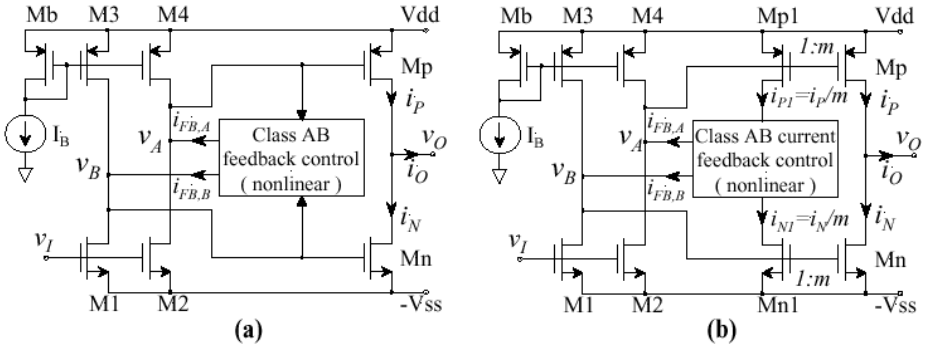

In steady-state (***clock* LOW**), $M_{B1}$ and $M_{B2}$ operate as an inverter.

When the clock is **HIGH**, capacitor $C_{B1}$ is precharged to $V_{DD}$ through transistor $M_{B3}$ (*during this process, the upper terminal behaves like a **source** and the transistor is usually in the triode region).* During this process, $V_{GB4}=V_{DD}$ and $V_{SB4}$ travels from $V_{SS}$ to $V_{DD}$ ; $M_{B4}$ is **OFF**, whereas $M_{B5}$ is **ON**, discharging load capacitor $C_{BL}$.

When the clock goes down, the output of the inverter $M_{B1}$-$M_{B2}$ goes to $V_{DD}$ . Then, $M_{B3}$ and $M_{B5}$ are **OFF** , whereas $M_{B4}$ is **ON**. If $C_{B1}$ is chosen much larger than $C_{BL}$, the output voltage is boosted above $V_{DD}$. Although $V_{OUT}$ tries to reach $2V_{DD}$, during the last part of the transient, the bulk junctions of $M_{B3}$ limit this to approximately $V_{DD}$**+0.6V**. Nevertheless, this is a sufficiently high voltage to drive the switches **S3** and **S4** in the output stage, when a power supply of $V_{DD}+|V_{SS}|$**=1.2V** is used.

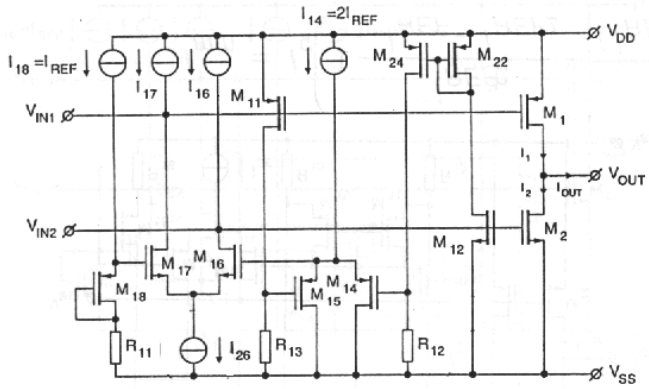
So, the ***SC** techniques* seem to be quite promising for obtaining functional analog circuits operated from low power supplies.

The ***feedback*** *approach* for ***class-AB control*** is generally performed by using copies of drain currents or gate voltages of the output transistors, to obtain an information about the output signal.




In the figure above, (a) and (b) shows generalized structures for ***feedback***-based ***class-AB control*** via using the gate voltages and drain currents of the output transistors, respectively.






On the left, a good example for ***feedback*** *approach* is supplied.

A copy of $\mathbf{I}_1$ flows on $\mathbf{R}_{13}$ and a copy of $\mathbf{I}_2$ on $\mathbf{R}_{12}$ .

Assuming $\mathbf{M}_{14}$-$\mathbf{M}_{15}$ and $\mathbf{R}_{12}$-$\mathbf{R}_{13}$ pairs matched, we find $\mathbf{V}_{G14}=\mathbf{V}_{G15}$ for **quiescent** conditions.

Then, assuming $\mathbf{M}_{18}$ matched with $\mathbf{M}_{14}$-$\mathbf{M}_{15}$ and $\mathbf{R}_{11}$ matched with $\mathbf{R}_{12}$-$\mathbf{R}_{13}$ , we obtain $\mathbf{V}_{G17}=\mathbf{V}_{G16}$ , thus $|\mathbf{I}_{11}|=\mathbf{I}_{REF}$ .

$$I_q = \frac{W_1}{L_1}\frac{L_{11}}{W_{11}} I_{REF}$$

$$I_{min} = I_q\left(1 - \frac{(\sqrt{2}-1)}{R_{12}}\sqrt{\frac{2L_{14}}{\mu_p C_{ox} W_{14} I_{REF}}}\right)$$

In this way, the quiescent and minimum currents are well defined as given on the left.



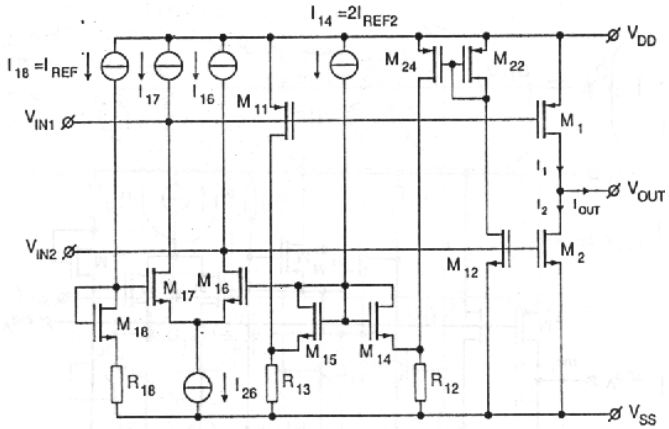
$\mathbf{I}_{MIN}$ is kept non-zero with the aid of the feedback loop, as described below.

If $\mathbf{M}_1$ tries to go **OFF** (***i.e.*** *reduce its drain current to very low levels*), $\mathbf{R}_{13}$ will receive a very low current; thus $\mathbf{V}_{G15}$ is pulled towards $\mathbf{V}_{ss}$ (*note that for low currents of* $M_1$, $V_{G14}$ *will be much larger; thus it is practically* ***OFF***). Then, $M_{15}$ will receive all of the current $\mathbf{2I}_{REF}$ . Thus, $\mathbf{V}_{S15}$ will be controlled by ***only*** $\mathbf{V}_{G15}$ (***i.e.*** by the *small* current of $M_1$). In this way, The drop in $\mathbf{V}_{G15}$ will in turn reduce $\mathbf{V}_{S15}$ and that will – *via the differential amplifier* $\boldsymbol{M_{16}}$-$\boldsymbol{M_{17}}$ – increase $\mathbf{V}_{G2}$ and reduce $\mathbf{V}_{G1}$ . These supply an extra $\mathbf{I}_{MIN}$ current left behind from the net output current. Thus, the minimum current never becomes zero. When $\mathbf{M}_2$ tries to go **OFF** an opposite similar process keeps its drain value equal or above $\mathbf{I}_{MIN}$ .

The above $\mathbf{I}_{MIN}$ expression, however, requires additional care to be understood in detail.

Below, another very similar ***class-AB*** output stage, based on the ***feedback*** *approach*, is given. Here, $\mathbf{R}_{12}$ and $\mathbf{R}_{13}$ receive not only






copies of the drain currents of $\mathbf{M}_2$ and $\mathbf{M}_1$ but also those of $\mathbf{M}_{14}$ and $\mathbf{M}_{15}$ , respectively.

Two different current references are used in this circuit; namely, $\mathbf{I}_{REF}$ and $\mathbf{I}_{REF2}$.

The feedback will try to achieve $\mathbf{V}_{G16}=\mathbf{V}_{G17}$ . Assuming $\mathbf{R}_{12}$-$\mathbf{R}_{13}$-$\mathbf{R}_{18}$ and $\mathbf{M}_{14}$-$\mathbf{M}_{15}$-$\mathbf{M}_{18}$ matched, we find that, for quiescent conditions, (*when* $\boldsymbol{I_{OUT}=0A \rightarrow I_1=I_2=I_Q}$) the equality $\mathbf{I}_{R13}=\mathbf{I}_{R12}$ , thus $\mathbf{V}_{S15}=\mathbf{V}_{S14}$ will be satisfied. This yields $\mathbf{I}_{D15}=\mathbf{I}_{D14}=\mathbf{I}_{REF2}$ (*since* $\boldsymbol{V_{G15}=V_{G14}}$ *as a result of connection*). Assuming $\mathbf{M}_1$-$\mathbf{M}_{11}$ and $\mathbf{M}_2$-$\mathbf{M}_{12}$ matched, we obtain

$$\mathbf{V_{GS18} + I_{REF}R_{18} = V_{GS15} + (I_{REF2} + I_Q)R_{13}}$$

Then we obtain $\mathbf{I_Q}$ as

$$\mathbf{I_Q = I_{REF} - I_{REF2} + (V_{GS18} - V_{GS15})/R_{13}}$$

$\mathbf{I_{REF}}$ is usually chosen slightly larger than $\mathbf{I_{REF2}}$ to supply a small $\mathbf{I_Q}$ . Therefore, typically $\mathbf{V_{GS18} - V_{GS15}}$ is very small. Thus, $\mathbf{I_Q = I_{REF} - I_{REF2}}$ is obtained. Obtaining $\mathbf{I_Q}$ as a difference of two currents makes design more flexible.

Usually, $\beta_{11}/\beta_1$ and $\beta_{12}/\beta_2$ are chosen less than **1** to avoid large currents flowing along the control circuitry in large signal conditions. Therefore, more generalized expressions for $\mathbf{I_Q}$ and $\mathbf{I_{MIN}}$ are given below.

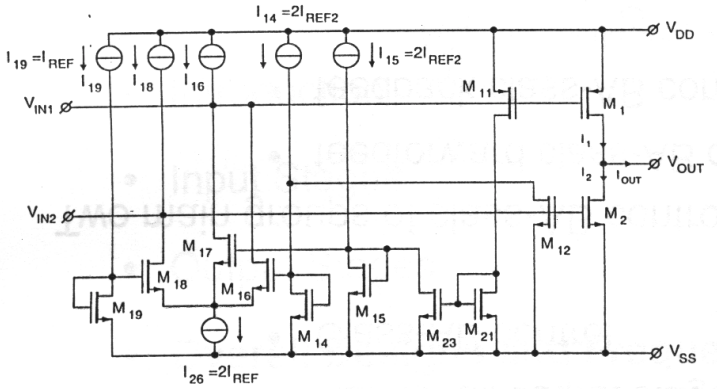
$$I_q = \frac{W_1}{L_1}\frac{L_{11}}{W_{11}}(I_{REF} - I_{REF2})$$

$$I_{min} = I_q\left(1 - \frac{I_{REF2}}{I_{REF} - I_{REF2}} - \frac{\sqrt{2}-1}{(I_{REF} - I_{REF2})R_{12}}\left(\sqrt{\frac{2I_{REF}L_{14}}{\mu_n C_{ox} W_{14}}}\right)\right)$$



Avoiding the drain currents of $M_1$ and $M_2$ from being zero for large signal conditions is achieved similarly as the previous circuit. Depending on which output transistor is starting to go **OFF**, the voltage $\mathbf{V_{G16}}$ is modulated to supply an opposite move to regulate the drain current of that output transistor at a minimum value.

The resistors may be a problem, for example in area consumption point of view. Therefore, an ***all-MOS*** structure like the one on the right would be appreciated. The operation is slightly different but the main principle is same as the two circuits explained above.




The quiescent and minimum currents for this output stage are

$$I_q = \frac{W_1}{L_1}\frac{L_{11}}{W_{11}}(2I_{REF2} - I_{REF})$$

$$I_{min} = I_q\left(1 - \frac{I_{REF}}{2I_{REF2} - I_{REF}}\left(2(\sqrt{2}-1)\sqrt{\frac{W_{19}L_{18}}{L_{19}W_{18}}} + (3-2\sqrt{2})\frac{W_{19}L_{18}}{L_{19}W_{18}}\right)\right)$$

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These examples are enough for the "***class-AB output stages***"

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