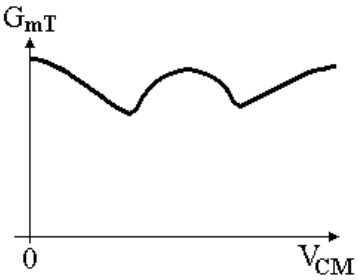
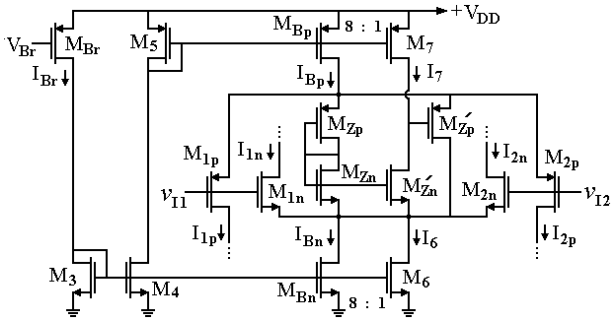
The maximum relative $\mathbf{G_{mT}}$ deviation is worse than that of a current-based method. However, the relatively lower power consumption is still an important advantage.

Typical value of maximum relative $\mathbf{G_{mT}}$ error is **20%**. Sharpening the ON-OFF transition is a must.

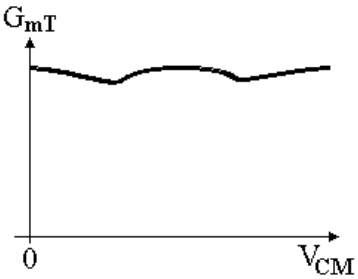


In the circuit on the right, additional devices are used (*but power consumption increases only marginally*) to obtain a better "Zener diode".

A maximum $\mathbf{G_{mT}}$ error less than **10%** is easily achievable.



With help of the added current sources and transistors, the ***V_{CM}-dependent*** "*current sharing* uncertainty" between the "Zener" and the input pairs has been dominantly prevented. In this new version, the "Zener" receives constant current when both input pairs are ON. Then the result is as shown on the right.



Insert voltage level shift between inputs of *p* and *n* pairs :

Two different techniques can be supplied under this classification:

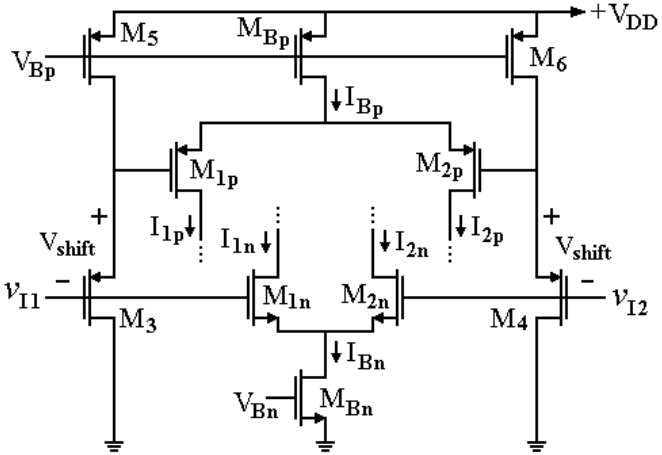
- DC level shifting
- Dynamic level shifting (*particularly for very low supplies; **e.g.** V_{DD}~1V*)

DC level shifting inserts a constant voltage between the inputs of ***p*** and ***n*** pairs, so as to get rid of the "**both pairs ON**" region to obtain a *rail-to-rail* constant $\mathbf{G_{mT}}$ (*obviously, it relies on β_n- β_p matching*).

A simple realization is supplied on the right.

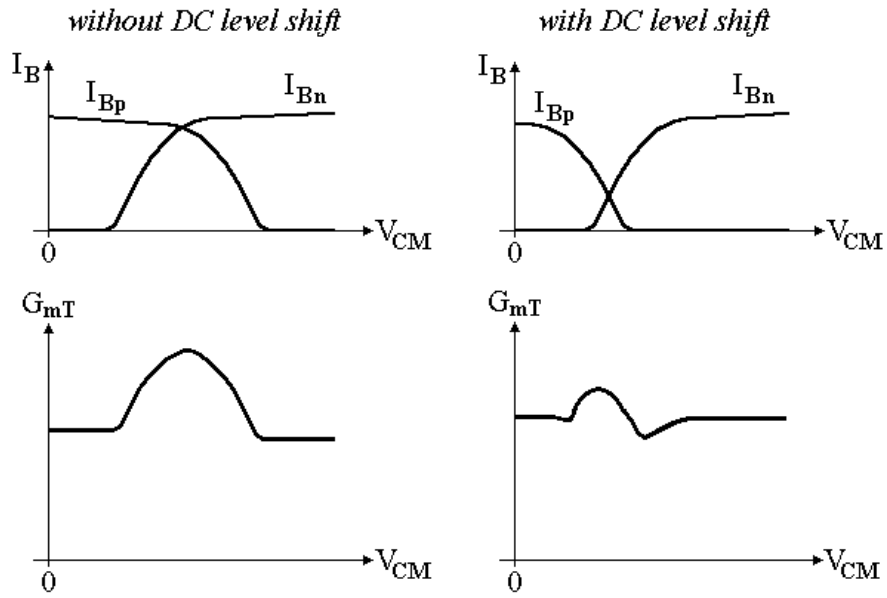
The source followers $\mathbf{M_3}$-$\mathbf{M_5}$ and $\mathbf{M_4}$-$\mathbf{M_6}$ supply the required DC level shift.

The design must be made such that $\beta_n=\beta_p$ and $\mathbf{V_{shift}}$ takes the proper value so as to obtain a $\mathbf{G_{mT}}$ curve as flat as possible along the input CM range.



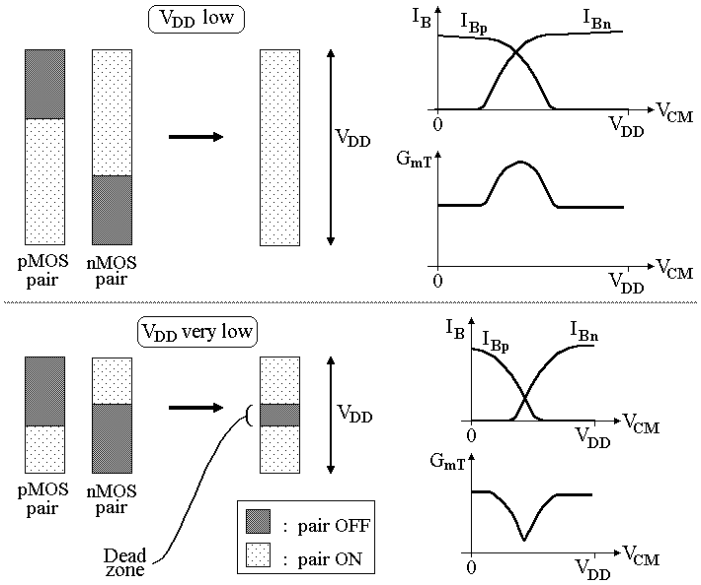
Typically, a maximum $\mathbf{G_{mT}}$ error less than **15%** can be achieved.

Below, to avail comparison, curves for tail currents of **p** and **n** pairs and corresponding $\mathbf{G_{mT}}$ are supplied for $\mathbf{V_{shift}}$**= 0** and $\mathbf{V_{shift}}$**=** $\mathbf{V_{shift,opt}}$.



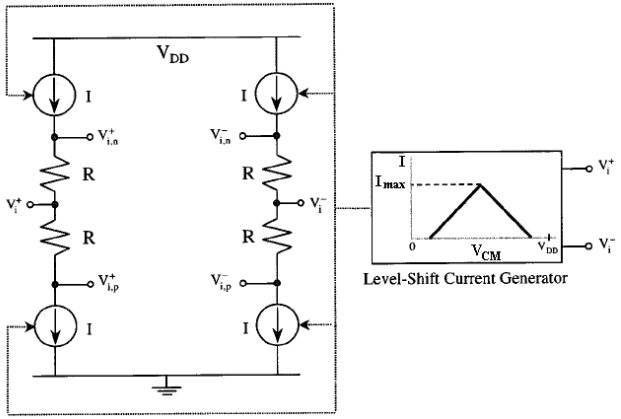
Dynamic level shifting inserts a *dynamic* voltage (*changed in accordance with the CM input voltage level*) between the inputs of ***p*** and ***n*** pairs. This is done so as to avoid the "**dead zone**" wherein **both pairs are OFF** (*this occurs for very low* V_{DD} *values;* ***e.g.*** **1V**).

In this way, a *rail-to-rail* constant G_{mT} can be obtained, provided that the voltage shift is properly adjusted along the CM range and $\beta_n=\beta_p$ equality is achieved.



So as to prevent the dead zone, a nonlinear circuit (*the square box*) is used, generating a current ***I*** as a function of the input CM voltage, as shown in the square box itself.

The generated current reaches its maximum value (I_{max}) for the middle of the input CM range and decreases down to **zero** when V_{CM} is close to V_{DD} or **GND**.



The value of I_{max} coincides with the nominal value of the tail currents I_{Bn} and I_{Bp} of the ***n*** and ***p*** pairs, which are chosen equal. Four replicas of the current ***I*** are applied to two identical pairs of passive level-shift resistors. The output terminals of this circuit will feed the inputs of the ***n*** and ***p*** pairs, such that, $V_{i,n}^{+}$ and $V_{i,n}^{-}$ are the input voltages of the ***n*** pair, whereas $V_{i,p}^{+}$ and $V_{i,p}^{-}$ are the input voltages of the ***p*** pair.

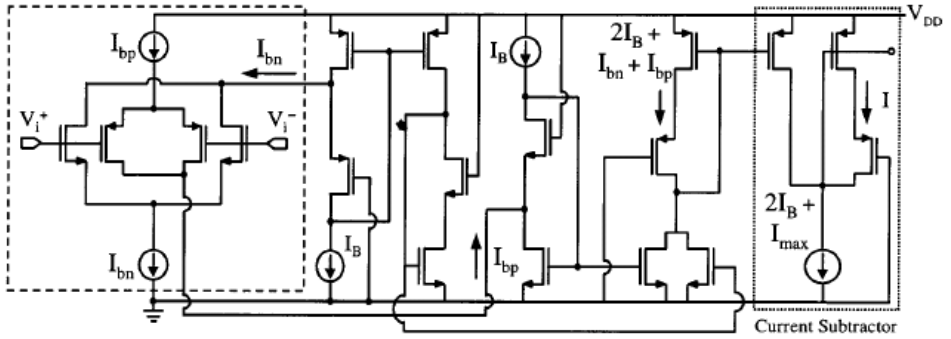
The common mode input voltages of the ***n*** and ***p*** pairs can be given in terms of the main input common mode voltage V_{CM}, as follows.

$$V_{CM,n} = V_{CM} + I\,R \quad , \quad V_{CM,p} = V_{CM} - I\,R$$

When V_{CM} is close to V_{DD} or **GND** (actually meaning, "*when one of the pairs is able to operate properly without any help*"), **I** is set zero (*notice that*, for **I=0**, $V_{CM,n}= V_{CM,p}= V_{CM}$); thus the circuit will function just like a conventional *rail-to-rail* input stage, with equal tail currents - *at their nominal values*.

As long as the **I** current sources and **R** resistors are matched, main input terminal currents will be **zero**. Thus, the input impedance will be very high ☺. However, in practice, mismatches will degrade the input impedance ☹, but only to tolerable levels ☺.

For the generation of the nonlinear level-shifting current, the circuit given below is used. A replica of the complementary input pairs is used (*enclosed by the dashed line – on the left*) for sensing the input CM voltage. The drain nodes of the transistors in each pair are connected together; thus, in this circuit, I_{Bn} and I_{Bp} are replicas of the nominal bias current I_B.

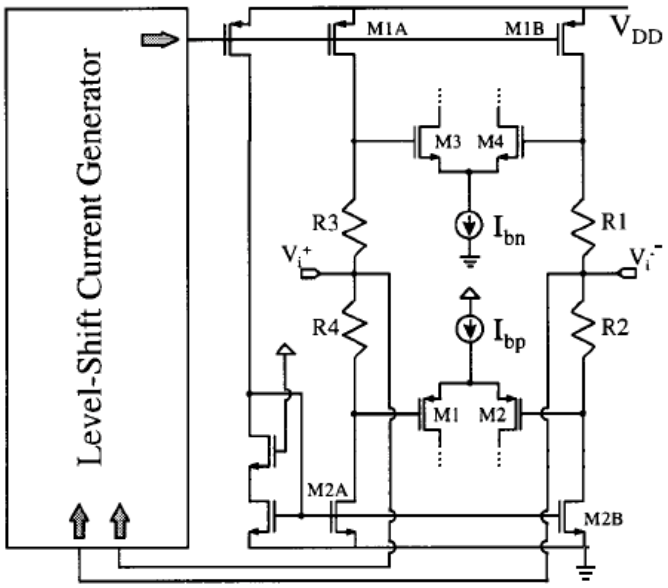


After appropriate mirroring of I_{Bn} and I_{Bp} with LV current mirrors biased with I_B, the sum of I_{Bn} and I_{Bp} is subtracted from I_{max} in the ***current subtractor*** circuit (*enclosed by dotted line - on the right*). The following nonlinear operation is performed by the current subtractor:

$$I = I_{max} - (I_{Bn} + I_{Bp}) \quad , \quad when \;\; I_{Bn} + I_{Bp} < I_{max}$$

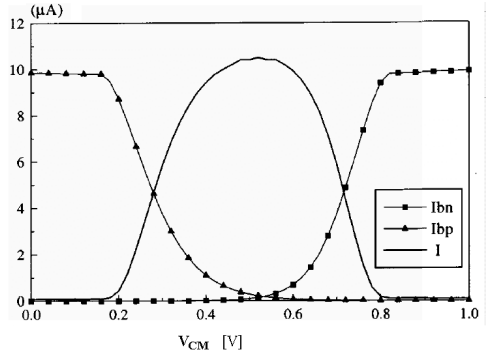
$$I = 0 \quad , \quad when \;\; I_{Bn} + I_{Bp} > I_{max}$$

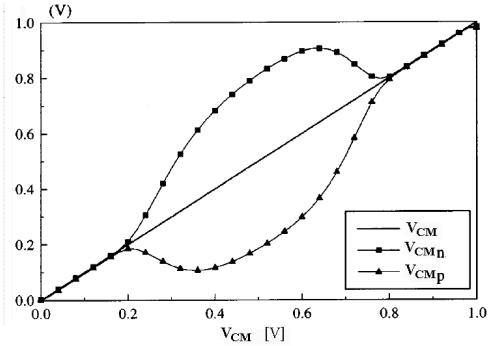
The final structure of the *rail-to-rail* constant-G_m input stage is given on the right.



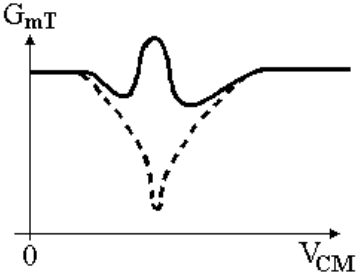
As $\mathbf{V_{CM}}$ changes from rail to rail, typical variations of the currents $\mathbf{I_{Bn}}$, $\mathbf{I_{Bp}}$, $\mathbf{I}$ and the voltages $\mathbf{V_{CMn}}$, $\mathbf{V_{CMp}}$ are as supplied in the figures below.

As can be observed, close to the rails, the circuit behaves like a primitive *rail-to-rail* input stage, wheras, when $\mathbf{V_{CM}}$ is in the middle of the rails, the ***n*** and ***p*** pairs are pushed apart, towards $\mathbf{V_{DD}}$ and **GND**, respectively.





Consequently, the typical nature of the $\mathbf{G_{mT}}$ curve is as given on the right (for **2** cases: ***solid curve :*** method is applied. ***dashed curve:*** method not applied).



Practically, a maximum relative $\mathbf{G_{mT}}$ error less than **15%** is achievable (*Additionally, a* ***tuning*** *can be performed to increase the performance*).

References used for the *"constant-G_m rail-to-rail input stages"* **section**

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- Yan, S. and Sanchez-Sinencio, E., "Low voltage analog circuit design techniques: A Tutorial," IEICE Trans. Analog Integrated Circuits and Systems, vol.E00 –A, no.2, pp.1-17, 2000.
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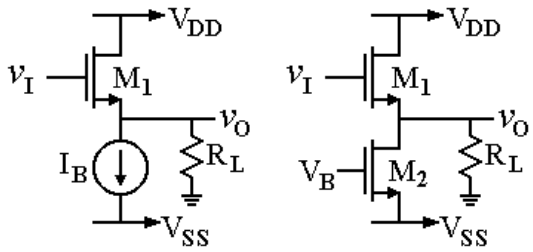
Rail-to-rail output stages

The output stage of an opamp is very important. It must be able to drive the load without degrading the important performance characteristics of the opamp.

For low voltage operation, on the other hand, voltage swing range at the output node is expected to be **rail-to-rail** – *once again*.



The **source follower** is a very good choice as the output stage of an opamp, especially for its low output impedance level. Unfortunately, the voltage swing is limited by at least **1** $\mathbf{V_{GS}}$ with respect to one of the rails (*wrt* $\mathbf{V_{DD}}$ for an ***nMOS*** source follower). Furthermore, the body effect causes the $\mathbf{V_{GS}}$ drop om M_1 be even larger as v_I tends to $\mathbf{V_{DD}}$. For these reasons, in ***LV*** design, the **source follower** is not preferred as an output stage.