Multi-stage amplifier compensation techniques *for very low-voltage operational amplifers*

- Operational amplifiers must supply a large enough gain for achieving high precision in linear (*negative feedback*) applications.
- At the same time, the speed must be high enough; in other words, the a large bandwidth is desired (**i.e.** *a large enough gain bandwidth product :* ***GB***).
- The stability of the opamp (*when connected in local feedback configuration*) must also be guaranteed for the worst type of feedback (*this is usually the* ***unity-gain*** *configuration*)

Single- or *two-stage* amplifiers (*usually bringing* ***not*** *more than* ***2*** *effective poles*) can be kept stable by applying simple techniques; the most complex one being the "**Miller compensation technique**". Therefore, using one or two gain stages is usually preferred for keeping the design simple. (**Note:** *the "effective" poles are those appearing dominantly in the open-loop transfer function. The remaining "far-away" poles/zeros which are due to negligible effects are usually not considered, - ! ! ! they can modify the phase margin by a few degrees though ! ! !)*

Unfortunately, simple gain stages (***e.g.*** *common source stage*) cannot supply sufficient voltage gain (*When using MOSFETs as active devices, this becomes even worse* ☹). Nevertheless, by using **cascoding** and/or **gain boosting** (*regulated cascode*), it is possible to obtain a large gain from a single stage ☺, *but this costs a lot of voltage headroom* ☹.

It is possible to use the ***vertical*** connections (***e.g.*** *cascoding*) for $\mathbf{V_{DD}}$ values down to, *for example*, **2V** ; however, as $\mathbf{V_{DD}}$ tends to lower values, cascoding and other ***vertical*** gain boosting techniques can ***no longer*** be applied. Then, ***horizontal*** connections (***cascading***) must be used.

When simple gain stages are *cascaded* in an opamp, more than two stages (*typically,* ***three*** *or* ***four***) must be used so as to obtain a large enough open-loop gain. However, in this case, the number of effective poles in the open-loop transfer function will be increased (*typically, to* ***3*** *or* ***4***) making the compensation process very complicated ☹. Therefore, several compensation techniques have been proposed to simplify the compensation of multi-stage low-voltage operational amplifiers.

There exist **3** dominant approaches for multi-stage amplifier compensation:

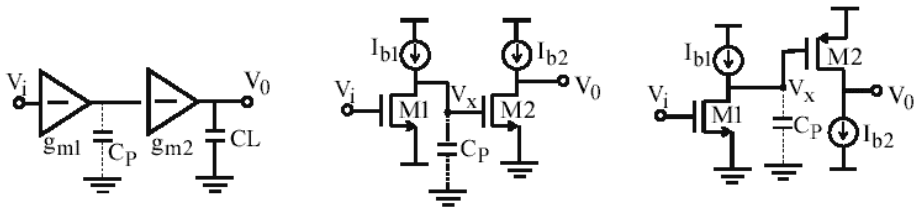
- Nested Miller Compensation (**NMC**)
- Multi-path Nested Miller Compensation (**MNMC**)
- Nested $\mathbf{G_m}$**-C** Compensation (**NGCC**)

Before starting to explain these approaches, it will be helpful revisiting the *conventional Miller compensation technique*.

Miller compensation

A 2-stage amplifier can be compensated by connecting a capacitor across the output and input of nodes of the second -inverting- amplifier.

Without compensation, a generalized view of the amplifier is given in **(a)** in the figure below (the gains are *naturally* negative, since the best amplifier stage supplying a large gain with a large input impedance level is the common source stage – *with a negative gain*). In **(b)** and **(c)**, two possible transistor-level realizations are supplied (+ *parasitics*).



(a) (b) (c)

Such an amplifier will supply a **DC** (*low-frequency*) gain of

$$\mathbf{H(0)=g_{m1}r_{o1}g_{m2}r_{o2}}$$

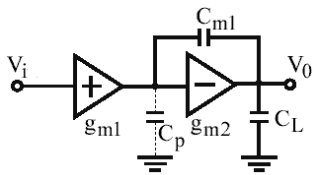
Assuming the input voltage source ideal, typically, two poles will be coming; one due to $\mathbf{C_p}$ and the other due to $\mathbf{C_L}$ (☝ *This must include both the capacitive load and the parasitic output capacitance*):

$$\omega_{p1}=1/(r_{o1}C_p) \quad , \quad \omega_{p2}=1/(r_{o2}C_L)$$

It is well-known that, so as to obtain a large enough phase margin (***e.g.*** **60°**), the ***non-dominant*** (the much larger) pole must be located after (*must be larger than*) the unity-gain frequency (*if this is satisfied, the* ***unity-gain frequency*** *and the* ***GB*** *become equal*).

Very typically, this condition does not hold *naturally*, therefore, one of the poles is *artificially* made **dominant** by increasing the node capacitance corresponding to that pole, such that the unity-gain frequency comes before the second (*non-dominant*) pole.

- The simplest method to make a pole **dominant** is, to connect a capacitor between the corresponding node and ground (*or AC ground*). However, usually a **large** capacitor value is required for most of the cases, in turn increasing the consumed chip area ☹ (*nevertheless, this method is used for some applications*).
- The "Miller multiplication" idea can be used to obtain large capacitance values (***in effect***) while using tolerable capacitance values. This is simply done by connecting the artificial capacitor in between the input and output of a *negative-gain* amplifier. It is obvious that, for a *2-stage* amplifier, this can be apllied to the second amplifier (*see the figure*); thus the first pole ω_{p1} will be made dominant (it can be shown that ω_{p2} will be moving even further ☺).



It is obvious that, so as to bew able to use this method, the second stage must be an ***inverting-type*** amplifier. The sign of the gain of the first stage does not have an effect (*a positive-gain amplifier is used since the multi-stage compensation requires this. ... will be clear shortly*).

Without any compensation, the transfer function of the given *2-stage* amplifier will be,

$$H(s)=\frac{V_0(s)}{V_i(s)}\cong\frac{H(0)\,\omega_{p1}\,\omega_{p2}}{(s+\omega_{p1})(s+\omega_{p2})}=\frac{+\dfrac{g_{m1}g_{m2}}{C_pC_L}}{s^2+s\left(\dfrac{g_{01}}{C_p}+\dfrac{g_{02}}{C_L}\right)+\dfrac{g_{01}g_{02}}{C_pC_L}}$$

where $\mathbf{g_{o1}=1/r_{o1}}$ and $\mathbf{g_{o2}=1/r_{o2}}$.

On the other hand, for the 2-stage amplifier using a Miller compensation capacitor $\mathbf{C_{m1}}$, an additional capacitive contribution of value $\mathbf{(|A_{V02}|+1)C_{m1}}$ will come in parallel to $\mathbf{C_p}$, where, $\mathbf{|A_{V02}|=g_{m2}r_{o2}}$ is the absolute value of the *low-freq.* voltage gain of the second stage. (*Typically, this contribution dominates; thus C_p can be omitted in remaining analyses. On the other hand, the contribution of C_{m1} to*

the output node capacitance is approximately C_{m1} , typically small enough with respect to C_L)

Using a thorough analysis, it can be shown that the transfer transfer function for the compensated 2-stage amplifier is

$$H(s)=\frac{g_{m1}(g_{m2}-sC_{m1})/C_LC_{m1}}{s^2+s\left(g_{01}(C_L+C_{m1})/C_LC_p+g_{m2}/C_L+g_{02}/C_L\right)+g_{01}g_{02}/C_LC_{m1}}$$

Note that the **DC gain** remains unchanged (*the sign of the gain discarded for brevity*) The new locations of the poles are

$$\omega_{p_1}\cong\left(\frac{g_{01}}{C_{m1}}\right)\frac{g_{02}}{g_{m2}}=\left(\frac{g_{01}}{C_{m1}}\right)\frac{1}{A_{V_{02}}}\qquad,\qquad\omega_{p_2}\cong(g_{m2}+g_{02})/C_L$$

It is obvious that ω_{p1} has been pushed to much lower frequencies (*made dominant*), whereas ω_{p2} is pushed to higher frequencies with respect to their original locations. This is called "pole splitting".

Unforunately, a *real* zero ($\omega_z=-g_{m2}C_{m1}$) is formed on the ***right half plane*** of the s-plane ☹. This may be a problem (*precautions needed*).

- Usually a resistor is used in series with $\mathbf{C_{m1}}$ to force the zero to the *left half plane*. It is also possible to coincide this zero with the *non-dominant* pole ω_{p2} so as to improve the phase margin further.

The effect of the zero can be explained with a *physical* point of view:

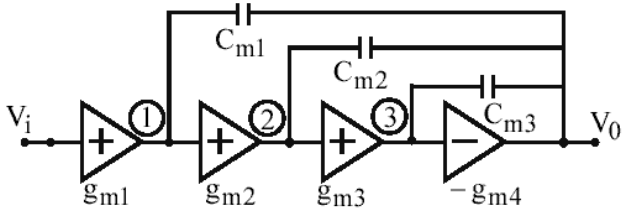
As frequency increases, the mentioned zero inverts the gain (*change the phase of the gain by **–180°***). This is because the compensation capacitor is forming a *feedforward path,* eventually becoming **short-circuit** for high frequencies to form a direct path from the input of the second stage to the output.

- An alternative method to prevent the effect of the zero is to use a buffer between the output node and $\mathbf{C_{m1}}$ to supply a **one-way** (*feedback-only*) path along $\mathbf{C_{m1}}$.
- A third method is based on addition of a *feedforward* amplifier (*This will be analysed when we explain the "Nested G_m-C Compensation" method*).

→ *Now, we can explain the multi-stage amplifier compensation methods.*

Nested Miller Compensation (NMC)

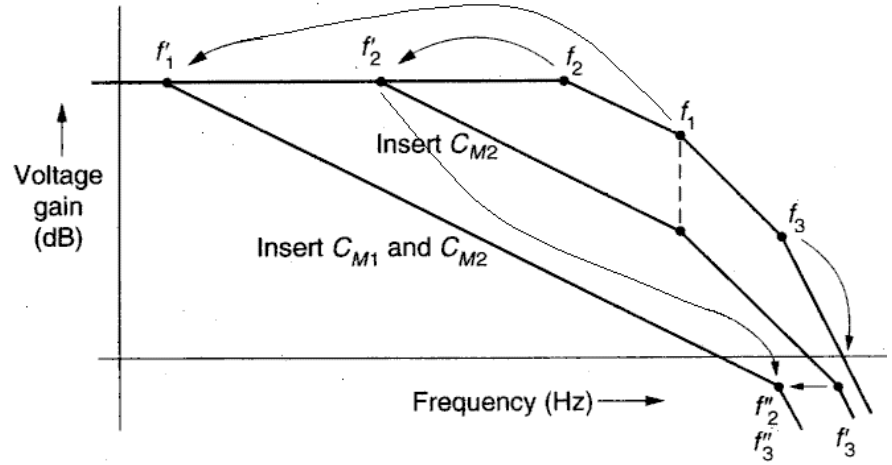
The main idea in this compensation approach is that, "**at the each new step of compensation, an *already-compensated* two-stage amplifier can be treated as an ordinary single-stage amplifier**". In this way, starting from the last two stages, the whole system is step-by-step compensated by applying the Miller compensation in a ***nested*** fashion, as shown in the figure below, where a 4-pole system is compensated with three capacitors.



By connecting $\mathbf{C_{m3}}$, A ***local*** dominant pole (f_{p3}) is created at node **3** for the amplifier formed by $\mathbf{g_{m3}}$ and $\mathbf{-g_{m4}}$. Thus, down to its own *unity-gain frequency*, this 2-stage amplifier will behave like a ***single-pole*** system. Then, connecting $\mathbf{C_{m2}}$ will achieve *pole splitting* for the poles $\mathbf{f_{p2}}$ and $\mathbf{f_{p3}}$, such that $\mathbf{f_{p2}}$ and $\mathbf{f_{p3}}$ will take smaller and larger values, respectively,

with respect to their last values. Eventually, with help of connecting $\mathbf{C_{m1}}$ the pole at node **1** (f_{p1}) will be the dominant pole.

The typical *evolution* of the pole frequency locations (*for a **3-stage** amplifier to which **NMC** is applied*) while the compensation capacitors are being connected, is depicted by the Bode plot below.



As a rule of thumb, at each compensation step (*connection of a new compensation capacitor*) the new non-dominant pole must be ***buried*** at least 3dB below the 0dB level to achieve a good phase margin and for *this* non-dominant pole as not to be affected badly (not to be driven *complex*) by the next compensation step. This approach, however, in turn degrades the final overall **GB** value (*this is also apparent from the above Bode plot*).

Generalizing the scheme to an N-stage amplifier, it can be shown that, the above approach for obtaining a good phase margin requires the following conditions to be satisfied:

$$\mathbf{g_{m(i)}/C_{m(i)} \bullet \tfrac{1}{2}\, g_{m(i+1)}/C_{m(i+1)}} \quad , \quad \mathbf{i} = 1,\ldots,N\text{-}1$$

$$\mathbf{g_{m(N)} >> g_{m(i)}} \quad , \quad \mathbf{i} = 1,\ldots,N\text{-}1$$

In this way, the non-dominant poles can be approximated by

$$\omega_{p(i)} = \mathbf{g_{m(i)}/C_{m(i)}} \qquad \mathbf{i} = 2,\ldots,N$$

If the above conditions were not satisfied, the calculation of the non-dominant poles would be rather complex.

It is no doubt that, the dominant pole will come from the first node. Assuming a four-stage amplifier, it can be approximated as,

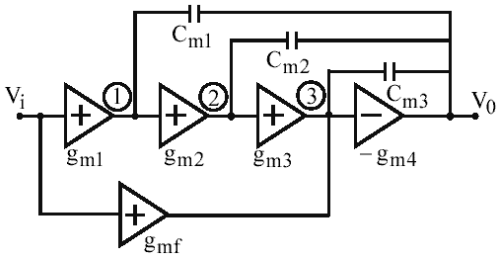
$$\omega_{p1} = \mathbf{g_{o1}g_{o2}g_{o3}g_{o4}/(C_{m1}g_{m2}g_{m3}g_{m4})}$$

This pole must be at low enough frequencies, such that the Bode plot drop with **–20dB/dec** down to the unity-gain frequency.

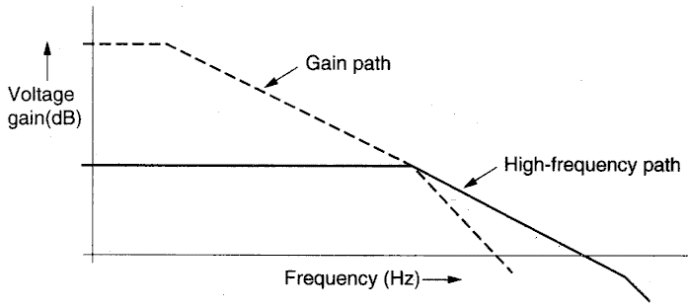
The effort to *bury* each non-dominant pole 3dB below the 0dB level is requireds to make sure that the next step *does not affect/is not affected by* these previous non-dominant poles badly, as far as possible. Using an independent *feedforward* amplifier can solve this problem. ☺

Multi-path Nested Miller Compensation (MNMC)

The **MNMC** adds an independent parallel input stage to transform the **NMC** structure to the **MNMC** structure, as shown in the figure. At low frequencies, the gain stages formed by $\mathbf{g_{m1}}$, $\mathbf{g_{m2}}$ and $\mathbf{g_{m3}}$ dominate from the



input to the node **3**, wheras, for high frequencies (*when the compensation capacitors C_{m1} and C_{m2} reduce the overall gain of the 3-stage amplifier g_{m1}-g_{m2}-g_{m3}*), the feedforward amplifier g_{mf} supplies the dominant signal path from the input to node **3**. Thus, the overall system behaves similar to a typical *miller compensated 2-stage amplifier* (*formed by g_{mf} , $-g_{m4}$ and C_{m3}*). If design is made properly, then a Bode plot like the one given on the right is achievable. (*the plot is for a* 3-stage ***MNMC*** *amplifier*)



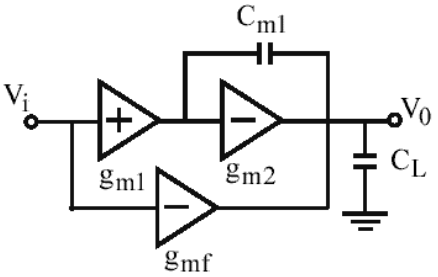
It is obvious that, in this case, the **GB** degradation is almost fully prevented. It can be shown that, so as to achieve this improvement, we must choose g_{m2} as low as possible. Unfortunately, the feedforward path inserts a zero to the transfer function ☺;

nevertheless, this zero can be coincided with one of the non-dominant poles if g_{m3}/C_{m2} and g_{m4}/C_{m1} are set **equal**. That is, matching g_{m3} with g_{m4} and C_{m2} with C_{m1} will be sufficient (*fortunately, this is not a hard work when we are designing an integrated circuit* ☺).

Nested G_m-C Compensation (NGCC)

Recall that we had mentioned (*but postponed the explanation of*) a ***third*** method for conventional Miller compensation so as to aviod the *right-half-plane* zero. The startpoint of **NGCC** approach is that method; therefore we'd better exame that first.

The alternative method to avoid the zero in a Miller compensated 2-stage amplifier is to use an *inverting* feedforward amplifier from the input to the node which forms the dominant pole. The method is visualized in the figure on the right. If g_{mf} is chosen equal to g_{m1} , the

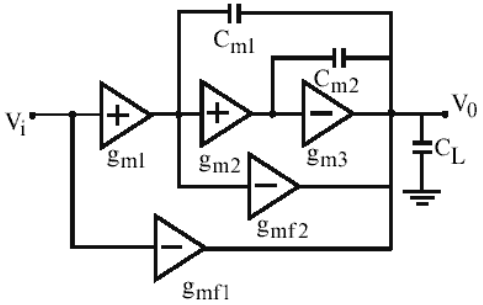


transfer function is obtained with a simple form as

$$H(s)\Big|_{g_{mf}=g_{m1}} = \frac{-g_{m1}g_{m2}}{s^2C_{m1}C_L + sC_{m1}g_{m2} + g_{01}g_{02}}$$

It is obvious that there exists no zero in the transfer function ☺.

Using this structure as a core, it is much easier and more efficient to apply a ***nested*** compensation procedure. The concept is supplied in the figure on the right, where a *3-stage* **NGCC** amplifier is shown. For this amplifier, setting $g_{mf1}=g_{m1}$ and $g_{mf2}= g_{m2}$ is sufficient to avoid the zero(s). When a general case is considered, the overall transfer function is



$$H(s) = -\frac{g_{m1}g_{m2}g_{m3} + sg_{m1}(g_{mf2}-g_{m2})C_{m2} + s^2(g_{mf1}-g_{m1})C_{m1}C_{m2}}{g_{o1}g_{o2}g_{o3} + sg_{m2}g_{m3}C_{m1} + s^2(g_{m3}+g_{mf2}-g_{m2})C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}}$$

So, it's obvious that setting $g_{mf1}=g_{m1}$ and $g_{mf2}= g_{m2}$ will yield the simplified form below.

$$H(s) = \frac{Vo(s)}{Vi(s)} = \frac{-g_{m1}g_{m2}g_{m3}}{g_{o1}g_{o2}g_{o3} + sg_{m2}g_{m3}C_{m1} + s^2g_{m3}C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}}$$

Thsi transfer function can be rewritten as

$$H(s) = \frac{-A_0}{\left(1+s\frac{A_0}{f_1}\right)\left(1+\frac{s}{f_2}+\frac{s^2}{f_2f_3}\right)}$$

where,

$$A_0 = \frac{g_{m1}g_{m3}g_{m2}}{g_{01}g_{03}g_{02}} \quad , \quad f_1 = GB = \frac{g_{m1}}{C_{m1}}$$

$$f_2 = \frac{g_{m2}}{C_{m2}} \; , \; f_2f_3 = \frac{g_{m2}g_{m3}}{C_{m2}C_L} \; ; \; f_i = \frac{g_{mi}}{C_{mi}}$$

The dominant pole, on the other hand, is

$$P_1 = \frac{f_1}{A_0} = \frac{\frac{g_{m1}}{C_{m1}}}{\frac{g_{m1}g_{m2}g_{m3}}{g_{01}g_{02}g_{03}}} = \frac{g_{01}g_{02}g_{03}}{g_{m2}g_{m3}C_{m1}} = \left(\frac{g_{01}}{C_{m1}}\right)\frac{1}{A_{V0_2}A_{V03}}$$

For a 4-stage NGCC amplifier, it can be shown that, the design is very easy, such that, for example guaranteeing $\mathbf{f_1<f_2< f_3<f_4}$ together with the condition

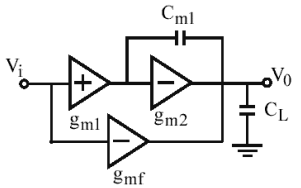
$$f_4 > \frac{f_2}{1-f_2/f_3}$$

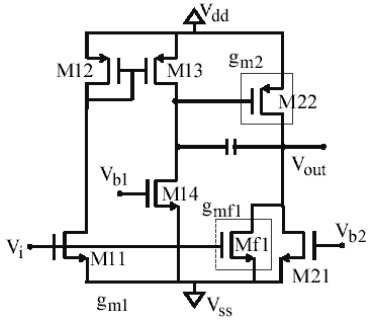
is sufficient for efficient application of the method. Note that, whatever the number cascaded stages is, the bandwidth is not reduced due to the applied nested compensation. ☺

Below is the generalized transfer function for an ***N-stage*** **NGCC** amplifier when $\mathbf{g_{mf(i)}=g_{m(i)}}$ (i=1...N-1) matchings are all satisfied.

$$H(s) = \frac{-\prod_{j=1}^{N} g_{mj}/g_{oj}}{\left(1+\frac{-\prod_{j=1}^{N} g_{mj}}{f_1}\right)\cdot\left(1+\frac{s}{f_2}+\frac{s^2}{f_2 f_3}+\ldots+\frac{s^{n-1}}{\prod_{i=2}^{N} f_i}\right)}$$

Below onthe left is the conceptual circuit and on the right is an implementation of a *2-stage* **NGCC** amplifer. (*Notice how the* ***positive*** g_m *is obtain by supplying a current inversion via the current mirror M12-M13*)





For concluding, a **4-stage NGCC operational amplifier** implementation is given below. The function of each block is clearly observed.