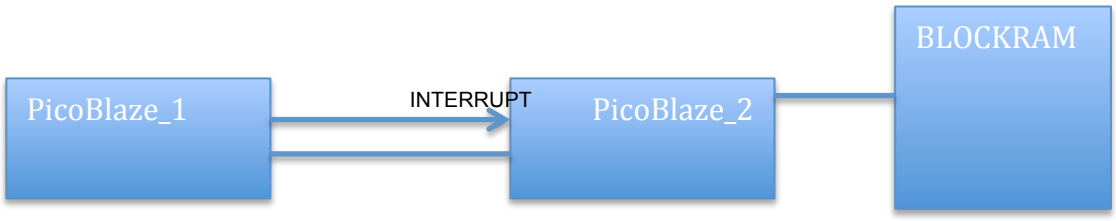
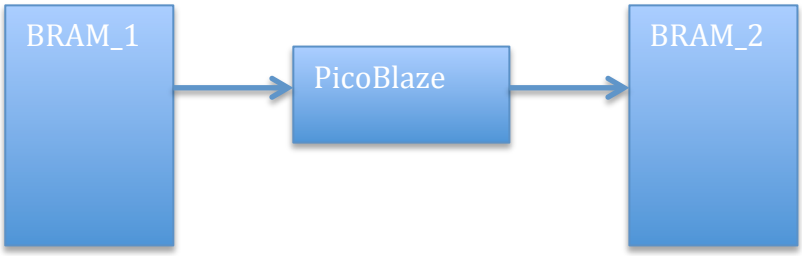
HOMEWORKS

1. Design the system given in Figure 1 that includes two PicoBlazes and a Block RAM. Data in Block RAM will be transfer to PicoBlaze_1 via PicoBlaze_2. PicoBlaze_1 initiates the data transfer, PicoBlaze_2 responds to the initiation request. PicoBlaze_1 uses a request line which is connected to interrupt port of PicoBlaze_2. When PicoBlaze_1 asserts the request line to initiate a transfer, PicoBlaze_2 puts the data where is in an arbitrary address. PicoBlaze_1 stores the data on its Scratchpad RAM.

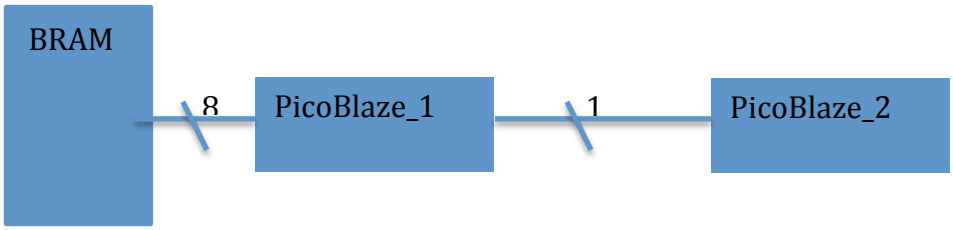


2. Design the system given in Figure 2 that includes two Block RAMs and a PicoBlaze. PicoBlaze transfers all the data in BRAM_1 to BRAM_2.

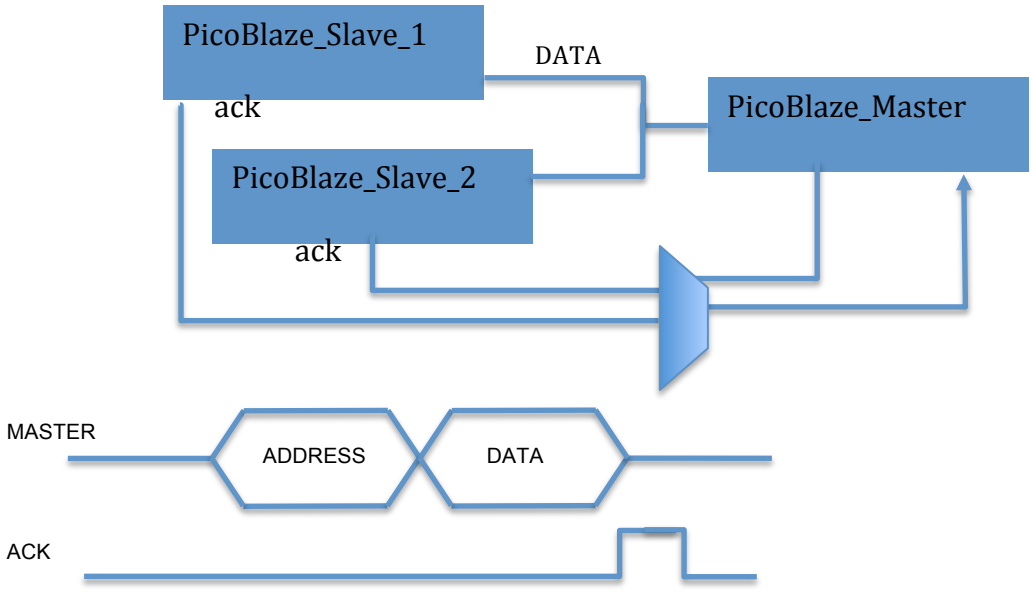


3. Design a system which includes a single BlockRAM and two PicoBlazes. A 6 x 6 matrix is stored in BRAM (0000h – 0024h). Even rows of the transpose of the matrix are computed and then stored to BRAM (0100h-010F) by PicoBlaze_1, odd rows are computed and stored to the same BRAM (0200h-020fh) by PicoBlaze_2.

4. Design a system with two PicoBlazes and a single BlockRam. PicoBlaze_1 is directly connected to the BlockRAM. PicoBlaze_1 reads the memory (64 byte, form arbitrary address) and then sends the data to PicoBlaze_2 via 1 bit line.

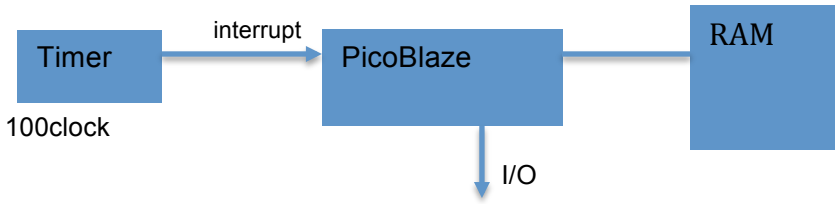


5. Design a system which has 3 PicoBlazes (one master (PicoBlaze_Master), two slaves (PicoBlaze_Slave_1 and PicoBlaze_Slave_2), each slave PicoBlaze is assigned an address. Timing diagram of communication is given, master puts address of slave PicoBlazer, then data on bus (8 bits). Slave asserts ack and master ready for next transmission.

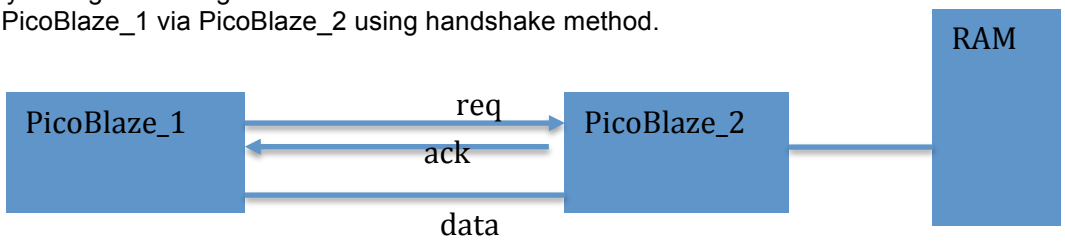


6. Desing a system which has two PicoBlazes that shares the same program memory. Each PicoBlaze connects a BlockRam. Each BlockRam has a sequence which is started from 0001h address and the sizes of sequences is written in 0000h address of the BlockRams. Each PicoBlaze finds the largest element in its memory and write to the end of the memory address.

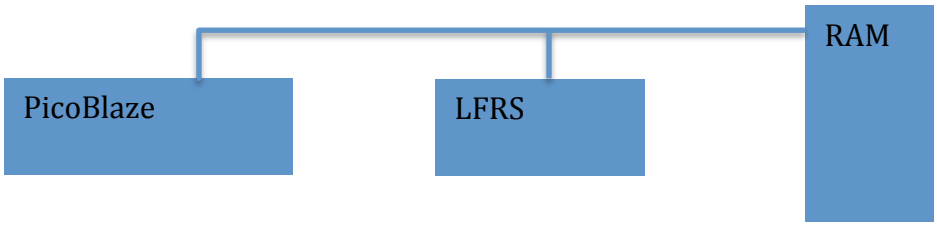
7. Design a system with 2 picoblazes which connect a dual port Block RAM. The system computes determent of a 3x3 matrix such that det [a b c; d e f; g l m]=a*det[e f;l m]-b*det[d f; g m]+c*det[d e; g l]. The matrix is read from RAM by the PicoBlazes and then a*det[e f;l m]-b*det[d f; g m] part of computation done by PicoBlazes_1 and c*det[d e; g l] is computed by PicoBlazes_2.
8. A timer generates an interrupt for a PicoBlaze after each 100-clock cycle and then the PicoBlaze reads data from a specified memory addressed and writes it to output port. After each interrupt, next memory address (+1) is saved. Meanwhile the main program of PicoBlaze is simple counting (i=i+1).



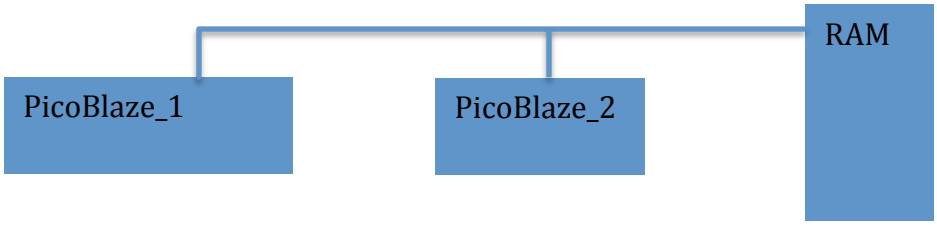
9. Design a system given in Figure 9 that includes two PicoBlazes and a Block RAM. Data in Block RAM will be transfer to PicoBlaze_1 via PicoBlaze_2 using handshake method.



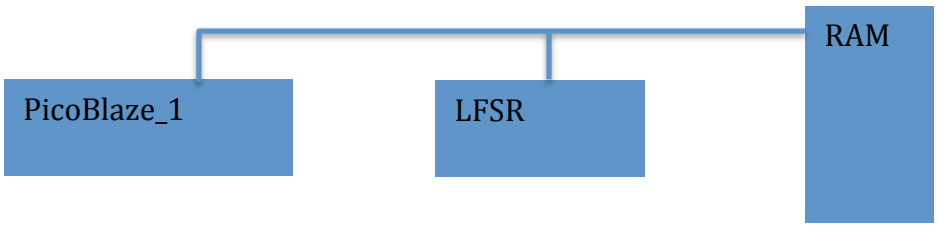
10. Design a system to implement Vernam cipher (http://www.cs.miami.edu/home/burt/learning/Csc609.051/notes/02.html) (one-time pad). Vernam proposed a bit-wise exclusive or of the message stream(m(i)) with a random stream (z(i)) which was shared by sender and receipient. PicoBlaze computes cipher text C(i)=m(i)EXORz(i) and writes back to memory. In this design, random stream z(i) is generated by linear feedback shift register (http://www.eng.auburn.edu/~strouce/class/elec6250/LFSRs.pdf) with characteristic polynomial x^8+x^6+x^5+x^4+1 (seed value z(0)=12h) and is read by Picoblaze to compute cipher text. The message is written in RAM.



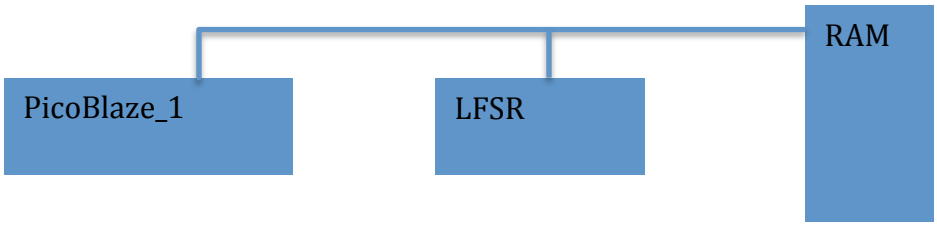
11. Design a system to implement Vernam cipher (http://www.cs.miami.edu/home/burt/learning/Csc609.051/notes/02.html) (one-time pad). Vernam proposed a bit-wise exclusive or of the message stream(m(i)) with a random stream (z(i)) which was shared by sender and receipient. PicoBlaze_1 computes cipher text C(i)=m(i)EXORz(i) and writes back to memory. In this design, random stream z(i) is generated by PicoBlaze_2 with characteristic polynomial x^8+x^6+x^5+x^4+1 (seed value z(0)=12h) and is read by Picoblaze_1 to compute cipher text. The message is written in RAM.



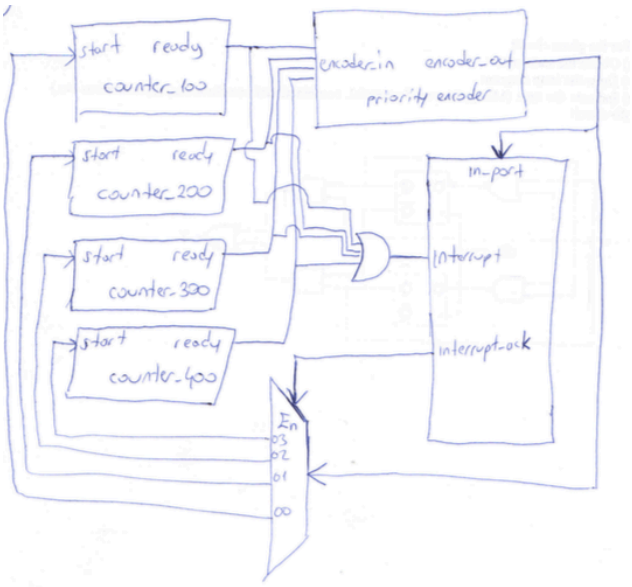
12. Design a system to implement a self-synchronizing stream cipher (http://cacr.uwaterloo.ca/hac/about/chap6.pdf) which is one in which the key-stream is generated as a function of the key and a fixed number of previous ciphertext digits. PicoBlaze read the message stream(m(i)) from the memory then computes ciphertext c(i)=m(i)EXORg(i). Linear feedback shift register (http://www.eng.auburn.edu/~strouce/class/elec6250/LFSRs.pdf) generates z(i) with characteristic polynomial x^8+x^6+x^5+x^4+1 using c(i-1) as seed value. Picoblaze computes keystream (g(i)) by g(i)=z(i)EXOR KEY. KEY is stored in Program memory which is the secret key.c(0)=12h is public key and is in the RAM.



13. Design a system to implement a self-synchronizing stream cipher (http://cacr.uwaterloo.ca/hac/about/chap6.pdf) which is one in which the key-stream is generated as a function of the key and a fixed number of previous ciphertext digits. PicoBlaze_1 read the message stream(m(i)) from the memory then computes ciphertext c(i)=m(i)EXORg(i). PicoBlaze_2 generates z(i) with characteristic polynomial x^8+x^6+x^5+x^4+1 using c(i-1) as seed value. Picoblaze_1 computes keystream (g(i)) by g(i)=z(i)EXOR KEY. KEY is stored in Program memory which is the secret key.c(0)=12h is public key and is in the RAM.



14. Design the system which is given in Figure



When interrupt is asserted, s1 register will give the counter number of interrupt in interrupt subroutine. When more than one interrupt is received, s1 register will give output of priority encoders. For priority_encoder.v and conter.v please contact eabtioglu@gmail.com