

Microprocessor System Design

EHB432E

Lecture -5

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Memory

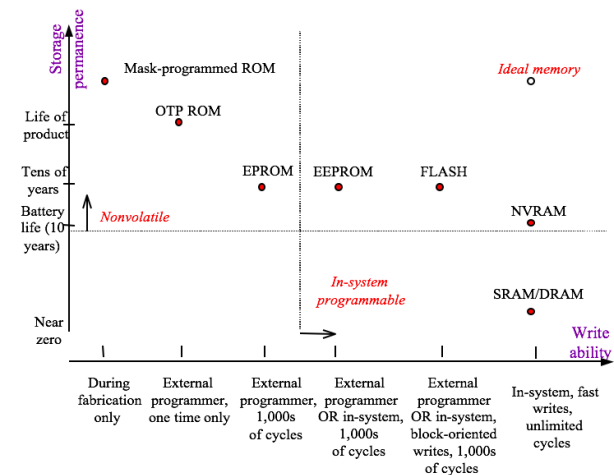
- Stores large number of bits
 - mxn : m words of n bits each
 - $k = \log_2(m)$ address input signals
 - or $m = 2^k$ words e.g., 4,096x8 memory: 32,768 bits, 12 address input signals, 8 input/output data signals
- Memory access
 - r/w: selects read or write
 - enable: read or write only when asserted
 - multiport: multiple accesses to different locations simultaneously

Memory

Write ability/ storage permanence

- Traditional ROM/RAM distinctions
 - ROM read only, bits stored without power
 - RAM read and write, lose stored bits without power
- Traditional distinctions blurred
 - Advanced ROMs can be written to e.g., EEPROM
 - Advanced RAMs can hold bits without power e.g., NVRAM
- Write ability
 - Manner and speed a memory can be written
- Storage permanence
 - ability of memory to hold stored bits after they are written

Memory



Memory

Ranges of write ability:

- High end [processor writes to memory simply and quickly, e.g., RAM]
- Middle range [processor writes to memory, but slower e.g., FLASH, EEPROM]
- Lower range [special equipment, "programmer", must be used to write to memory e.g., EPROM, OTP ROM]
- Low end [bits stored only during fabrication e.g., Mask-programmed ROM]

Range of storage permanence

- High end [essentially never loses bits e.g., mask-programmed ROM]
- Middle range [holds bits days, months, or years after memory's power source turned off e.g., NVRAM]
- Lower range [holds bits as long as power supplied to memory e.g., SRAM]
- Low end [begins to lose bits almost immediately after written e.g., DRAM]

Mask-programmed ROM

- Connections "programmed" at fabrication(mask)
- Lowest write ability (once)
- Highest storage permanence

OTP ROM: One-time programmable ROM

- Connections "programmed" after manufacture by user
- Very low write ability (typically written only once and requires ROM programmer device)
- Very high storage permanence
- Commonly used in final products

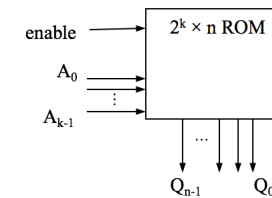
► Atmel: OTP EPROM

EPROM: Erasable programmable ROM

- Programmable component is a MOS transistor
- Better write ability (can be erased and reprogrammed thousands of times)
- Reduced storage permanence (program lasts about 10 years)
- Typically used during design development

ROM: "Read-Only" Memory

- Nonvolatile memory
- Can be read from but not written to, by a processor in an embedded system
- Traditionally written to, "programmed", before inserting to embedded system
- Uses
 - Store software program for general-purpose processor
 - Store constant data needed by system
 - Implement combinational circuit (BLG 231E Digital Circuits)



A *datasheet*, *data sheet*, or *spec* sheet is a document that summarizes the performance and other technical characteristics of a product, machine, component (e.g., an electronic component), material, a subsystem (e.g., a power supply) or software in sufficient detail to be used by a design engineer to integrate the component into a system. [► Wikipedia](#)

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

MICROCHIP **27C64**
64K (8K x 8) CMOS EPROM

FEATURES	PACKAGE TYPES
<ul style="list-style-type: none"> High speed performance <ul style="list-style-type: none"> 120 ns access time available CMOS Technology for low power consumption <ul style="list-style-type: none"> 20 mA Active current 100 μA Standby current Factory programming available <ul style="list-style-type: none"> Auto-insertion-compatible plastic packages Auto ID aids automated programming Separate chip enable and output enable controls High speed "express" programming algorithm Organized 8K x 8; JEDEC standard pinouts <ul style="list-style-type: none"> 28-pin Quad-in-line package 	<p>DIP/SOIC</p>



► Datasheet:27C64

EEPROM: Electrically erasable programmable ROM

- Programmed and erased electronically
 - typically by using higher than normal voltage
 - can program and erase individual words
- Better write ability
 - can be in-system programmable with built-in circuit to provide higher than normal voltage
 - writes very slow due to erasing and programming
 - can be erased and programmed tens of thousands of times
- Similar storage permanence to EPROM (about 10 years)
- Far more convenient than EPROMs, but more expensive

► Atmel EEPROMs

► Datasheet:Atmel AT28C010

► Datasheet:Atmel 24AA32A

Flash Memory

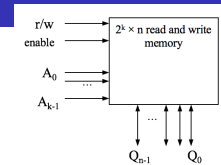
- Extension of EEPROM
 - Same gate principle, write ability and storage permanence
- Fast erase
 - Large blocks of memory erased at once, rather than one word at a time
Blocks typically several thousand bytes large
- Writes to single words may be slower
 - Entire block must be read, word updated, then entire block written back
- Used with embedded systems storing large data items in nonvolatile memory



► Toshiba: NAND Flash

► Datasheet:Atmel

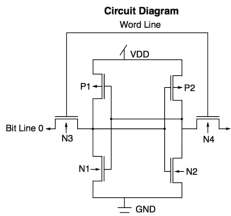
Random-access memory (RAM)



- Typically volatile memory
 - bits are not held without power supply
- Read and written to easily by embedded system during execution
- Internal structure more complex than ROM
 - a word consists of several memory cells, each storing 1 bit
 - each input and output data line connects to each cell in its column
 - rd/wr connected to every cell
 - when row is enabled by decoder, each cell has logic that stores input data bit when rd/wr indicates write or outputs stored bit when rd/wr indicates read

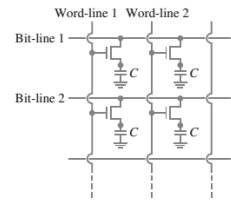
SRAM: Static RAM

- Memory cell uses flip-flop to store bit
- Requires 6 transistors
- Holds data as long as power supplied

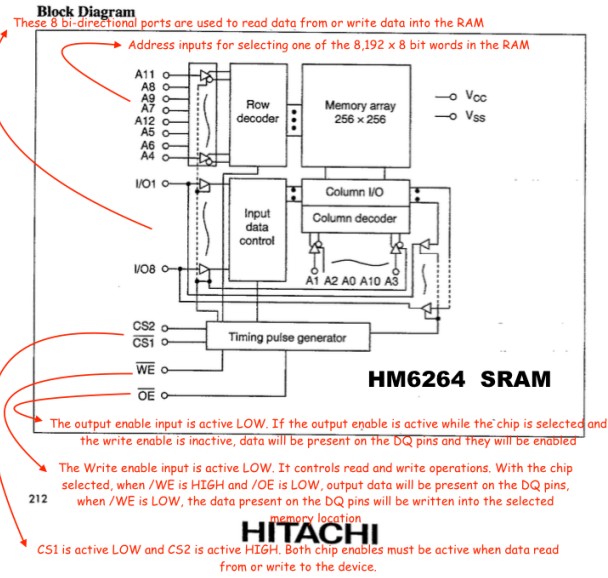


DRAM: Dynamic RAM

- Memory cell uses MOS transistor and capacitor to store bit
- More compact than SRAM
- "Refresh" required due to capacitor leak
- dynamic memory cells must be repeatedly read and restored, this process is called memory refresh.
- Typical refresh rate 15.625 microsec.
- Slower to access than SRAM



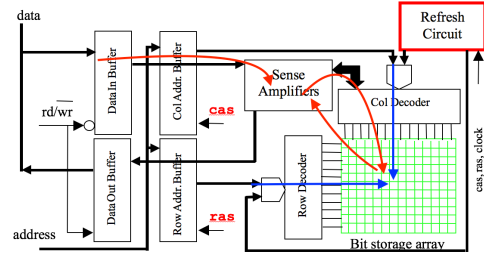
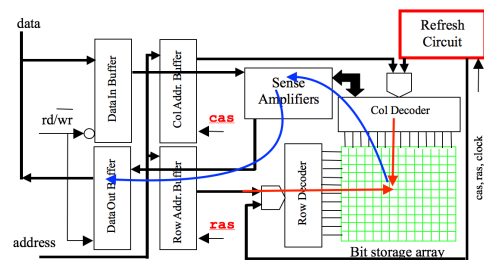
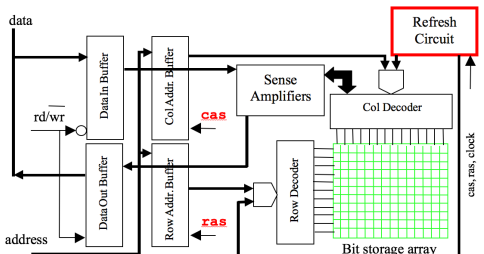
▶ YouTube :RAMs ▶ YouTube:SRAM ▶ YouTube:DRAM

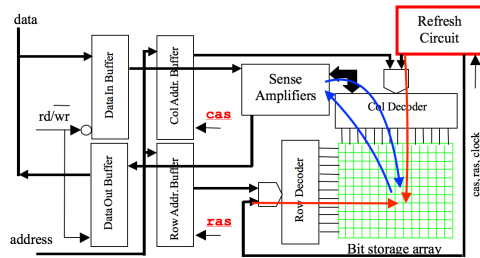


▶ HM6264 Datasheet

DRAM Architecture

- Address bus multiplexed between row and column components
- Row and column addresses are latched in, sequentially, by strobing ras and cas signals, respectively
- Refresh circuitry can be external or internal to DRAM device
 - strokes consecutive memory address periodically causing memory content to be refreshed
 - refresh circuitry disabled during read or write operation





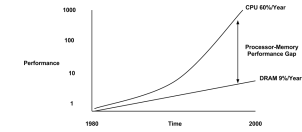
▶ YouTube: Raed ▶ YouTube: Refresh ▶ YouTube: Write

▶ KM41464 Samsung, Datasheet

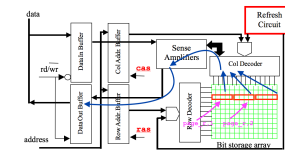
256 rows and 256 cols., 256 rows refresh in 4ms therefore $15\mu s$ per row!

- Refresh cycle shown needs an external DRAM controller to step through the rows and supply refresh signals at appropriate times
- More modern method is "CAS before RAS" refresh (memory uses the otherwise unused CAS before RAS input to initiate a refresh cycle) which is associated with an internal refresh address counter. DRAM controller only chooses refresh times.

- DRAMs commonly used as main memory in processor based embedded systems (high capacity, low cost)



- Many variations of DRAMs proposed
 - FPM DRAM: fast page mode DRAM



- EDO DRAM: extended data out DRAM
- SDRAM/ESDRAM: synchronous and enhanced synchronous DRAM
 - SDRAM latches data on active edge of clock
 - Eliminates time to detect ras/cas and rd/wr signals
 - A counter is initialized to column address then incremented on active edge of clock to access consecutive memory locations

▶ MT48LC32M8A2 Micro, Datasheet