# Microprocessor System Design

EHB432E

Lecture -3

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## Single-purpose processors

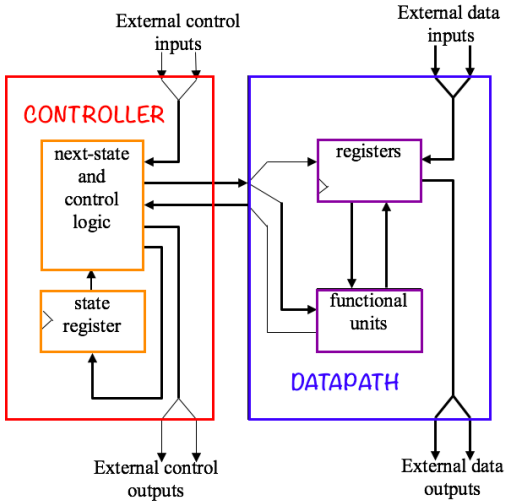
A single-purpose processor can only carry out particular computational task.

- Combinational Logic
  - Driver, AND, OR, XOR, INVERTER, NAND, NOR, XNOR
  - RT-Level Combinational Components:
    - Miltiplexor, Decoder, Adder, Comparator, ALU
  - Combinational logic design (Karnaugh map,...)
- Sequential Logic
  - RT-Level Sequential Components
    - Register, Shift Register, Counter
  - Sequential logic design

BLG 231E Digital Circuits



## Single-purpose processor basic model

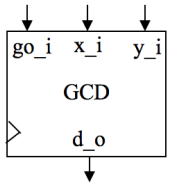





## Example: greatest common divisor

- The system specification
  " compute a greatest common divisor of two inputs"

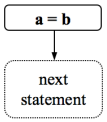
Black-box view




```
0:  int x, y;
1:  while (1) {
2:  while (!go_i);
3:  x = x_i;
4:  y = y_i;
5:  while (x != y) {
6:  if (x < y)
7:  y = y - x;
else
8:  x = x - y;
}
9:  d_o = x;
}
```

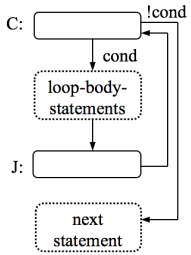
Assignment statement

```
a = b
next statement
```



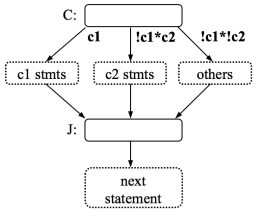

Loop statement

```
while (cond) {
loop-body-
statements
}
next statement
```




Branch statement

```
if (c1)
c1 stmts
else if c2
c2 stmts
else
other stmts
next statement
```

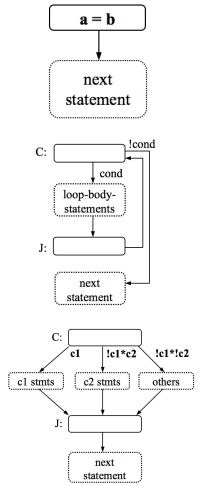




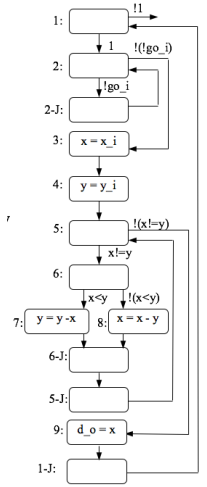

Algorithm

```
0:  int x, y;
1:  while (1) {
2:  while (!go_i);
3:  x = x_i;
4:  y = y_i;
5:  while (x !=
y) {
6:  if (x < y)
7:  y = y - x;
else
8:  x = x - y;
}
9:  d_o = x;
}
```

Templates




→ FSM with data (FSMD)

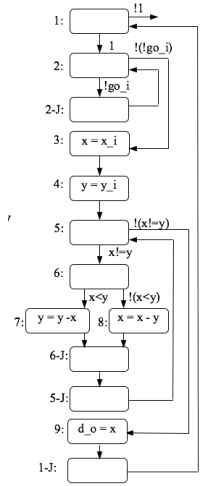


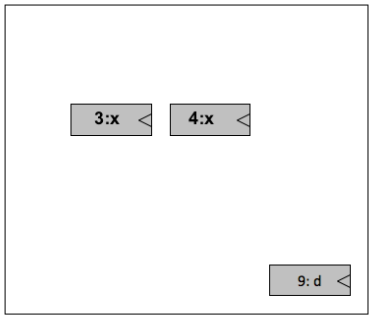

Behavioural Specification !



## Register Transfer (RT) specification

- Create a register for any declared variable

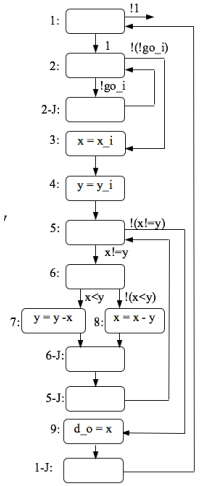


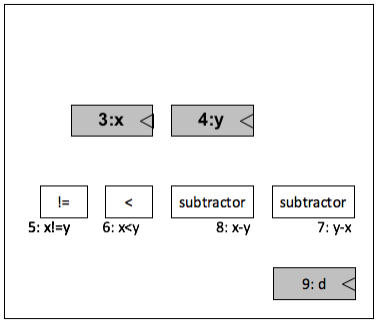






## Register Transfer (RT) specification

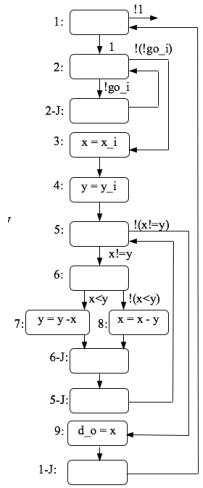
- Create a functional unit for each arithmetic operation

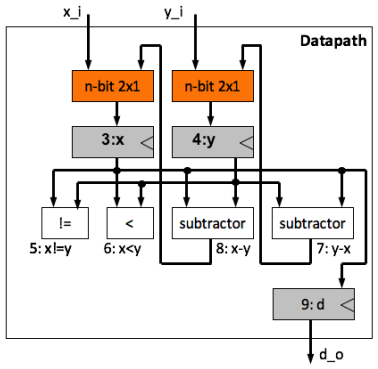


## Register Transfer (RT) specification

- Connect the ports, registers and functional units

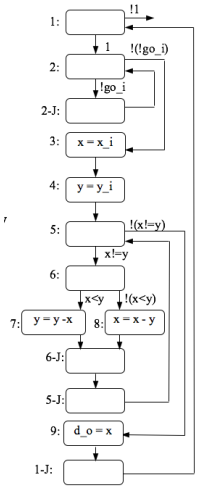


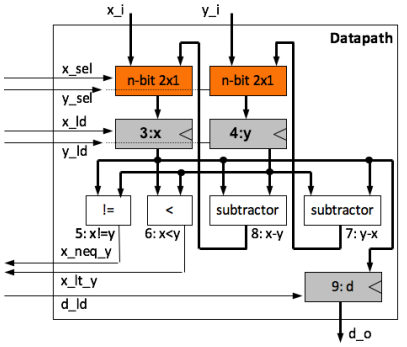






## Register Transfer (RT) specification

- Create unique identifier

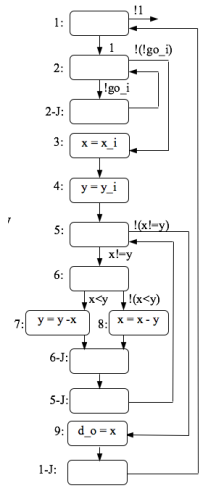


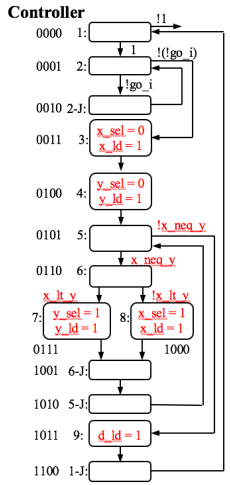






## Register Transfer (RT) specification

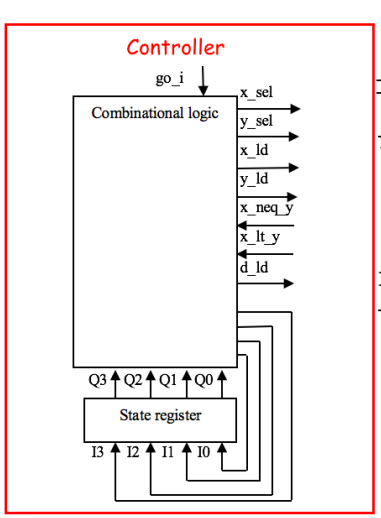
Creating the controller's FSM: Replace complex actions/conditions with datapath configurations

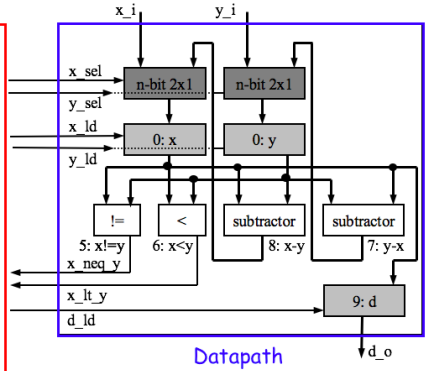





Creating the controller's FSM:




How to design combinational logic in the controller ? Figure 2.12, page: 43
Optimizing single-purpose Processor ! –; Read Chp. 2.6

# General-purpose processors