LOW VOLTAGE CURRENT DIFFERENCING TRANSCONDUCTANCE AMPLIFIER IN A NOVEL ALLPASS CONFIGURATION

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Summary

- Introduction
- CDTA (Current Differencing Transconductance Amplifier)
- Proposed Circuit and Its Simulation Results
- Allpass Filter Application and Its Simulation Results

Introduction

- Low power consumption is one of the important points in the circuit design. Using lower supply voltages is a trend with new technology. Low voltage can be best achieved in current mode circuits.
- CDTA active element is useful in current mode applications. It provides realization of circuit solutions with less number of passive elements than its counterparts.
- In this work, ±0.75V a new low voltage CDTA and its allpass filter application are given.

CDTA

CDTA is a five terminal active device. It consists of input current substractor which takes the difference of input currents and transfers it to z terminal. This current is converted into voltage at Z terminal and output dual transconductance stage converts this voltage to dual output currents with a transconductance "g".

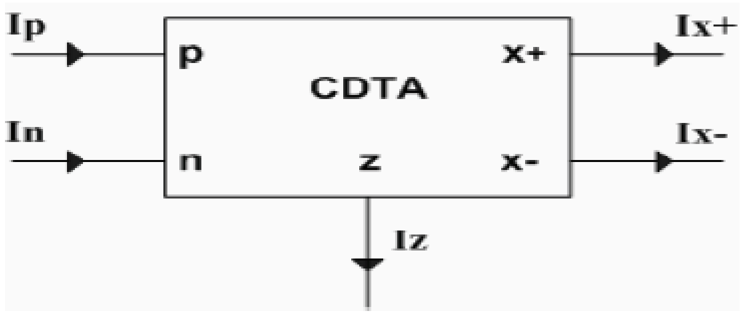


Figure 1: CDTA element symbol

$$V_p = V_n = 0 \qquad I_z = I_p - I_n$$
$$I_{x+} = gV_z \qquad I_{x-} = -gV_z$$

CDTA

- Input resistance of CDTA is ideally zero and output resistance is infinite.
- Z terminal is usually loaded with grounded impedance.
- If Z terminal is open circuit or a high resistance is connected to Z terminal, CDTA behaves like COA.

Proposed CDTA Circuit

M1-M10 transistors form the input stage. M2-M3, M8-M9 transistors are the input voltage followers. They decreases input resistance. Channel lengths of current mirrors are chosen larger to decrease channel length modulation effect which causes DC offset at the input. However, this decreases bandwidth.

M11-M18 are the transistors of the output stage.

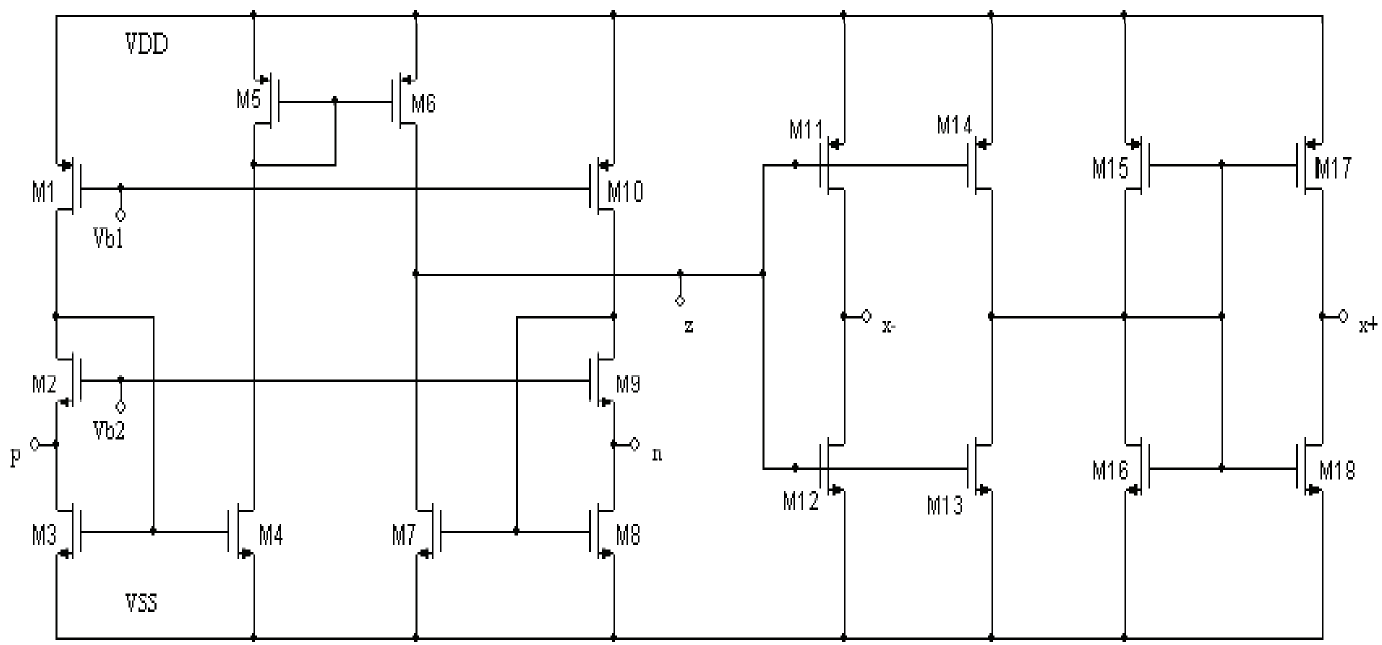


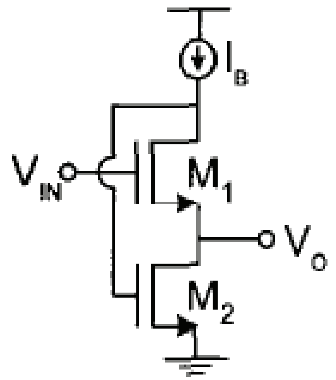
TABLE I. ASPECTS OF TRANSISTORS

M1= 30μ / 0.7μ	M10= 30μ / 0.7μ
M2= 30μ / 0.7μ	M11= 50μ / 0.7μ
M3= 90μ / 2.1μ	M12= 4μ / 1.4μ
M4= 90μ / 2.1μ	M13= 4μ / 1.4μ
M5= 150μ / 3.5μ	M14= 50μ / 0.7μ
M6= 150μ / 3.5μ	M15= 50μ / 0.7μ
M7= 90μ / 2.1μ	M16= 4μ / 1.4μ
M8= 90μ / 2.1μ	M17= 50μ / 0.7μ
M9= 30μ / 0.7μ	M18= 4μ / 1.2μ

Figure 2: Proposed CDTA circuit

Input Stage

Input stage consists of voltage follower stage as shown in Figure 3. Negative Feedback decreases the output resistance of this circuit.



$$R_{out} = \frac{\frac{1}{g_{m1}}(1+\frac{r_b}{r_{o1}}) // r_{o2}}{1+g_{m2}(r_b // g_{m1} r_{o1} r_{o2})}$$

Figure 3: Input Stage source follower

If the current source is a simple current mirror, $r_b \approx r_{o1} \rightarrow R_{out} = 2 / g_{m2} g_{m1} r_{o1}$

If it is a cascode current mirror, $r_b \approx g_{m1} r_{o1} r_{o2} \rightarrow R_{out} = 1 / g_{m2} g_{m1} r_{o1}$

For the proposed circuit these resistances are given below.

$$R_{in_p} \approx \frac{1}{g_{m2} g_{m3} r_{o3}} \qquad R_{in_n} \approx \frac{1}{g_{m8} g_{m9} r_{o8}}$$

Output Stage

- Output stage consists of cascaded 4 inverters that are used for analog signal processing. Output stage is given in Figure 4. M11-M12 and M13-M14 are 1st and 2nd inverters which are used as transconductance amplifier. They convert the voltage at z terminal to current. M15-M16 and M17-M18 transistors are 3rd and 4th inverters. They are used as current mirrors and form positive x+ current. Transconductance of the CDTA is given as $g_m=g_{m11}+g_{m12}$.
- Matching between these transistors is important for the circuit to operate properly.

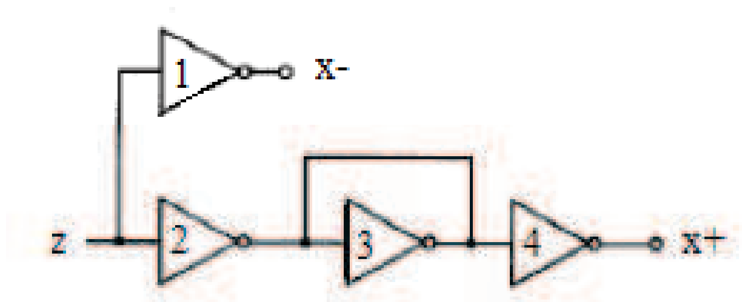


Figure 4: Output stage

Simulation Results

- Input Resistance vs Frequency

Change of input resistances is given below. It is seen that the input resistance is 24.4 ohm @1Mhz. After this frequency, resistance increases.

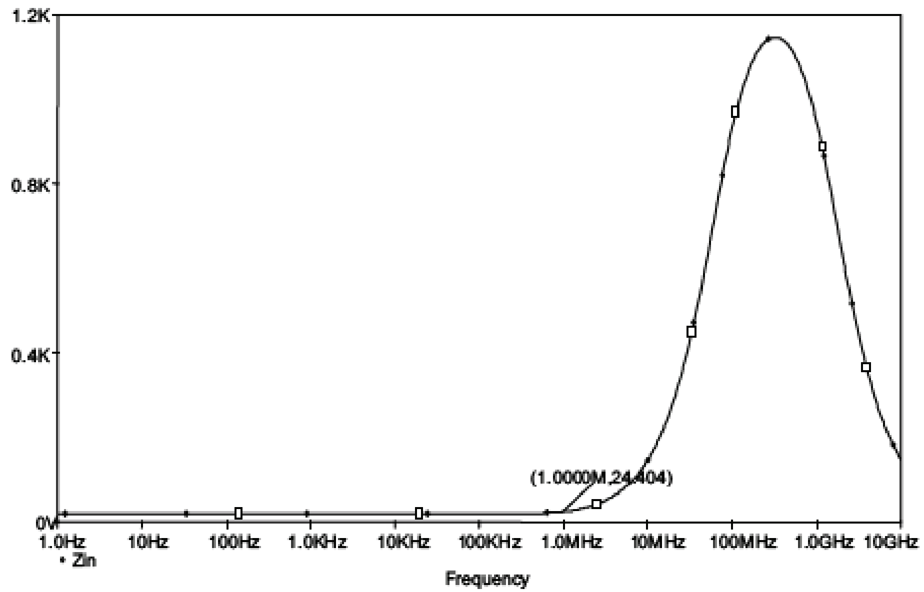


Figure 5: Input resistance vs frequency

Simulation Results

- **Variation of the z terminal current with respect to input currents**

Input offset current is 0.4uA. After 54uA, output current saturates. This is because bias current is constant. It can be increased using more bias current, but this increases power consumption.

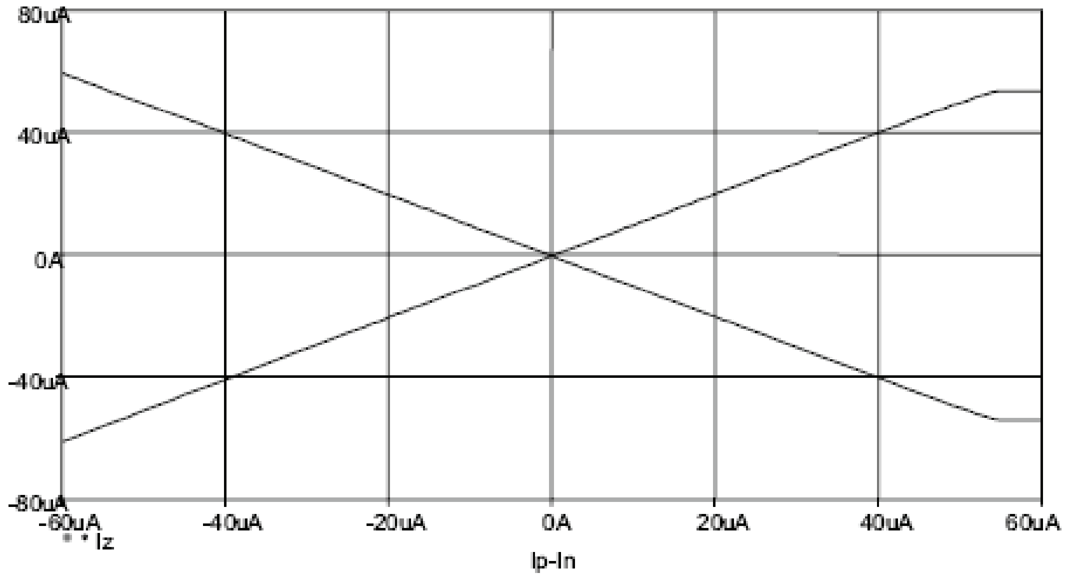


Figure 6: Variation of the z terminal current with respect to input currents

Simulation Results

Variation of current transfer from n to z with frequency

- Bandwidth of current transfer from n to z is 87 MHz.

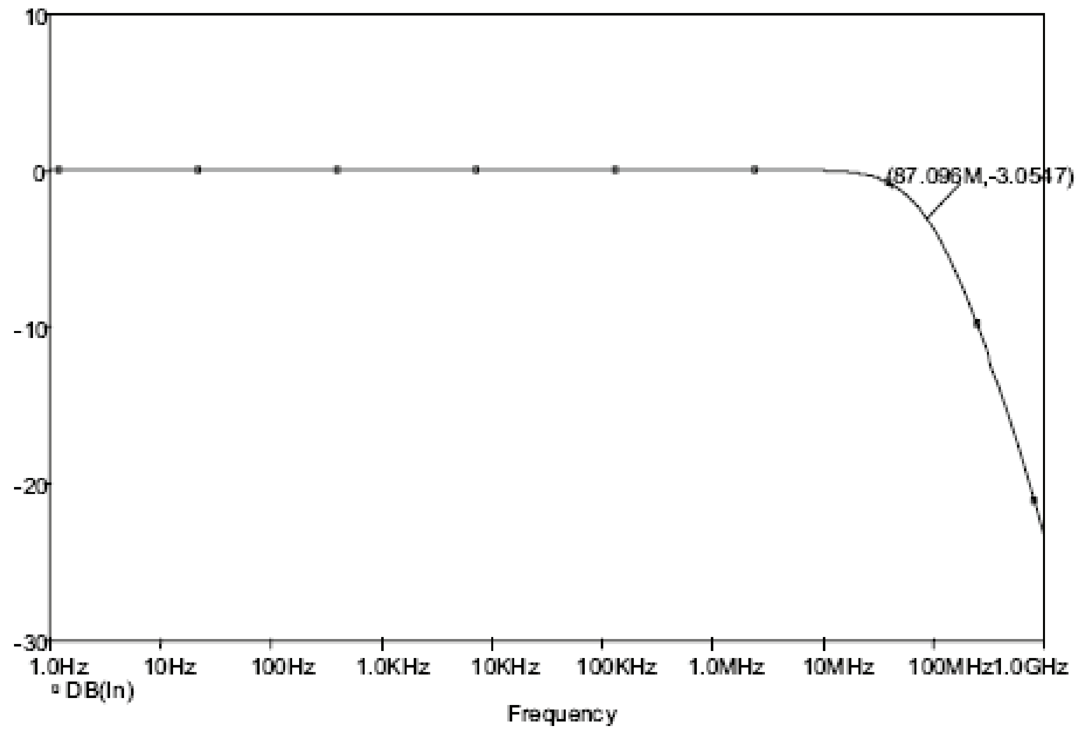


Figure 7: Variation of current transfer from n to z

Simulation Results

Variation of current transfer from p to z with frequency

Bandwidth of current transfer is 20 MHz. There is 70 MHz bandwidth difference between p and n current transfer curves. Current of p terminal passes through one more current mirror and it causes high frequency pole.

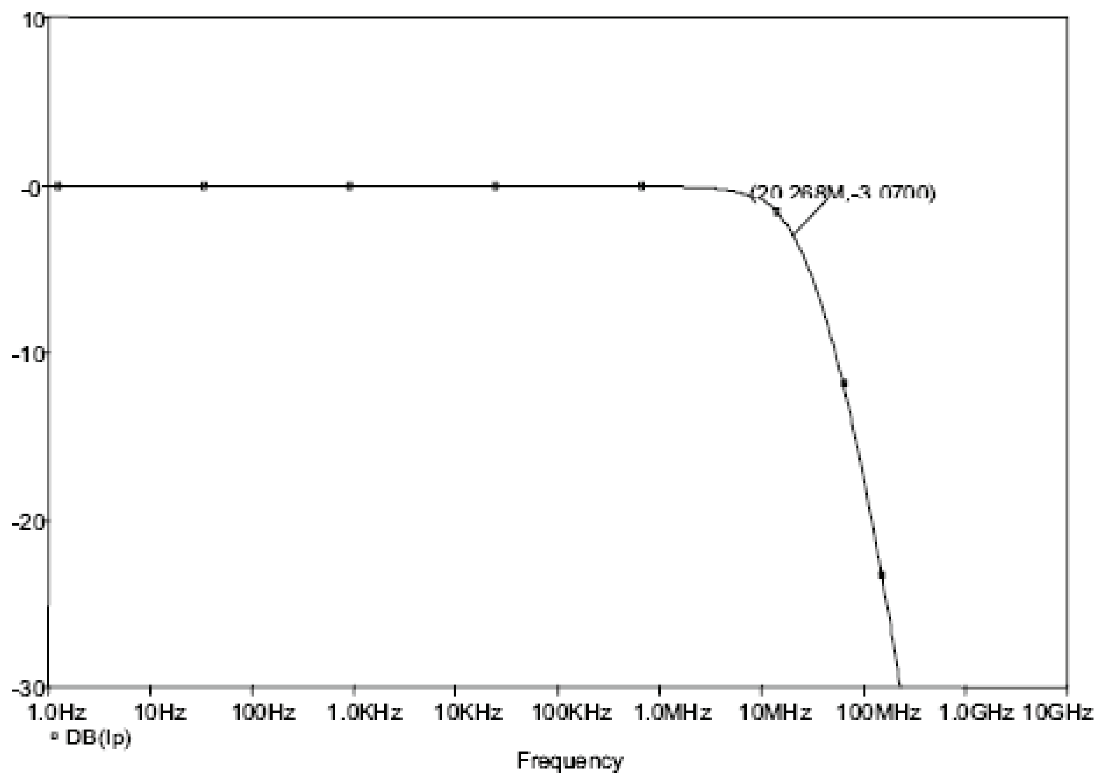


Figure 8: Variation of current transfer from p to z

Simulation Results

- Change of transconductances of CDTA

Since the outputs are not symmetric, bandwidths of +g and –g transconductances are not equal.

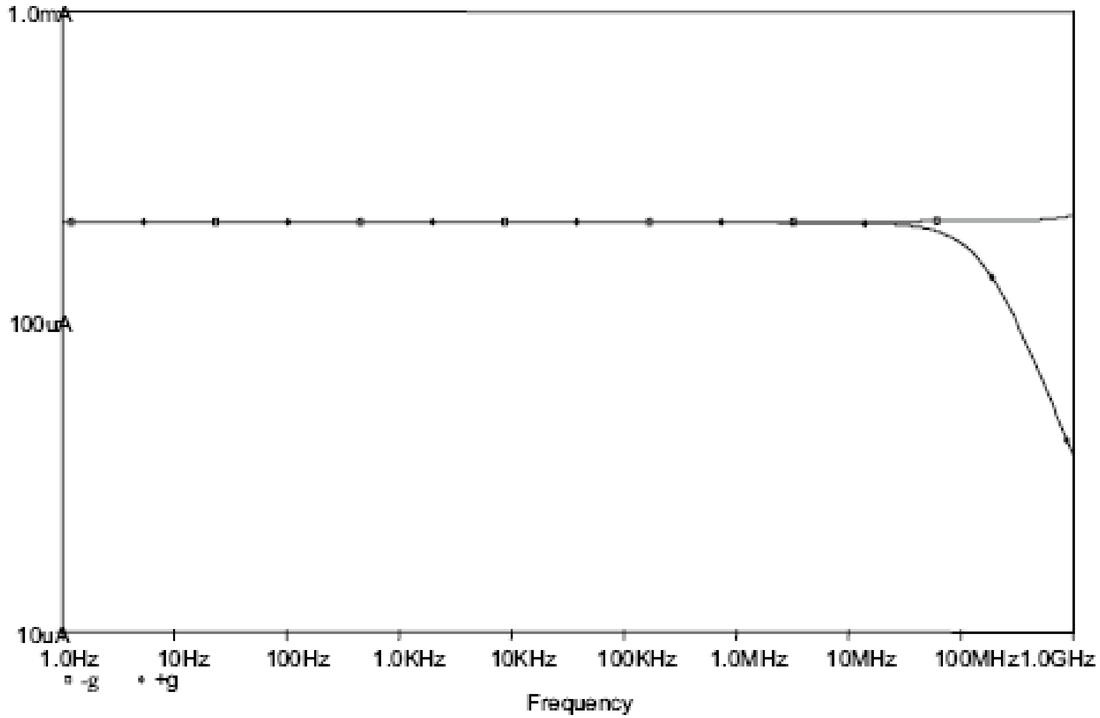


Figure 9: Transconductances of CDTA vs frequency

Simulation Results

- Summary of simulation results

  0.35μm AMIS process technology is used.

SUMMARY OF SIMULATION RESULTS

Supply Voltages	±0.75V
Bias Current	54μA
Technology	0.35μ AMIS
I_z/I_p (-3dB) Bandwidth	87MHz
I_z/I_n (-3dB) Bandwidth	20MHz
p input resistance	25Ω@1MHz
n input resistance	25Ω@1MHz
Power Consumption	0.37mW
Transconductance (g)	210μA/V
Biasing Voltages	Vb1=-0.2V, Vb2=0.3V
Input Offset Current	0.4μA

Allpass Filter Configuration

- Allpass filters have some applications from phase shaping to quadrature oscillators.
- Allpass configuration is given below. CDTA decreases number of passive elements to obtain allpass filter with respect to other active filters.

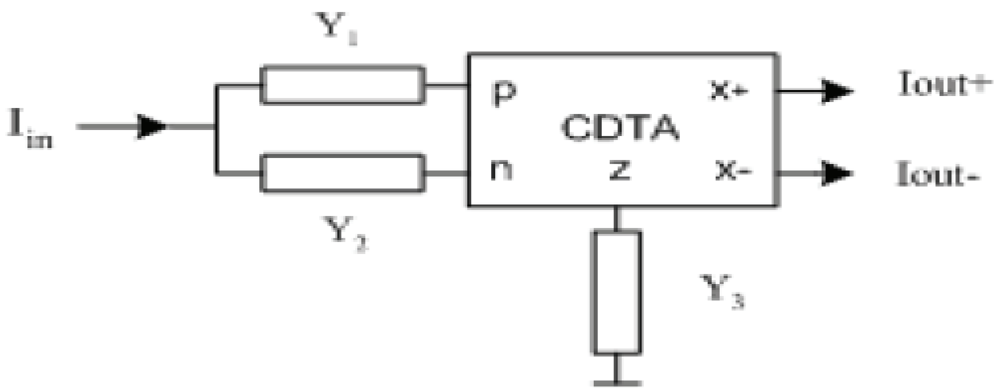


Figure 10: CDTA filter configuration

$$\frac{I_{out-}}{I_{in}} = (g / Y_3)\frac{Y_2 - Y_1}{Y_1 + Y_2}$$

Y_2=G, Y_1=sC

$$\frac{I_{out-}}{I_{in}} = \frac{1 - sCR}{1 + sCR}$$

Simulation Results

- Large signal response of the proposed filter

50k load resistance is connected to the output of filter, output voltage is given below. 1 V_{pp} output voltage is obtained.

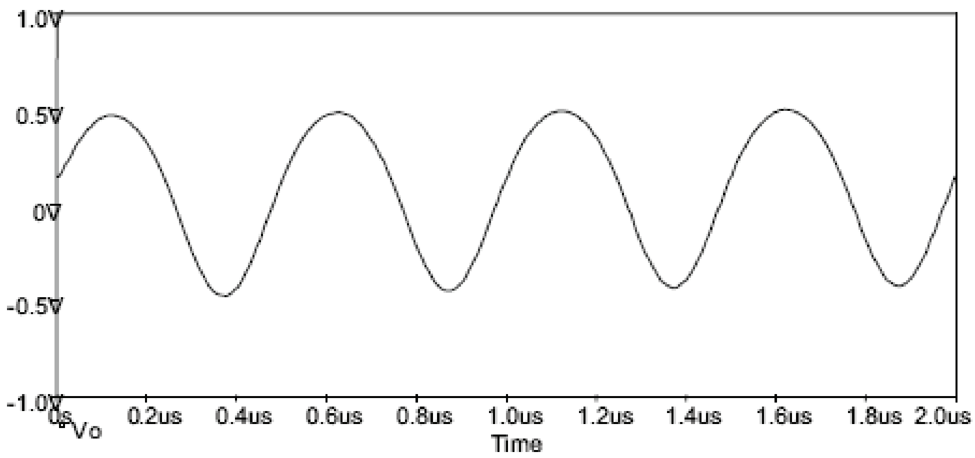


Figure 11: Large signal response of the allpass filter

Simulation Results

- Frequency Response of the filter

Change of phase and magnitude of the filter with frequency for the given passive element values are given below.

$R1=1k\Omega$, $R_2=4.8k\Omega$ and $C=1nF$

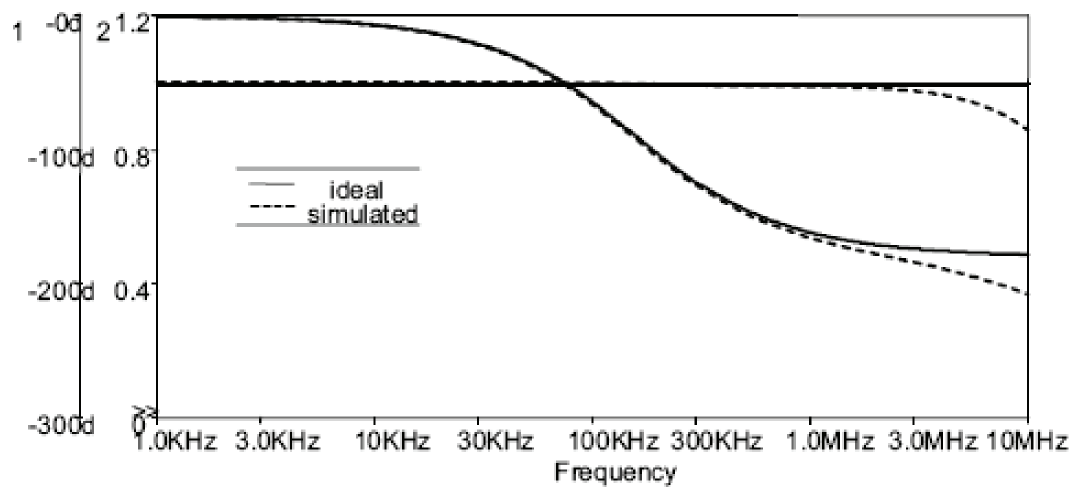


Figure 12: Frequency response of the filter

Conclusion

- A new low voltage CDTA is proposed.
- Its input resistance is low enough due to voltage followers at the input.
- Proposed CDTA is then used in first order allpass filter.

References

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[4] Mucha, I. “Low-voltage current operational amplifier with a very low current consumption”, Circuits and Systems, 1996. ISCAS '96., 'Connecting the World'., 1996 IEEE International Symposium Vol. 1, May 1996 pp. 525 – 528.