A New CMOS Current Differencing Transconductance Amplifier (CDTA) and Its Biquad Filter Application

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Outline

- Introduction
- Current Differencing Transconductance Amplifier (CDTA)
- CMOS Realization of CDTA and Simulation Results
- Biquad Filter Employing CDTA
- Conclusion

Introduction

- Nowadays, a universal filter working in current-mode has been more popular than voltage mode one.
- A recently reported five terminals active element, namely current differencing transconductance amplifier (CDTA) seems to be a versatile component in the realization of a class of analog signal-processing circuits, especially in realization of analog frequency filters.
- It leads to very compact circuit structures. Especially, when more than two output terminals are used, it is possible to obtain very compact circuit topologies requiring less passive elements.
- As a result, many implementations of CDTA-based circuits have also been developed by various researchers

Introduction (cont'd)

- Universal biquad filter is one of the most popular filter types.
- In this paper, a new improved CMOS configuration of CDTA is presented providing low input impedances at ports p and n, very high out impedances at ports z and x, a good linearity and high input/output gain ratio for current transfer.
- To demonstrate the performance of the CDTA circuit, a three input single-output transadmittance type universal filter was chosen
- The simulations show that the proposed CDTA circuit exhibits a very good performance and the results obtained for the filter are in good agreement with theory.

Current Differencing Transconductance Amplifier (CDTA)

- The CDTA symbol is illustrated in Figure.1 .
- Current differencing transconductance amplifier consists of an input current substractor and dual output transconductance stage.
- Using standard notation, the port relations of an ideal CDTA shown in Figure.1 can be characterized by

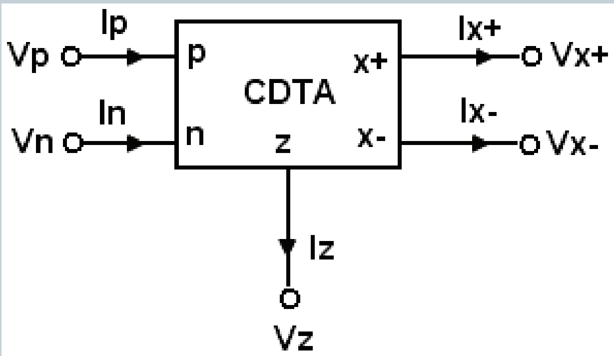

Figure.1. The Symbol of the CDTA

$$V_p = V_n = 0$$
$$I_z = \alpha_p I_p - \alpha_n I_n$$
$$I_{x+} = g V_z$$
$$I_{x-} = -g V_z$$

where α_p and α_n are current gains, and $\alpha_p = 1-\varepsilon p$, $\alpha_n = 1-\varepsilon n$. Here, εp, εn are the current tracking errors, and their absolute values are much less than the unit value

CMOS Realization

The proposed high performance CDTA is shown in Figure.2.

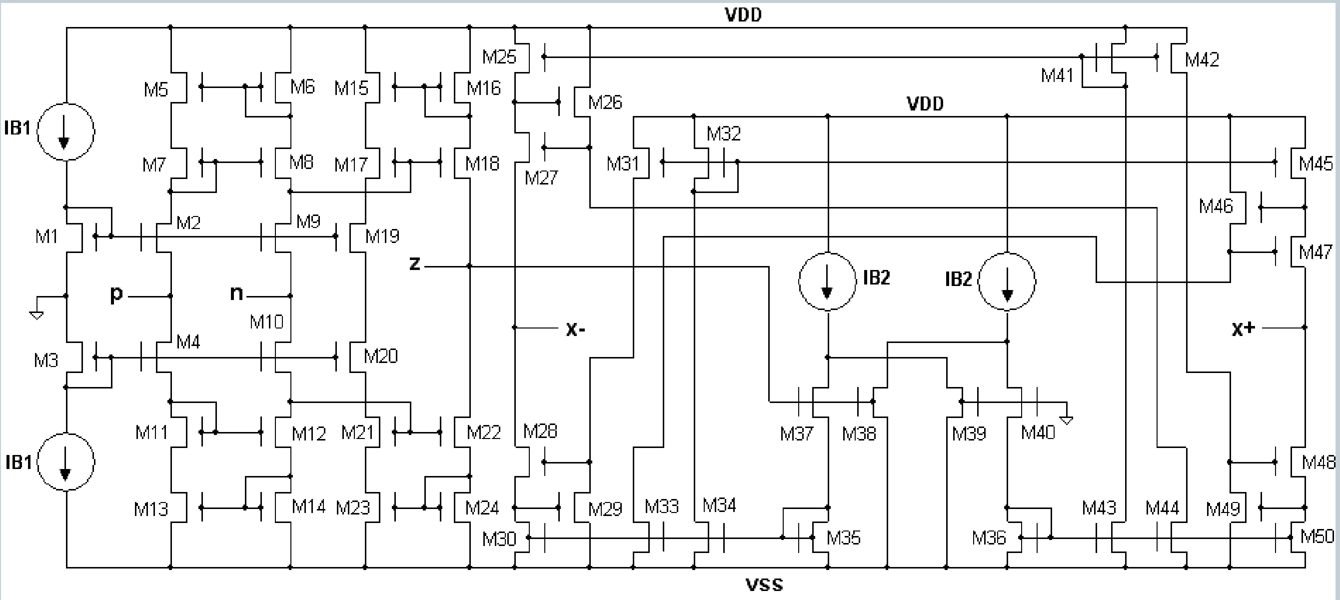

Fig.2. The proposed high performance CDTA

CMOS Realization (cont'd)

- Input resistances of the p and n terminals, output resistance of z, x+ and x- can be calculated approximately using the following equation.

$$R_p \cong \frac{1}{(g_{m2} + g_{m4}) + (r_{ds2} // r_{ds4})}$$

$$R_n \cong (r_{ds9} r_{ds8} g_{m9}) // (r_{ds10} r_{ds12} g_{m10})$$

$$R_z \cong \frac{1}{(g_{m18} + g_{m22}) + (r_{ds18} // r_{ds22})}$$

$$R_x \cong [g_{m48} g_{m49} r_{ds50}] // [g_{m47} g_{m46} r_{ds45}]$$

$$R_x \cong [g_{m28} g_{m29} r_{ds30}] // [g_{m27} g_{m26} r_{ds25}]$$

Simulation Results

- The performance of the proposed CDTA is verified using the SPICE simulation program. The MOS transistors are simulated using TSMC CMOS 0.35μm process model parameters.
- The supply voltages, and biasing currents are given by $V_{DD} = -V_{SS} = 1.5V$, $I_{B1} = 100$ μA, $I_{B2} = 50$ μA respectively.

Table.1 Transistors aspect ratios for the proposed circuit

Transistors	W(μm)	L(μm)
$M_1, M_2, M_5\text{-}M_8, M_{10}, M_{15}\text{-}M_{18}, M_{20}$	14	0.7
$M_3, M_4, M_9, M_{11}\text{-}M_{14}, M_{19}, M_{21}\text{-}M_{24}$	28	0.7
$M_{25}, M_{26}, M_{35}, M_{37}, M_{45}$	21	0.7
M_{27}, M_{30}	2.8	2.8
M_{28}, M_{29}, M_{44},	7	0.7
$M_{31}, M_{32}, M_{36}, M_{47}, M_{48}$,	2.1	0.7
$M_{33}, M_{34}, M_{40}, M_{41}, M_{49}, M_{50}$	1.4	0.7
$M_{38}, M_{39}, M_{42}, M_{43}, M_{46}$,	0.7	0.7

Simulation Results (cont'd)

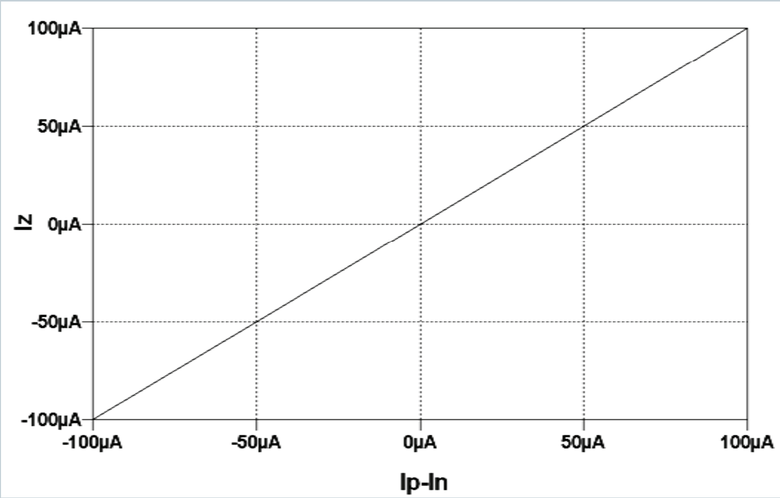

Fig.3 Current transfer from p to z. (I_n=0)

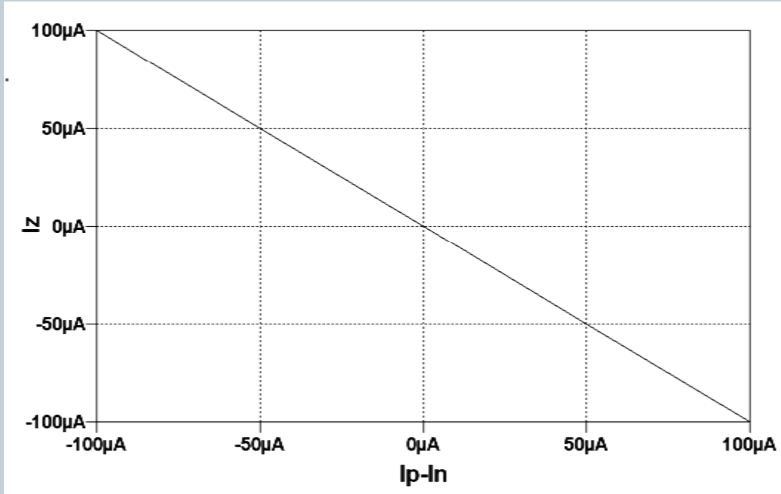

Fig.4 Current transfer from p to z. (I_p=0)

Simulation Results (cont'd)

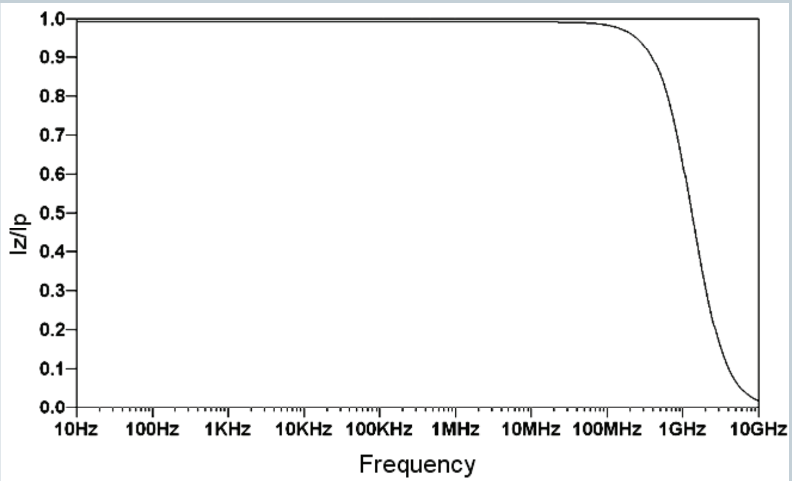

Fig.5 Frequency response of Iz/Ip

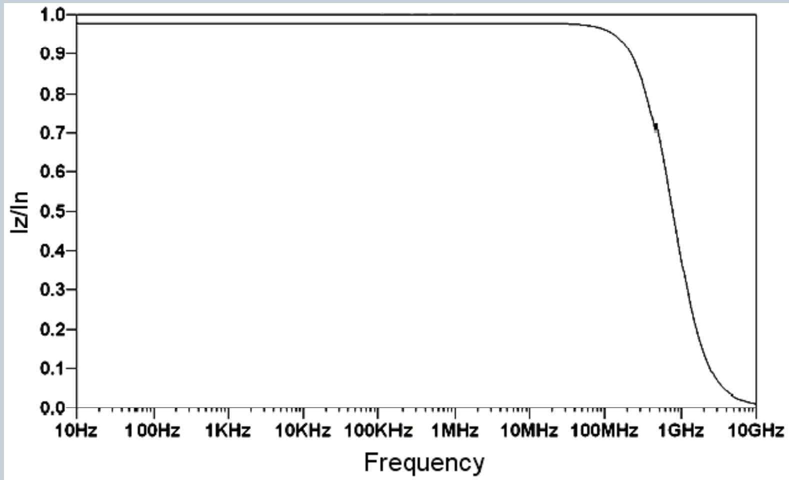

Fig.6 Frequency response of Iz/In

Simulation Results (cont’d)

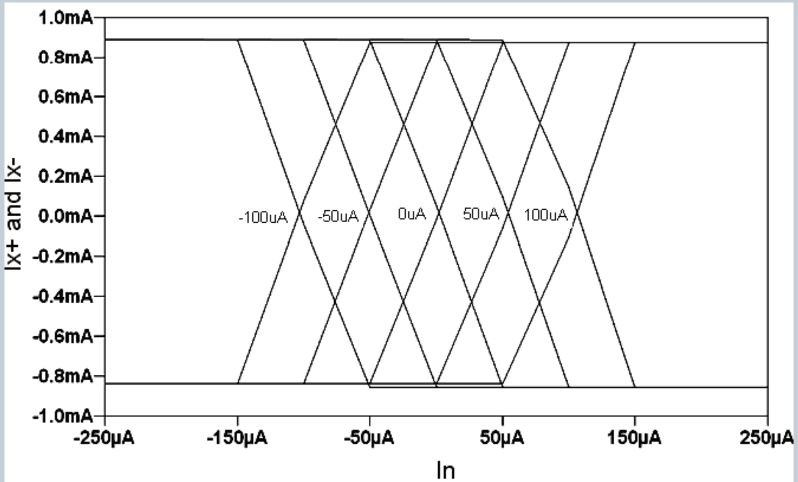

Fig.7 Variation of the z terminal current with respect to input currents (I_P: parametric)

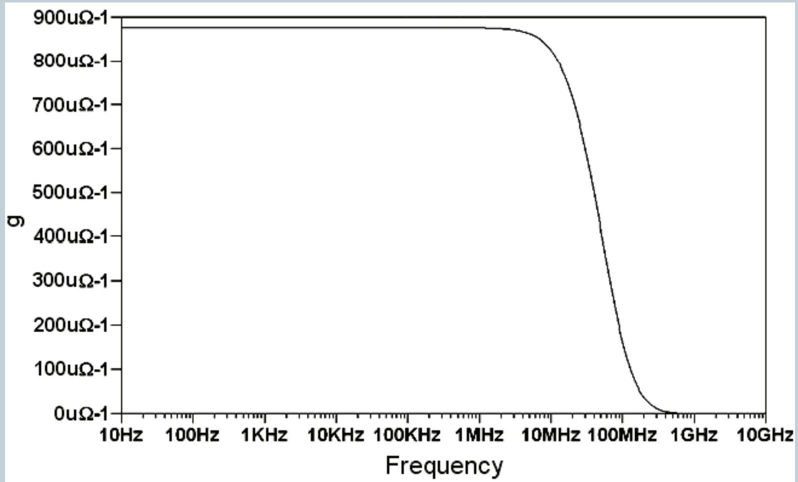

Fig.8 Transconductance of CDTA

Simulation Results (cont'd)

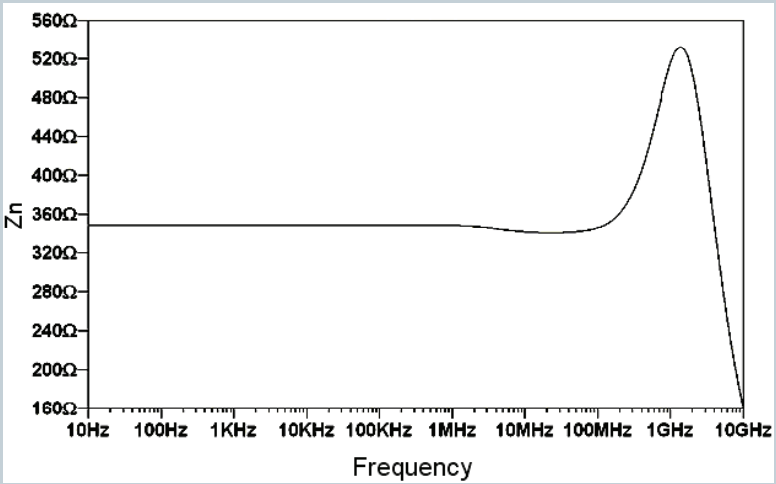

Fig.9 Frequency response of the input impedance at Z_n terminal

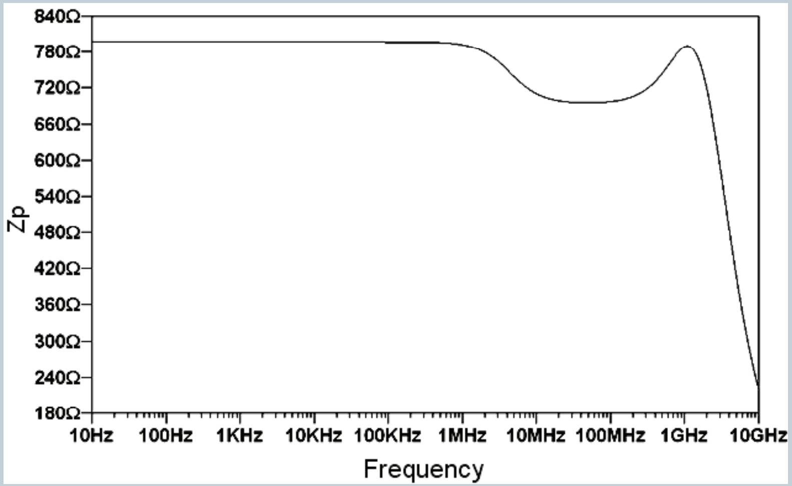

Fig.10 Frequency response of the input impedance at Z_p terminal

Simulation Results (cont'd)

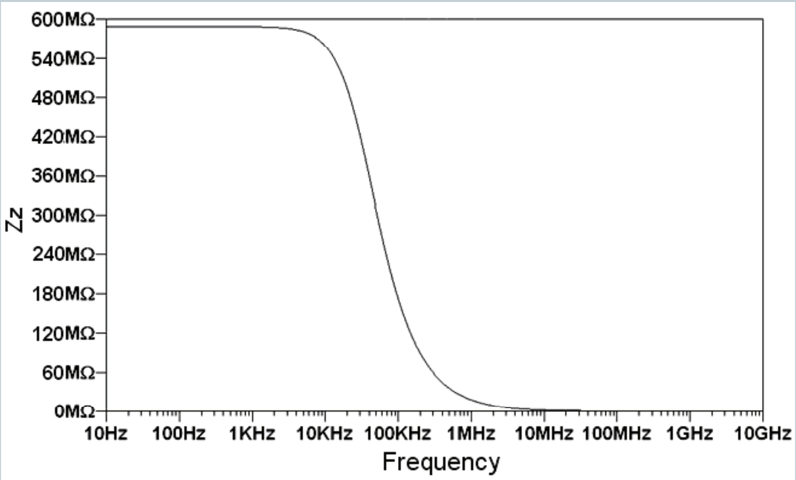

Fig.11 Frequency response of the input impedance at Z_Z terminal

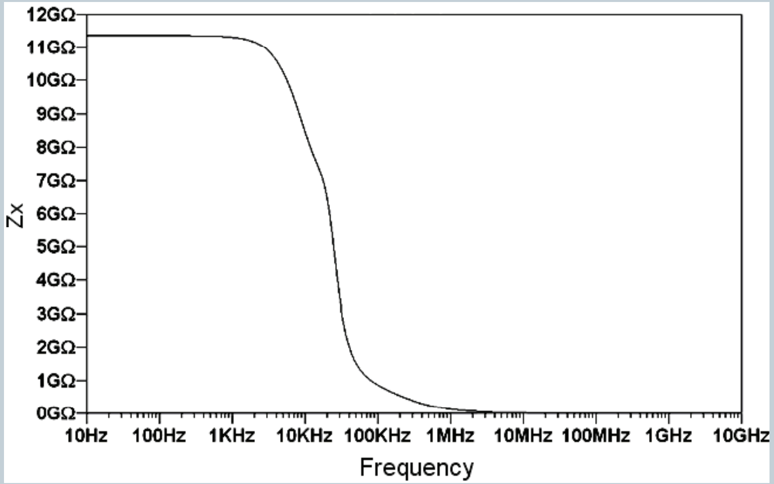

Fig.12 Frequency response of the input impedance at Z_X terminal

Simulation Results (cont'd)

Table.2. Circuit performances of the proposed CDTA

Supply Voltages	±1.5V
Bias Currents	I_{B1}=100µA, I_{B2}=50 µA
Technology	0.35µ TSMC
Iz/Ip (-3dB) Bandwidth	582 MHz
Iz/In (-3dB) Bandwidth	448 MHz
p input impedance	812 Ω
n input impedance	348 Ω
z output impedance	580 MΩ
x output impedance	11.7GΩ
Power Consumption	4.96 mW
Transconductance (g)	883 µA/V

Biquad Filter Employing CDTA

- One of the most important application areas of the transadmittance mode filters is the receiver baseband (BB) blocks of modern radio systems .
- The proposed transadmittance mode biquad contains two CDTAs, two capacitors and two resistors.

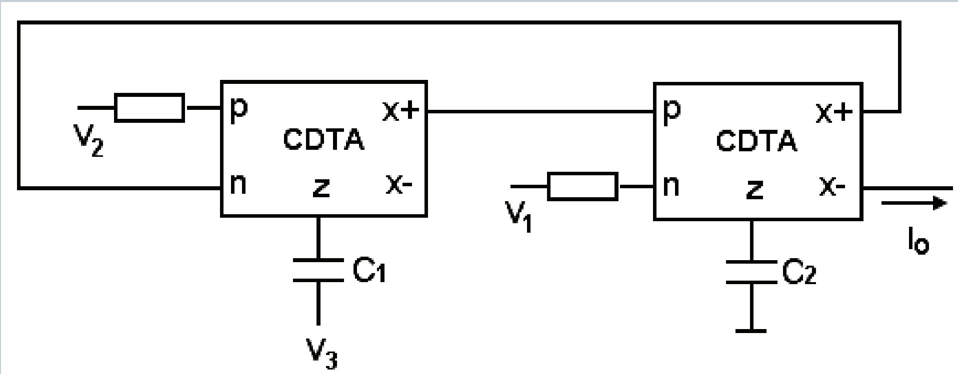

Fig.13 Proposed biquad filters employing CDTAs

Depending on the voltage status of V_{i1}, V_{i2}, and V_{i3} in the numerator of the following five transadmittance filter functions is realized:

1) $V_1 = V_{in}$ and $V_2 = V_3 = 0$, LPF
2) $V_2 = V_{in}$ and $V_1 = V_3 = 0$, BPF.
3) $V_3 = V_{in}$ and $V_1 = V_2 = 0$, HPF.
4) $V_1 = V_3 = V_{in}$ and $V_2 = 0$, BSF
5) $V_1 = -V_2 = V_3 = V_{in}$, APF

$$\omega_0 = \sqrt{\frac{g_1 g_2}{C_1 C_2}} \qquad Q = \sqrt{\frac{g_2 C_1}{g_1 C_2}}$$

$$I_{out} = g_1 \frac{V_3 s^2 + V_2 s \frac{1}{R_2 C_1} + V_1 \frac{g_2}{R_1 C_1 C_2}}{s^2 + s\frac{g_1}{C_1} + \frac{g_1 g_2}{C_1 C_2}}$$

Simulation Results

Figures 14, 15, 16, 17 and 18 show the simulated frequency responses for the low-pass band-pass, high-pass, notch and all-pass configurations.

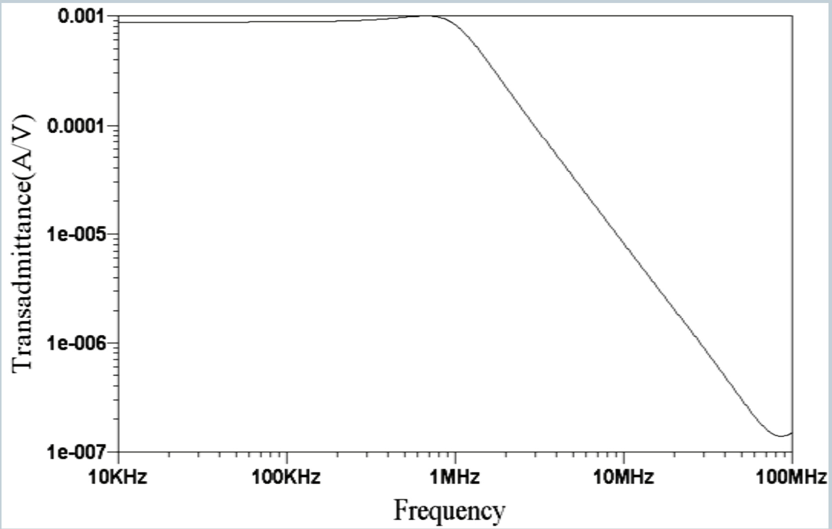

Fig.14 Frequency response of low-pass filter

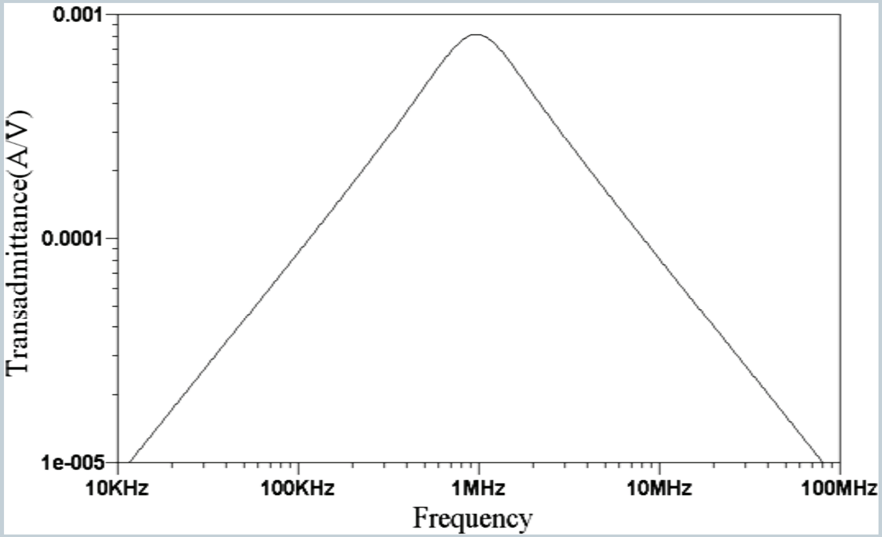

Fig.15 Frequency response of band-pass filter

Simulation Results (cont'd)

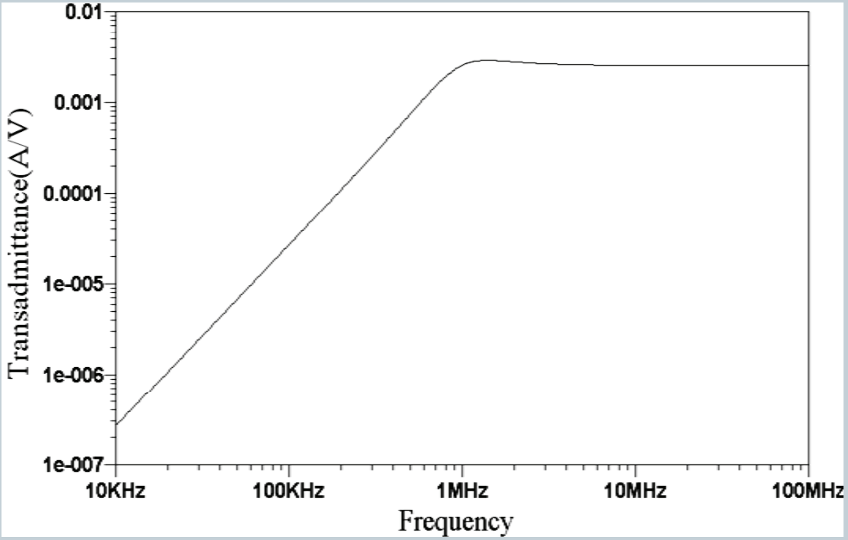

Fig.16 Frequency response of ligh-pass filter

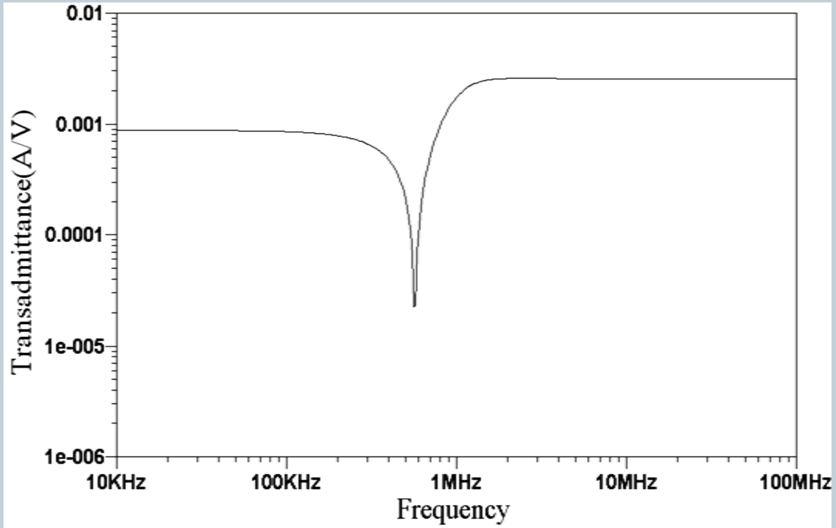

Fig.17 Frequency response of band-stop filter

Simulation Results (cont'd)

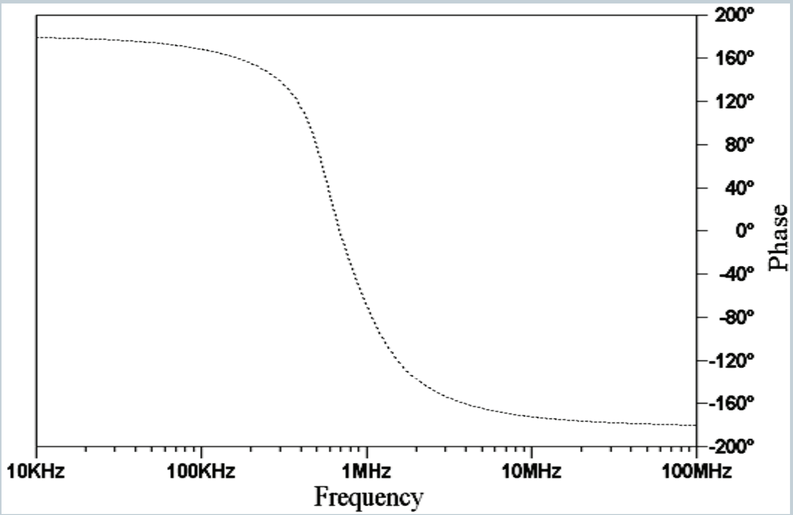

Fig.18 Frequency response of all-pass filter

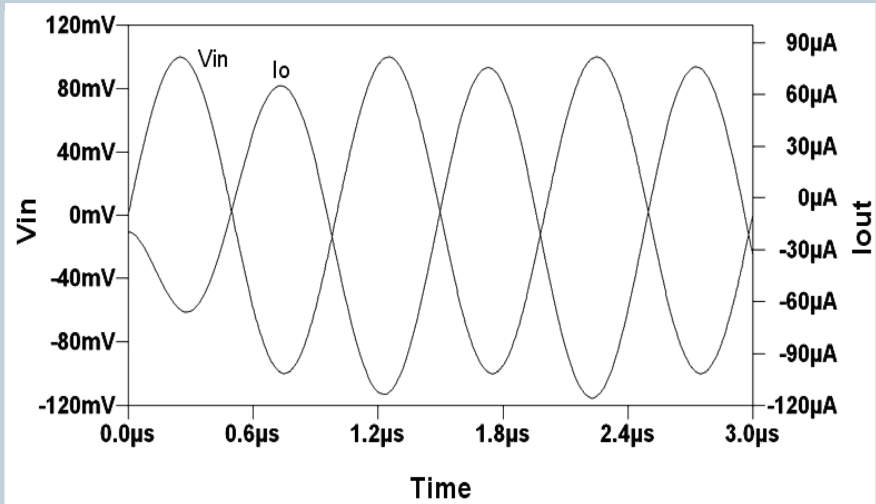

Fig.19 Time domain response of circuit in Fig.13 for 0.1V peak 1MHz sine wave input for band-pass filter configuration

Simulation Results (cont'd)

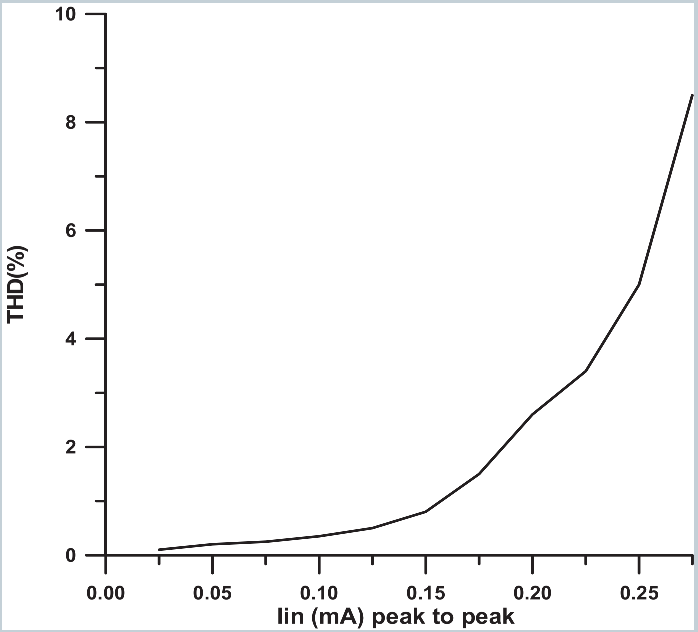

Fig.20 Total harmonic distortion (THD) of the LP filter for an input signal of 100μA amplitude at 1MHz.

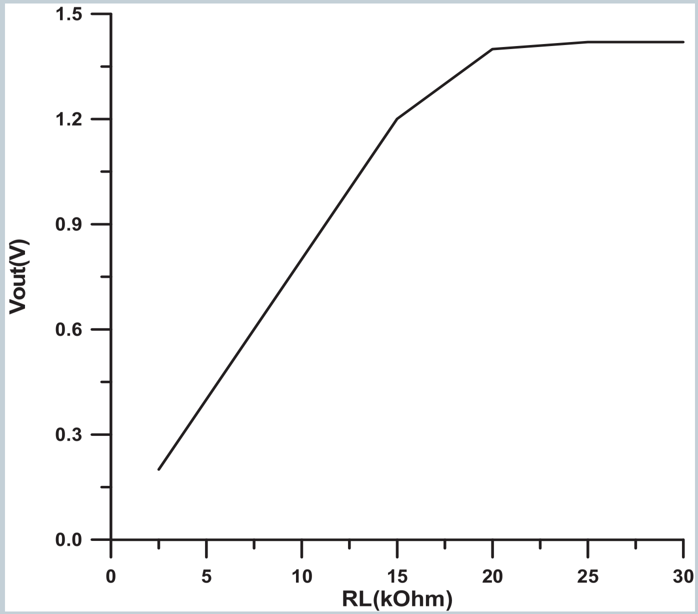

Fig.21 Dependence of the output amplitude on the load resistance for a constant input signal of 100μA.

Conclusion

- In this paper, a new high performance CMOS implementation of current differencing transconductance amplifier is presented.
- Simulated device characteristics show that the proposed circuit exhibits a very good performance.
- The simulation results confirm high linearity and high performance of the circuit in terms of good input and output resistances and wide bandwidths for both of the voltage and current operations.
- The proposed transadmittance mode biquad contains two CDTAs, two capacitors and two resistors. All of the filtering signals LP, BP, HP, BS and AP functions are obtained from the same configuration.
- The circuit also requires no component matching conditions. with the predicted theory.
- Proposed CDTA circuit and transadmittance type filter will provide new possibilities for analog IC designers.