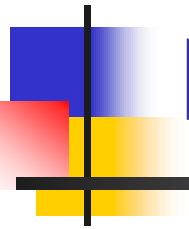
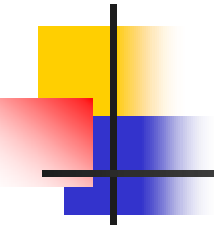


PLAs & PALs

Programmable Logic Devices (PLDs)

PLAs and PALs



PLAs&PALs

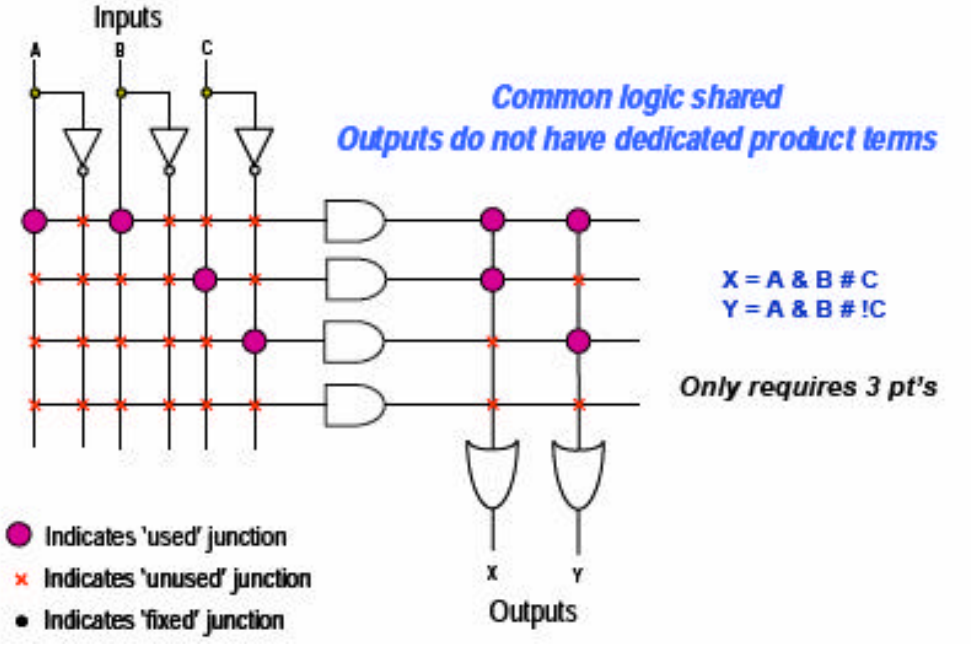
- By the late 1970s, standard logic devices were all the rage, and printed circuit boards were loaded with them.
- To offer the ultimate in design flexibility, Ron Cline from Signetics came up with the idea of two programmable planes.
- These two planes provided any combination of “AND” and “OR” gates, as well as sharing of AND terms across multiple ORs.

PLAs&PALs

- At the time wafer geometries of 10 μm made the input-to-output delay (or propagation delay) high, which made the devices relatively slow.

Simple PLA

Logic functions in Sum-of-Products



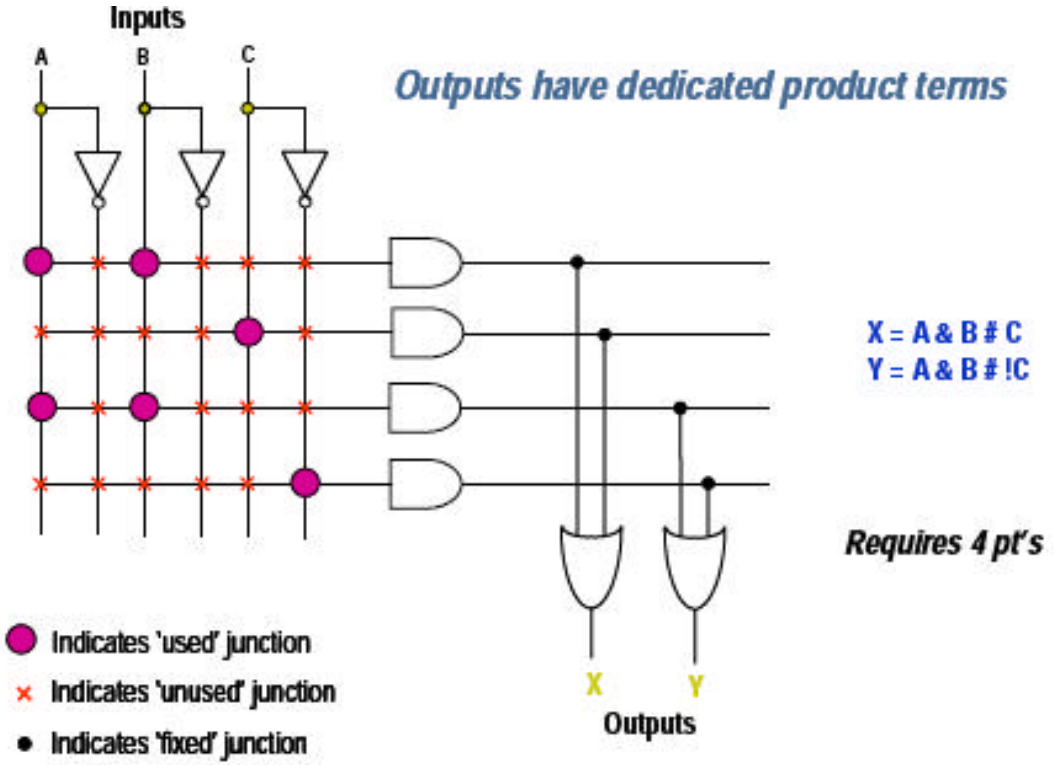
PLAs&PALs

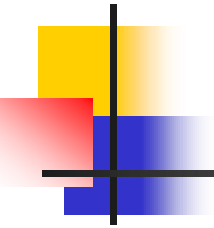
- MMI (later purchased by AMD™) was enlisted as a second source for the PLA array. After fabrication issues, it was modified to become the programmable array logic (PAL) architecture by fixing one of the programmable planes.

- This new architecture differed from that of the PLA in that one of the programmable planes was fixed – the OR array. PAL architecture also had the added benefit of faster t_{PD} and less complex software, but without the flexibility of the PLA structure.

PLAs&PALs

Simple PAL



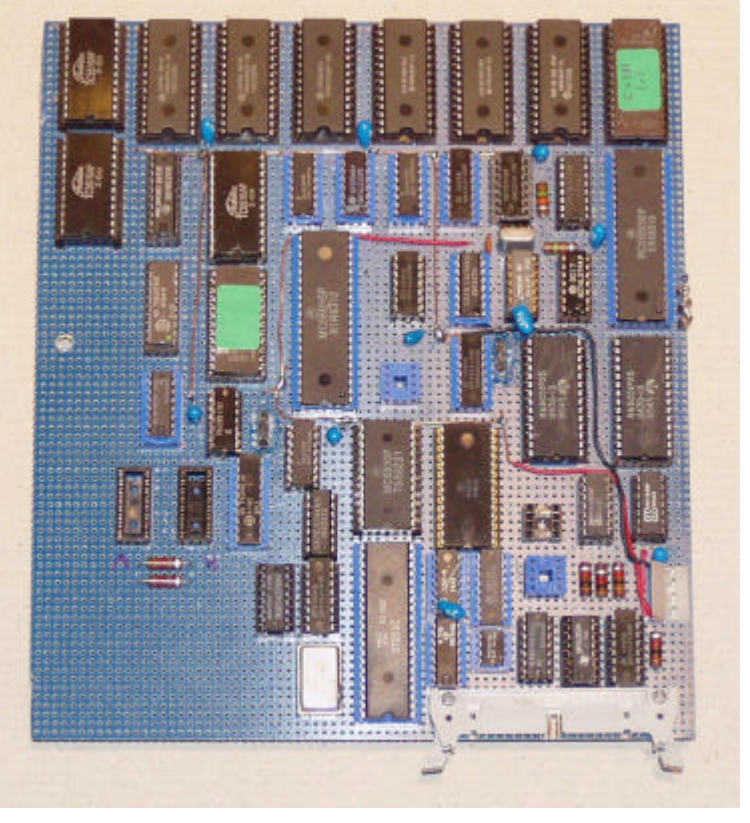


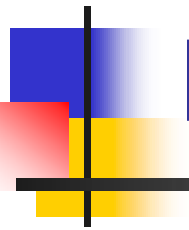
PLAs&PALs

- The architecture had a mesh of horizontal and vertical interconnect tracks.
- At each junction was a fuse. With the aid of software tools, designers could select which junctions would not be connected by “blowing” all unwanted fuses.
- Input pins were connected to the vertical interconnect. The horizontal tracks were connected to AND-OR gates, also called “product terms”. These in turn connected to dedicated flip-flops, whose outputs were connected to output pins.

PLAs&PALs

- PLDs provided as much as 50 times more gates in a single package than discrete logic devices!

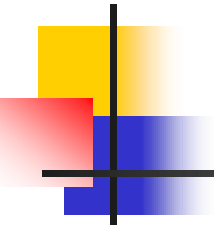




FPGAs & CPLDs

Programmable Logic Devices (PLDs)

CPLDs and FPGAs

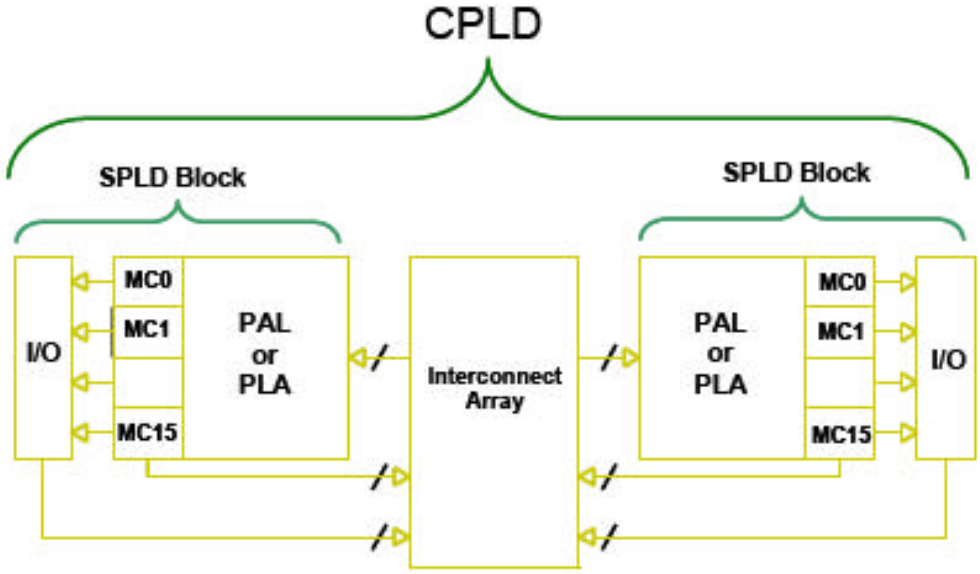


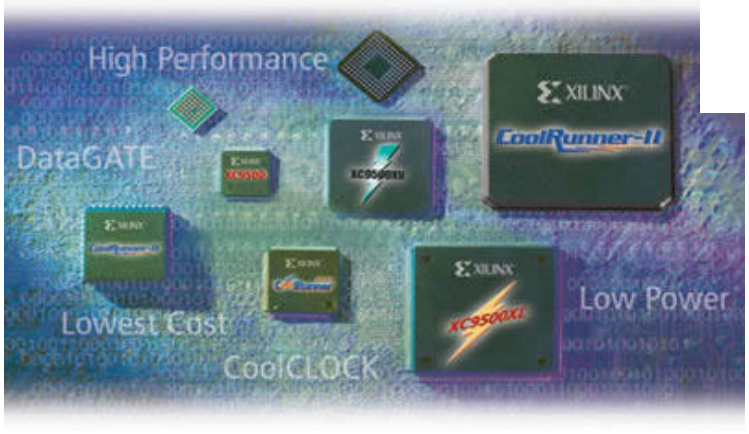
FPGAs & CPLDs

- Altera introduced first CPLD device.
- Complex programmable logic devices (CPLDs) extend the density of SPLDs.
- The concept is to have a few PLD blocks or macrocells on a single device with a general-purpose interconnect in-between. Simple logic paths can be implemented within a single block.

FPGAs & CPLDs

CPLD Architecture





FPGAs & CPLDs

- **Ease of Design:** CPLDs offer the simplest way to implement a design. Once a design has been described, by schematic and/or HDL entry, you simply use CPLD development tools to optimize, fit, and simulate the design.

- **Lower Development Costs:** CPLDs offer very low development costs. Because CPLDs are re-programmable, you can easily and very inexpensively change, optimize and improve your designs.

FPGAs & CPLDs

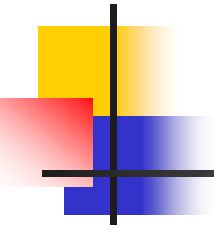
- **More Product Revenue:** CPLDs offer very short development cycles, which means your products get to market quicker and begin generating revenue sooner.

- **Reduced Board Area:** CPLDs offer a high level of integration (that is, a large number of system gates per area) and are available in very small form factor packages.

FPGAs & CPLDs

- An MPGA (Mask Programmable Gate Array) consists of an array of prefabricated transistors customized for the user's logic circuit by means of wire connections.

- Because the silicon foundry performs customization during chip fabrication, the manufacturing time is long, and the user's setup cost is high.



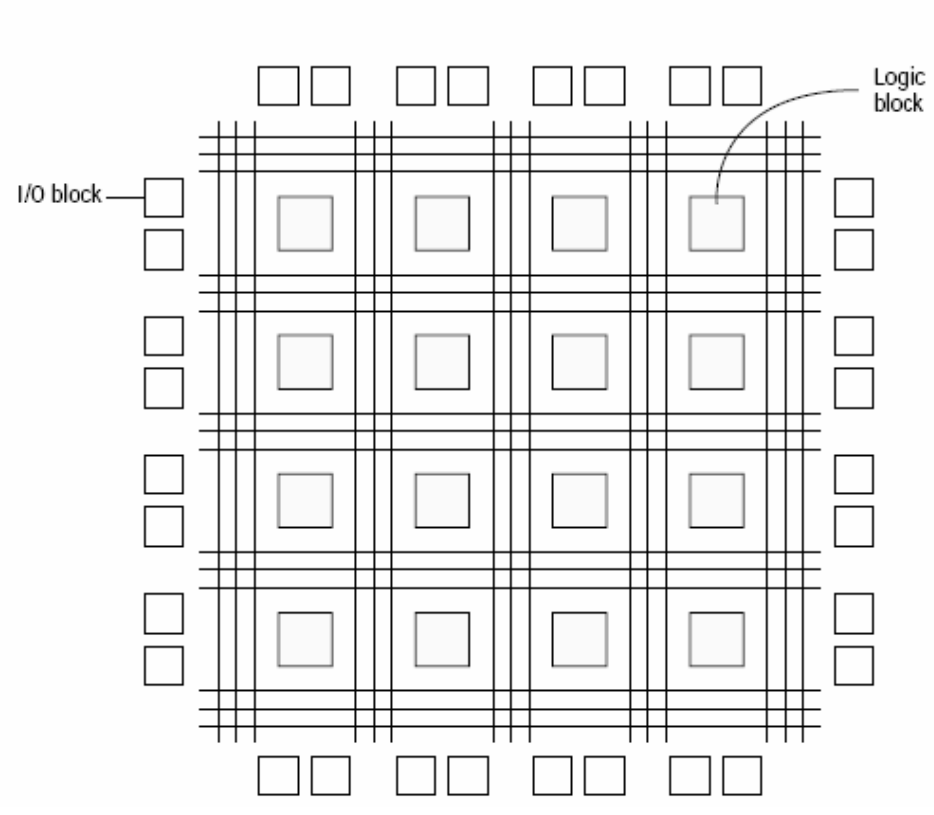
FPGAs & CPLDs

- An FPGA is a regular structure of logic cells (or modules) and interconnect, which is under your complete control. This means that you can design, program, and make changes to your circuit whenever you wish.

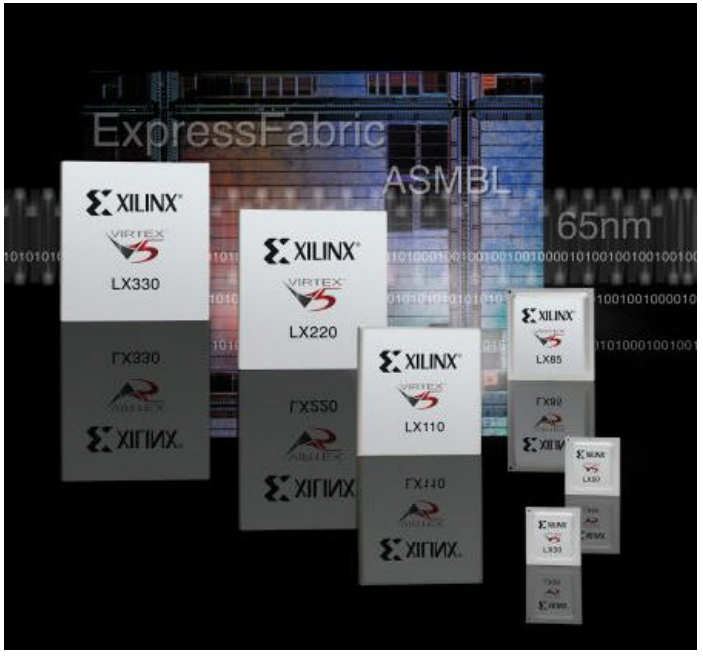
- In 1985 Xilinx introduced first FPGA.

- Now FPGAs exceed 10 million gate limit. (Here gate is equivalent to two input AND gate)

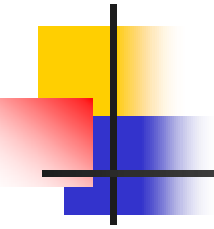
FPGAs & CPLDs



FPGA Architecture



Xilinx Virtex 5
550MHz Global Clock Speed

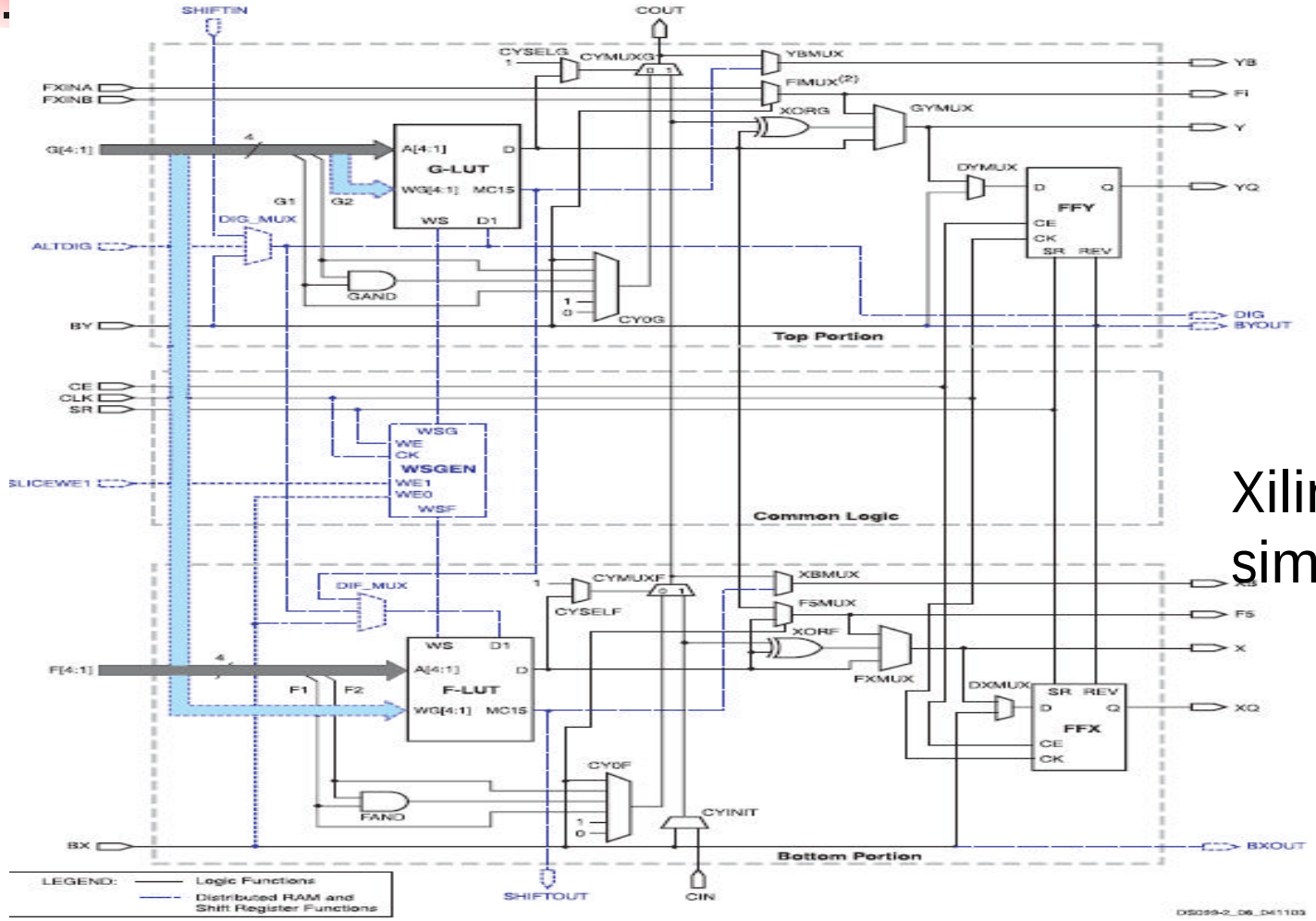


FPGAs & CPLDs

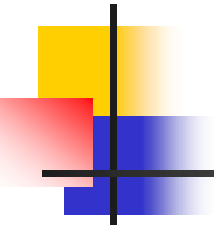
- FPGAs contain Configurable Logic Blocks (CLBs) and IO Blocks(IOBs).

- CLBs contain main logic resource for implementing synchronous as well as combinational circuits.

FPGAs & CPLDs



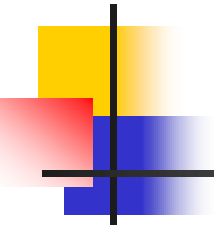
Xilinx XC3S200 simplified CLB



FPGAs & CPLDs

- There are two basic types of FPGAs: SRAM-based reprogrammable and OTP (One Time Programmable).

- These two types of FPGAs differ in the implementation of the logic cell and the mechanism used to make connections in the device.



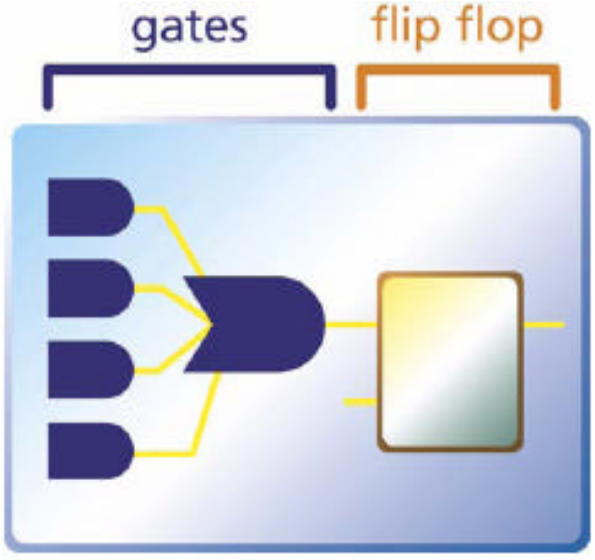
FPGAs & CPLDs

- The dominant type of FPGA is SRAM-based and can be reprogrammed as often as you choose.

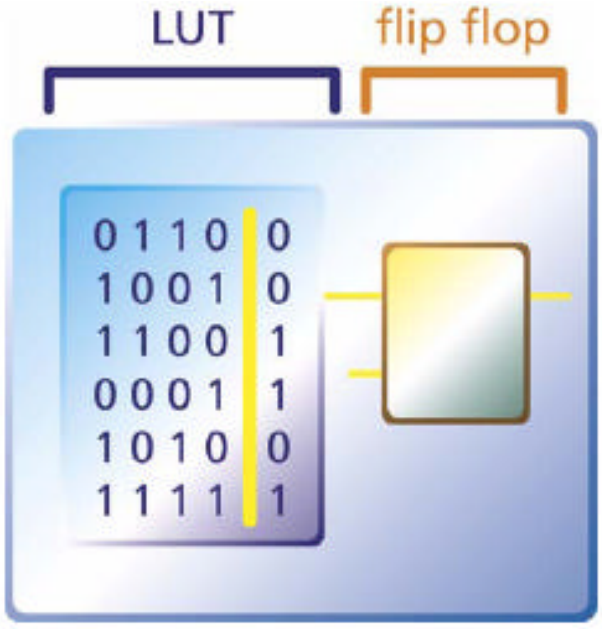
- In fact, an SRAM FPGA is reprogrammed every time it's powered up, because the FPGA is really a fancy memory chip. That's why you need a serial PROM or system memory with every SRAM FPGA.

FPGAs & CPLDs

- In the SRAM logic cell, instead of conventional gates, an LUT determines the output based on the values of the inputs.



OTP Logic Cell



SRAM Logic Cell

FPGAs & CPLDs

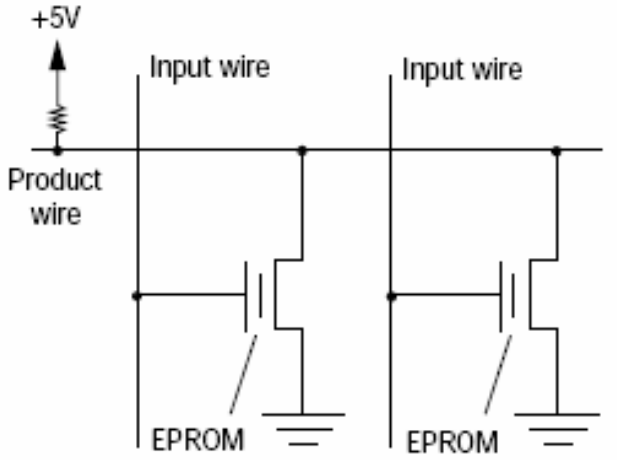
- OTP FPGAs use anti-fuses (contrary to fuses, connections are made, not “blown,” during programming) to make permanent connections in the chip.
- OTP FPGAs do not require PROM or other means to download the program to the FPGA.
- However, every time you make a design change, you must throw away the chip! The OTP logic cell is very similar to PLDs, with dedicated gates and flip-flops.

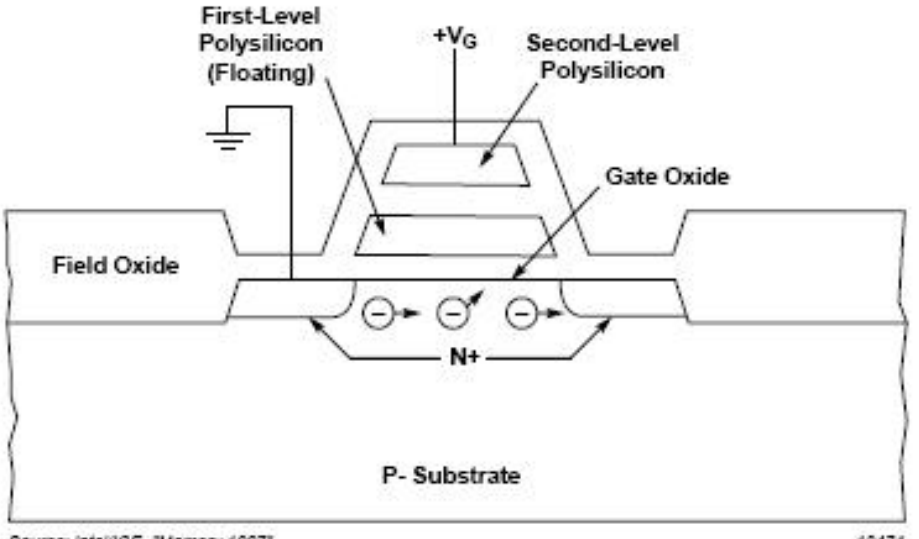
User Programmable Switch Technologies

- The first user-programmable switch developed was the fuse used in PLAs.
- For CPLDs, the main switch technologies are floating gate transistors like those used in EPROM (erasable programmable read-only memory) and EEPROM (electrically erasable PROM).
- For FPGAs, they are SRAM (static RAM) and antifuse.

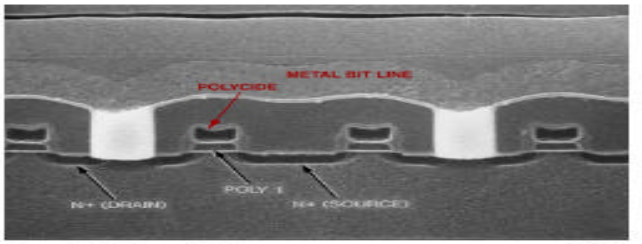
User Programmable Switch Technologies

Switch type	Reprogrammable?	Volatile?	Technology
Fuse	No	No	Bipolar
EPROM	Yes (out of circuit)	No	UVCMOS
EEPROM	Yes (in circuit)	No	EECMOS
SRAM	Yes (in circuit)	Yes	CMOS
Antifuse	No	No	CMOS+

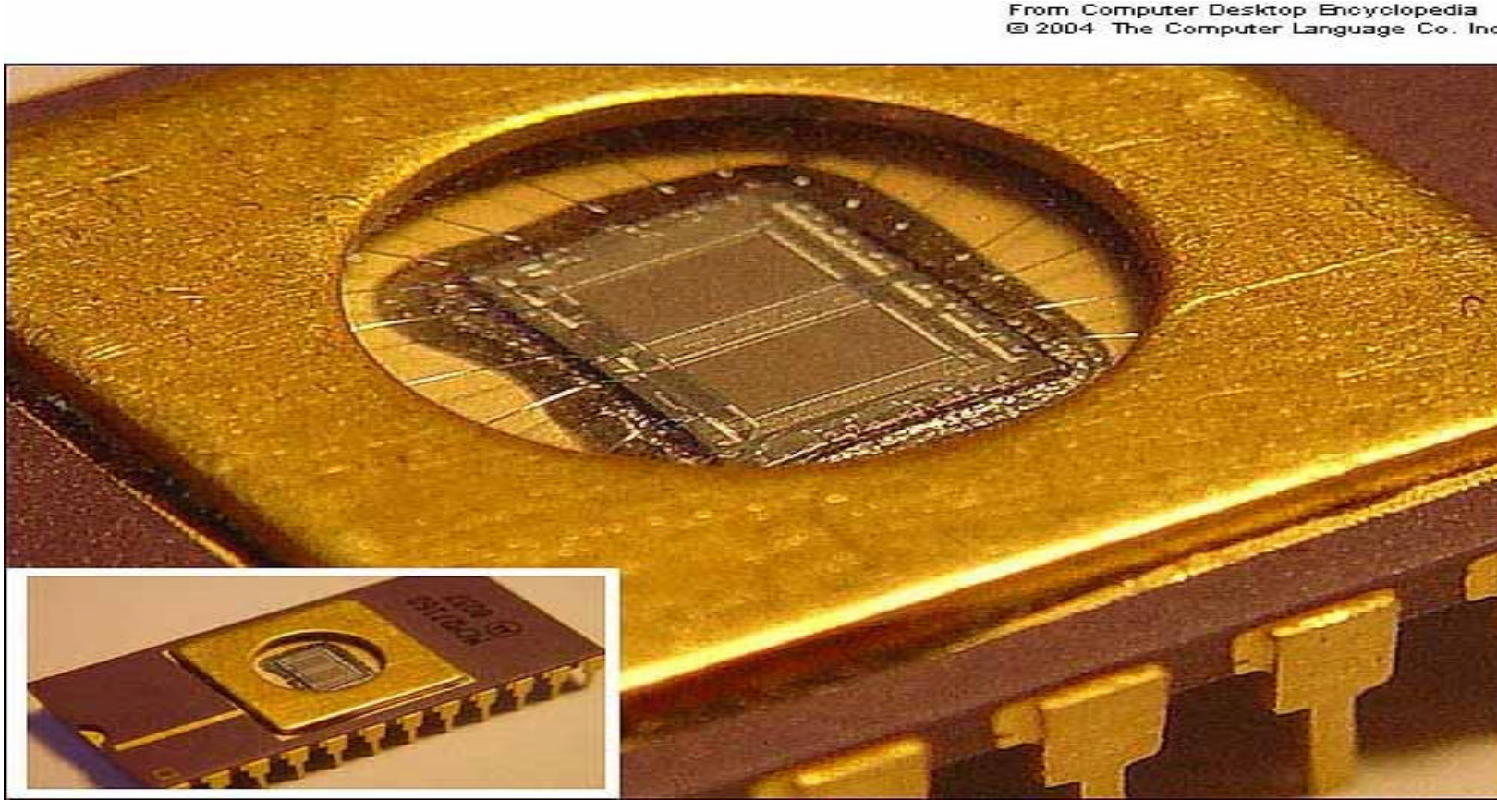




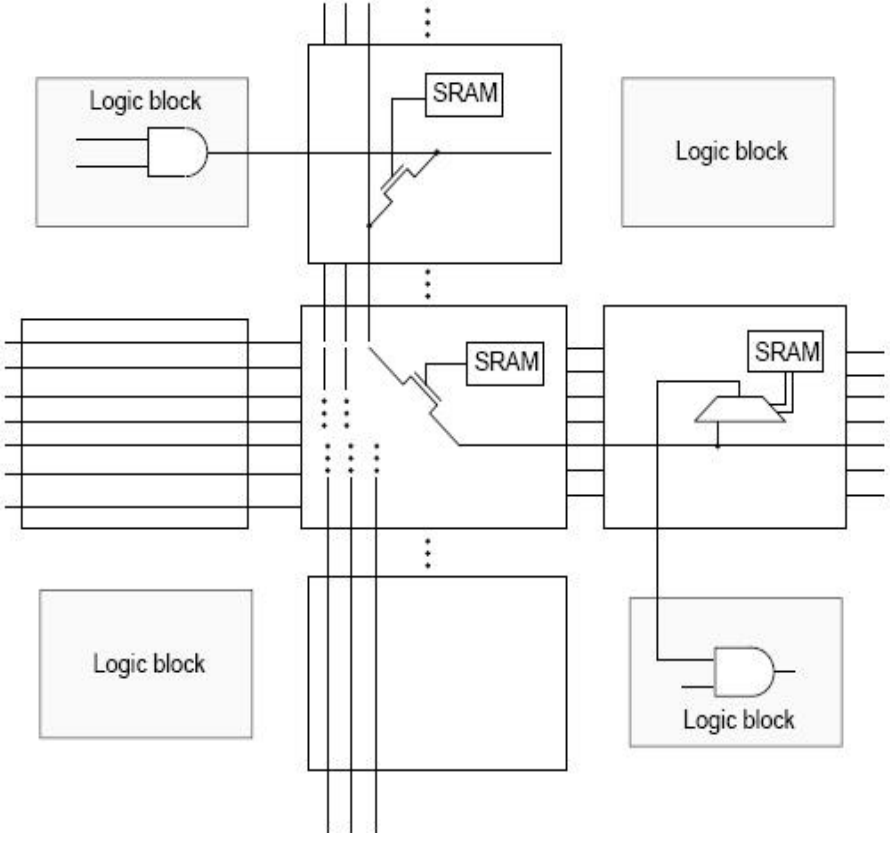
EPROM Programmable Switches



User Programmable Switch Technologies



User Programmable Switch Technologies



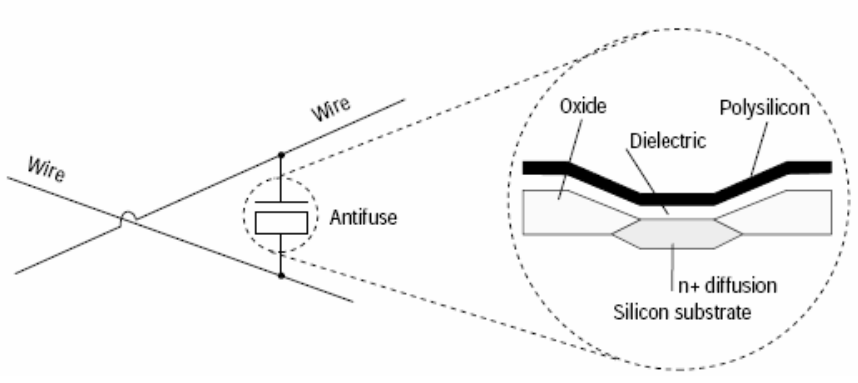
SRAM Controlled Programmable Switche

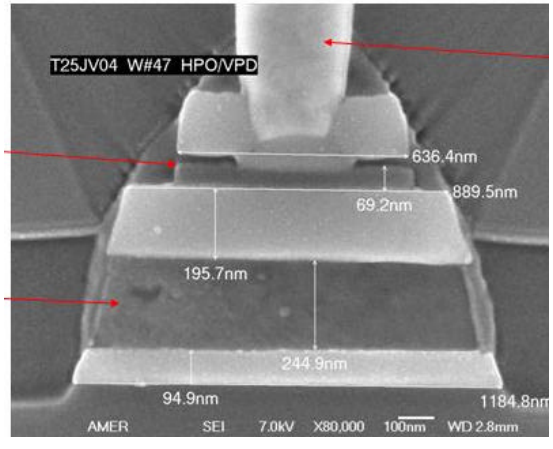
User Programmable Switch Technologies

- Antifuses are originally open circuits that take on low resistance only when programmed. Antifuses are manufactured using modified CMOS technology.

- Unprogrammed, the insulator isolates the top and bottom layers; programmed, the insulator becomes a low-resistance link.

User Programmable Switch Technologies





Antifuse Structure