3.7 Test structures:

In this section, test structures designed to characterise DCELL will be presented.

1. To measure process parameters, test block T1 containing 2 NMOS and 2 PMOS transistors was designed. Channel length and channel width of test transistors can be seen in Table 3.6.

Table 3.6 : Channel length and channel width of test transistors

Transistors	W (um)	L (um)	Type
M1	5.5	5.5	NMOS
M2	10	0.6	NMOS
M3	16.5	5.5	PMOS
M4	1	5	PMOS

2. To measure the effect of input capacitors mismatch on the behaviour of DCELL, 3 test blocks T2, T3, T4 were designed. Each of them contains a DCELL block with different input capacitance. The input capacitance of DCELL in block T2, T3 and T4 are 10fF, 15fF and 20fF respectively.

3. To measure the effect of charge injection from the channel of transistors M3 and M4 to nodes N1 and N2 respectively, 2 test block T5 and T6 were designed. These are simple DCELL blocks that have different M3 and M4 transistors' channel area. The channel area of T5's transistors M3 and M4 is $1um^2$. The channel area of T6's transistors M3 and M4 is $4um^2$.

4. To measure the poly layer sheet resistance, test block T7 was designed. T7 contains a single poly path of length 400um and width 0.6um.

5. To measure drain current mismatch of output transistor couple M1 and M2 in DCELL, 3 test block T8, T9 and T10 were designed. The channel length and area of transistor couples in the test blocks can be seen in Table 3.7.

Table 3.7 : Channel length and area of transistor couples in the test blocks

Test Block	Channel Length (um)	Channel area (um^2)
T8	5	5
T9	5	10
T10	5	25

6. To measure the DCELL's speed and the effect of refresh time on the behavior of DCELL, test block T11 was designed. T11 is constituted by the first 2 DCELL row of system DCELL matrix. Thus, it contains a DCELL matrix of size 2x18.Each row is ended by a ROW_AMP block. To measure the speed of DCELL a simple current comparator is designed. The schematic view of current comparator can be seen in Figure 3.83.

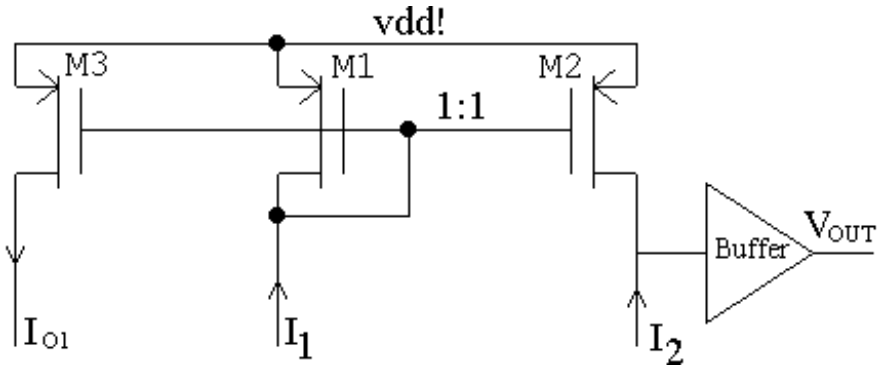

Figure 3.83 : The schematic view of current comparator.

In Figure 3.83, I_I represents the output current of ROW_AMP of row i. Transistor M3 is added to measure the effect of refresh time. The procedure to measure it is as follows:

a) $T_{ij} = \begin{cases} 0 & i \neq 1, j \neq 1 \\ 2.5 & i = 1, j = 1 \end{cases}$

b) The variation of DCELL terminal $V_{IN+(1)}$ can be seen in Figure 3.84

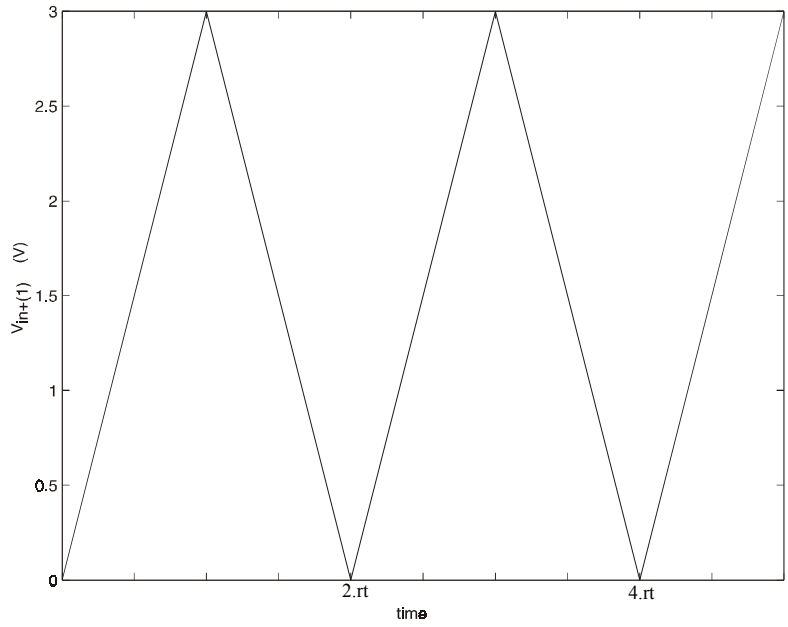

Figure 3.84 : The variation of DCELL terminals $V_{IN+(1)}$

In Figure 3.84 rt represents the refresh time.

c) We change the refresh time with the aid of uP_Interface block, then we measure and compare the drain current of transistor M3 for every different refresh time setting.