A PROGRAMMABLE CMOS ANALOG VECTOR QUANTIZER CHIP

SUMMARY

The basis of the quantization idea has a long history since 1898. The historical story of the quantizers and an important part of the related references can be found in the article title 'Quantization' of Robert M. GRAY and David L. NEUHOFF.

In the information theory, the quantization is generally considered as a method of signal compression. The goal of quantization is to encode the data from a source that is characterized by its probability density function with as minimum rate as possible in such a way that reproducing may be recovered from the bits as high quality as possible.

We can classify quantizers into two different sub-categories with respect to their input vector size. If the input vector space is one dimensional, the quantizer is classified as 'Scalar quantizer'; otherwise it is classified as 'Vector Quantizer'.

In recent years, there has been much interest focused on Vector Quantization. The main cause of this trend is: According to Shannon's rate-distortion theory, a better performance is always achievable in theory by coding a block of signal (vector) instead of coding each signal individually (scalar).

Vector quantization is a mapping Q from m dimensional vector space R^m into a finite subset T of R^m ($T \subset R^m$). It is denoted by

$$Q : R^m \rightarrow T$$

T is the set of reproduction vectors and it is called template-book (code-book) for the vector quantizer. For every input vector **X**, a template-word $\mathbf{t_i}$ is selected as the representation for **X**. This process is called quantization phase (or the template-book search phase) of the Vector Quantizer. It is denoted by

$Q(\mathbf{X}) = t_i$

Then the code word $\mathbf{t_j}$ is represented by some symbols (normally the address of the template-vector in the template-book). This is called the encoding phase of the Vector Quantizer. The first phase is an classification, and the second one is an encoding.

The problem of designing a VQ system is constituted by 2 part. First part of the problem concern to design an 'optimal' template-book for a given probability density function of input vector space in order to minimize average distortion in replacing any input vector by the closest template-vector. This part of the problem is the subject of Information Theory. The second part of the problem, which concerns the subject of this thesis, is to implement Vector Quantizer System for a given template-book. The schematic view of implemented VQ system can be seen in figure below.

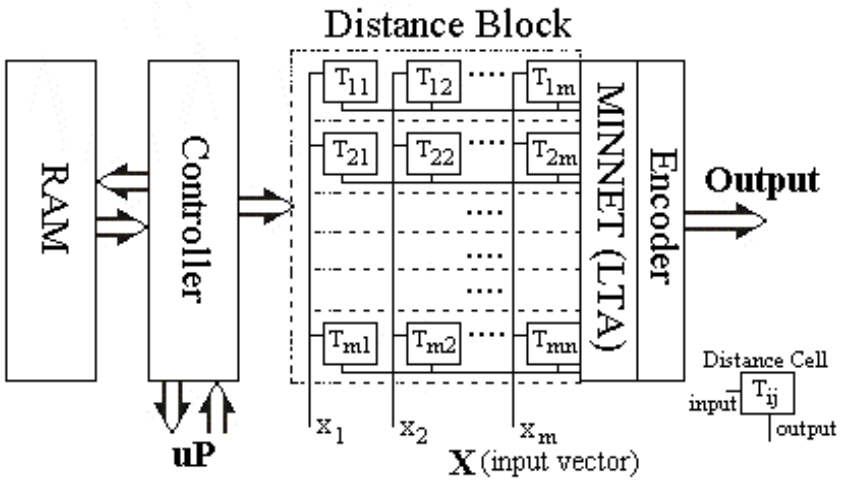

Figure 1: Block Schematic of the VQ system

In the schematic, The first part of the system consists of 'Distance block' and 'MINNET block' (Loser-Takes-All). The second part of the system consists of 'The Encoder block'.

The block Distance contains the Distance Cell (DCELL) matrix. The number of DCELL in each row is equal to the input vector dimension. And the number of the matrix row is equal to the number of template-vector in code-book. Each row stores related template-vector, and measures the Euclidean distance between the input vector and stored template-vector. The schematic view of the DCELL can be seen in figure below. The input signal of the circuit is voltage and the output signal is current. The template-vector is stored dynamically. The silicon area consumption of the cell is x 13.6μm.

The block MINNET, in Figure 1, is a circuit selecting the minimum one among its input signals. This is a famous Loser-Takes-All circuit. In the literature, there are many different circuit topologies. Every topology has its own advantages and disadvantages. In the VQ system, the block ROW_WTA realizes it. The schematic view of the block can be seen in Figure 3. Circuit subtracts the input current from a constant bias current being unconditionally greater than the input current and applies this difference current to the input of a current based Winner-Takes-All circuit of J. Lazarro. As the bias current is unconditionally greater than the input current, it is maximum when the measured distance is minimum. It consumes considerably small

silicon area. WTA part of the circuit may pose resolution problem. Therefore, different WTA topologies must be considered for high performance applications.

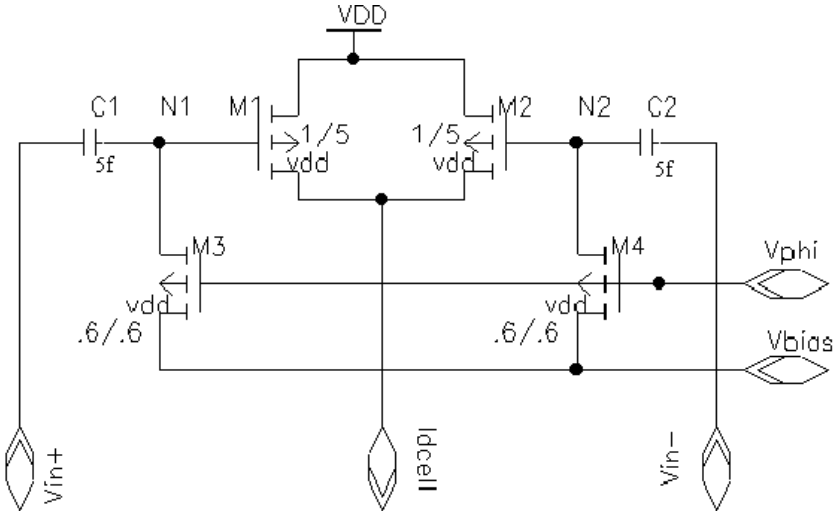

Figure 2: The schematic view of the Distance Cell

The block ENCODER is coding the selected template-vector's index in the code-book. In the system, a simple circuit showing the address in the code-book realizes it. It is optimal if all of the template-vector have the same probability.

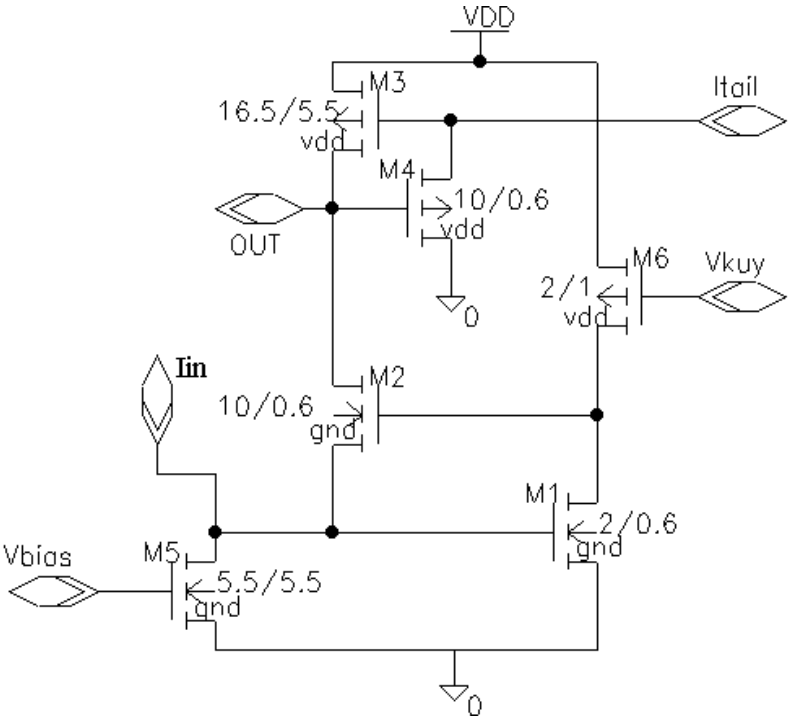

Figure 3 The schematic view of the block ROW_WTA

The block RAM stores the content of the code-book. As the template-vectors are stored dynamically in the Distance matrix, RAM block is used during the refresh phase. As we can easily remark from the system layout, RAM block consumes more

than 60% of the silicon area. The block Controller is responsible of the reading and writing operation to the Distance and RAM blocks. This is a simple digital block.

In the VQ system, there are two other block not showed in the system schematic but needed due to the analog structure of the system. They are input amplifier block IN_AMP and the digital to analog converter block DAC6. These blocks may determine the resolution and the speed of the system.

The design procedure of the all of the blocks is examined in detail in the thesis. Let me now briefly explain the working principles and the floorplan of the system.

Code-book is stored in the RAM block. The number of word is equal to the number of template-vector in the code-book. The word length of the block is equal to the multiple of the input vector size with the resolution of the one vector element (m). The resolution of the DAC is also equal to the resolution of the one vector element. The output buses of the RAM block are connected to the DAC blocks to constitute one of the template vector elements.

The number of row in the Distance matrix is equal to the number of template-vector. Each row stores its template-vector. The number of the colon in the Distance matrix is equal to the input vector size. Input vectors are applied to the Distance matrix from its colon inputs. Therefore, the distance cells on the same colon have the same input vector. Obviously, if the stored template-vector elements are different, their output will be different. As mentioned previously, the template-vectors are stored dynamically in the Distance matrix. Thus, we need to refresh them. During the refresh period, template-vector elements are applied from the colon input of the matrix too. For that reason, each row of the matrix must be activated for refresh operation sequentially.

The block IN_AMP drives matrix colon inputs because distance cell needs the input and its inverse at the same time for proper operation. Obviously, we must use one IN_AMP block for every colon of the matrix. The block has 2 inputs. During the operation phase, block accepts the input vector, whereas during the refresh phase, it accepts DAC block output.

Refresh phase can be summarized as follows: At the end of a time determined by the microprocessor, the block Controller starts to send the control signals to the RAM. Thus the template-vectors starts to appear at the output of the DAC blocks. During this phase, the block IN_AMP process the DAC output. And finally, all of matrix rows are activated sequentially for writing template-vectors when their template-vector appears at the colons of the matrix.

During the operation phase, colon signals change with the input signals. Therefore, row’s output changes, winner template changes and encoded index changes.

The structure of the system permits to adapt it to the Kohonen Self-Organizing Feature Map. We must simply post-process the system outputs and update the code-book.

The layout of the system can be found in the thesis. It contains 79 bonding pads. They are:

6 digital output pads for the Encoder block.

20 analog pad for input vectors.

8 analog pad for biasing.

8 bi-directional digital pad for microprocessor data bus.

10 digital input pad for microprocessor address bus.

3 digital input pad for microprocessor control signals.

2 digital input pad for system clock and reset.

4 couple of analog and 7 couple of digital power pads.

The total silicon area of the system including bonding pads is 4.1mm x 3.7mm (15.17 mm^2).