3.2 Row Amplifier (ROW_AMP)

In the previous section, I have found out the biasing condition of DCELL's transistors M1 and M2. Then, I need an analog block whose output signal (current) is a function of the input current (DCELL row's output current), while keeping the input node voltage at a constant level satisfying biasing condition. In this section, I will analyze in detail this analog block named ROW_AMP.

Each row of the DCELL matrix must contain one ROW_AMP block. The output currents of the blocks are the input signals of the classifier network determining the closest template-vector to the input vector. In order to utilize a Winner-Takes-All (WTA) network as a classifier, the output current of the block ROW_AMP must be maximum when the input current, distance, is minimum. Obviously, it must be minimum when the input current is maximum. This can be realized by simply subtracting the input current from a constant bias current I_B. The bias current I_B must be unconditionally greater than the input current.

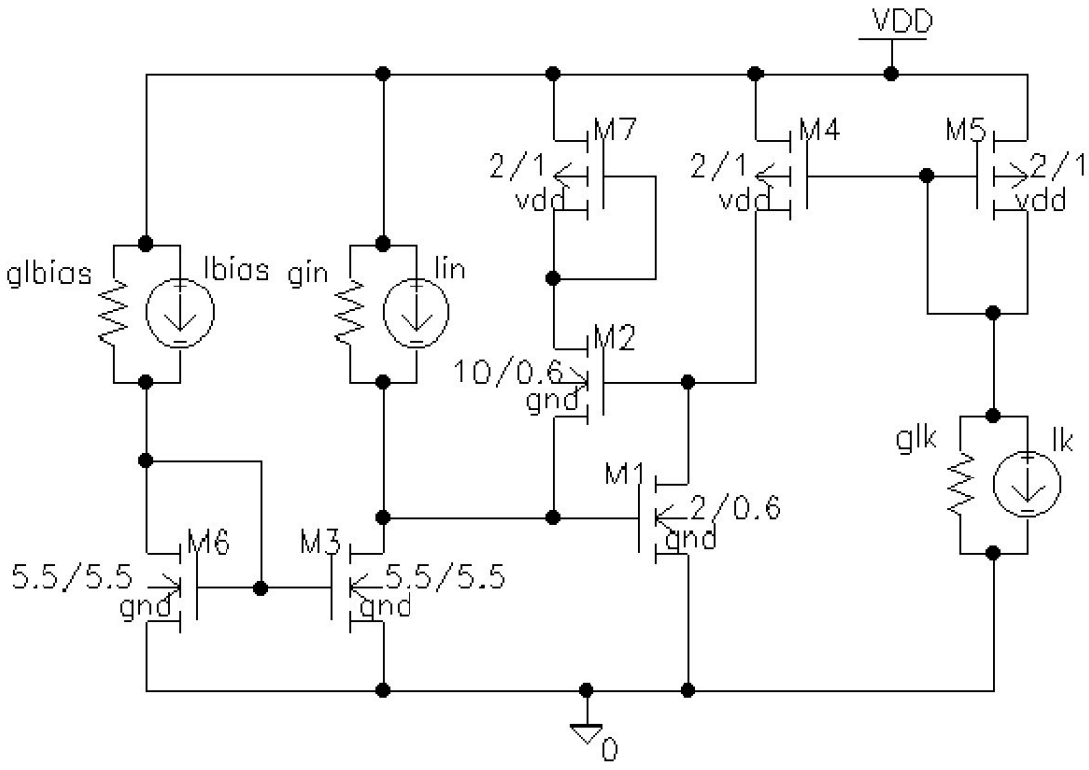

Figure 3.2-1 Schematic view of ROW_AMP and its bias circuits

The schematic view of the proposed ROW_AMP block and its bias circuits can be seen in Figure3.2.1. Thus, equations of definition of the block ROW_AMP are as follows:

$$\begin{aligned} V_{IN} &= V_{REF} \\ I_{OUT} &= I_B - I_{IN} \end{aligned} \qquad 3.2.1$$

Operation principle of ROW_AMP block can be explained as follows:

Transistors M1 and M2 form a regulated cascode structure. In this way, transistor M1, biased by transistor M4, keeps input terminal voltage at $V_{TN(M1)}$+gate over drive constant level. Transistor M3 flows the constant bias current I_B (or I_{BIAS}). As the drain voltage of this transistor is constant, there is no channel length modulation. With respect to KIRCHOFF current law, transistor M2 flows the output current being equal to (I_B - I_{IN}). As mentioned above, for a proper operation I_B must be unconditionally greater than I_{IN}.

Assuming that

$$\beta_3 = \beta_6, \quad \beta_4 = \beta_5, \quad V_{TN(M6)} = V_{TN(M3)} = V_{TN(M2)} = V_{TN(M1)} = V_{TN}$$

$$I_{IN} = 0, \quad V_{TP(M7)} = V_{TP(M4)} = V_{TP(M5)} = V_{TP} \qquad 3.2.2$$

DC node voltages of ROW_AMP can be expressed as follows

$$V_{IN} = \sqrt{\frac{2I_K}{\beta_1}} + V_{TN} \qquad 3.2.3$$

$$V_A = \sqrt{\frac{2I_B}{\beta_2}} + \sqrt{\frac{2I_K}{\beta_1}} + 2V_{TN} \qquad 3.2.4$$

$$V_O = -\sqrt{\frac{2I_B}{\beta_7}} + V_{DD} + V_{TP} \qquad 3.2.5$$

Input voltage level V_{IN} is equal to 770.2mV. Transistor M3 must operate in saturation region. Thus, during the determination of its aspect ratio, input voltage

level must taken into account. Let me now calculate small signal parameters of the block ROW_AMP. Its small signal equivalent circuit can be seen in Figure3.2.2.

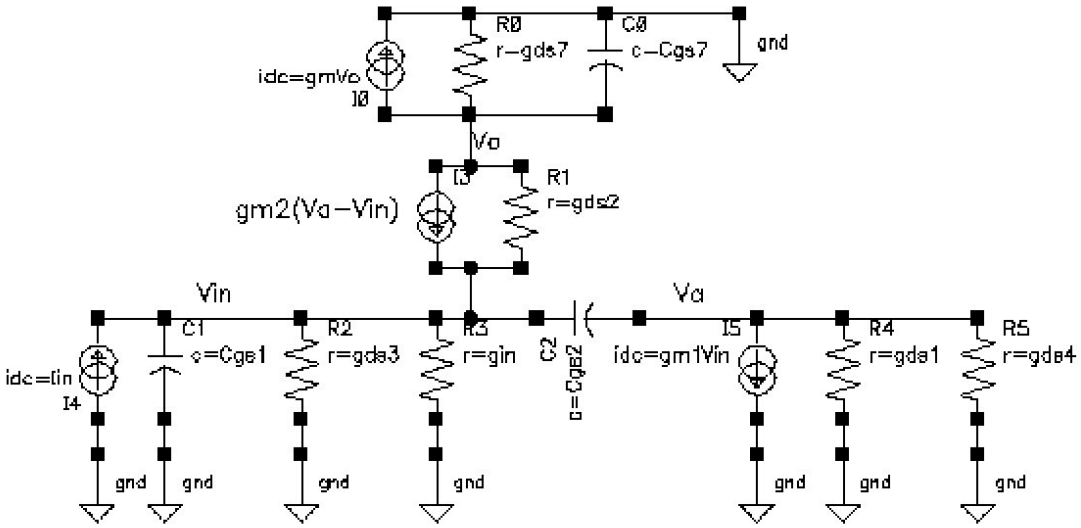

Figure 3.2-2 : Small Signal equivalent circuit of ROW_AMP.

Node equations of the circuit are

$$
\begin{aligned}
&1)\ I_O = -(gm_7 + gds_7 + sC_{GS7})V_O \\
&2)\ I_O = gm_2(V_A - V_{IN}) + gds_2(V_O - V_{IN}) \\
&3)\ I_O + I_{IN} = (sC_{GS1} + g_{IN} + gds_3)V_{IN} + sC_{GS2}(V_{IN} - V_A) \\
&4)\ sC_{GS2}(V_{IN} - V_A) = gm_1 V_{IN} + (gds_1 + gds_4)V_A
\end{aligned}
\qquad 3.2.6
$$

Thus, with respect to (3.2.6), the small signal current gain of the block ROW_AMP can be expressed as follows:

$$
\frac{I_O}{I_{IN}} = \frac{-(sC_{GS7} + gm_7 + gds_7)[gds_2 C_{GS2} s + gm_1 gm_2 + (gm_2 + gds_2)(gds_1 + gds_4)]}{(C_{GS7} s + gm_7 + gds_7 + gds_2)[C_{GS1} C_{GS2} s^2 + [C_{GS2}(g_{IN} + gds_3 + gds_1 + gds_4 + gm_1)}
$$

$$
\frac{}{+ C_{GS1}(gds_1 + gds_4)]s + (g_{IN} + gds_3)(gds_1 + gds_4)] + (C_{GS7} s + gm_7 + gds7)}
$$

$$
\frac{}{[gds_2 C_{GS2} s + gm_1 gm_2 + (gm_2 + gds_2)(gds_1 + gds_4)]}
$$

3.2.7

With a straightforward simplification, we can show that the DC current gain is equal to 1. Small signal output resistance of the block ROW_AMP is function of the input current. It reaches its minimum value when the input current is equal to 0.

Minimum small signal output resistance of the block can be expressed as follows:

$$R_{O\min} = \left.\frac{V_O}{I_O}\right|_{I_{IN}=0} = \frac{C_{GS1}C_{GS2}s^2 + \left[C_{GS2}\left(gds_4 + gds_3 + gds_2 + gds_1 + gm_1 + g_{IN}\right) + \right.}{gds_2\left[C_{GS1}C_{GS2}s^2 + \left[C_{GS2}\left(gds_4 + gds_3 + gds_2 + gds_1 + gm_1 + g_{IN}\right) + \right.\right.}$$

$$\frac{\left.C_{GS1}\left(gds_1 + gds_4\right)\right]s + gm_1gm_2 + \left(gds_1 + gds_4\right)\left(gm_2 + gds_3 + gds_2 + g_{IN}\right)}{\left.\left.C_{GS1}\left(gds_1 + gds_4\right)\right]s + \left(gds_3 + g_{IN}\right)\left(gds_4 + gds_1\right)\right]} \qquad 3.2.8$$

With some simplification, DC R_{Omin} can be denoted as follows

$$R_{O\min}\big|_{s=0} = R_{IN}.gm_1ro_1gm_2ro_2 \qquad 3.2.9$$

where R_{IN} is equal to $(gds_3+g_{IN})^{-1}$. We can easily remark that output resistance is a product of intrinsic gain of 2 transistors forming regulated-cascode structure. Small signal input resistance of the block ROW_AMP can be expressed as follows:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{\left(C_{GS7}s + gm_7 + gds_7 + gds_2\right)\left(C_{GS2}s + gds_1 + gds_4\right)}{\left(C_{GS7}s + gm_7 + gds_7 + gds_2\right)\left[C_{GS1}C_{GS2}s^2 + \left[C_{GS2}\left(g_{IN} + gds_3 + gds_1 + gds_4 + gm_1\right) + \right.\right.}$$

$$\left.\left.C_{GS1}\left(gds_1 + gds_4\right)\right]s + \left(g_{IN} + gds_3\right)\left(gds_1 + gds_4\right)\right] + \left(C_{GS7}s + gm_7 + gds_7\right)\left[C_{GS2}gds_2s + \right.$$

$$\left.gm_1gm_2 + \left(gm_2 + gds_2\right)\left(gds_1 + gds_4\right)\right] \qquad 3.2.10$$

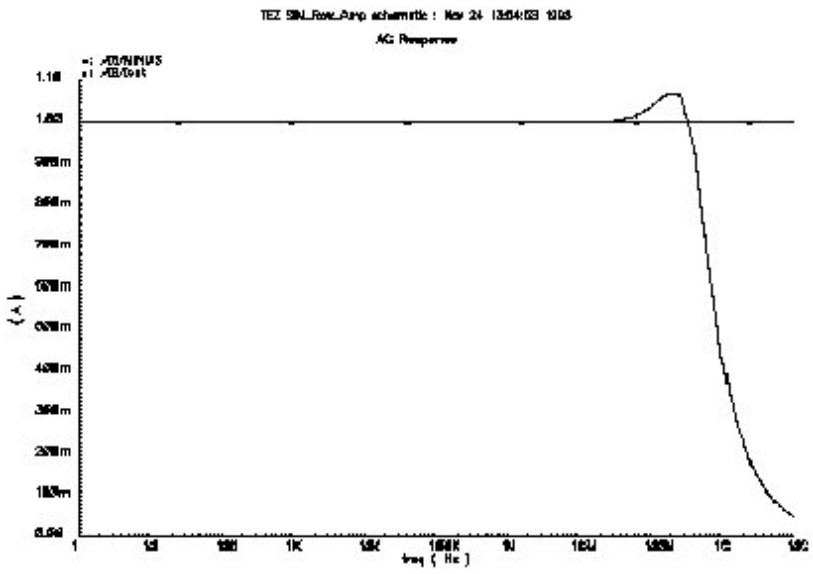

Figure 3.2-3: Small signal current gain of ROW_AMP

Simulated small signal current gain of ROW_AMP can be seen in Figure3.2.3. Increasing bias current I_B or decreasing I_K can prevent the peak on the gain characteristic. The stability condition of the block will be analyzed later in section 3.3 ROW_WTA.

Simulated small signal input resistance of the block ROW_AMP can be seen in Figure3.2.4.

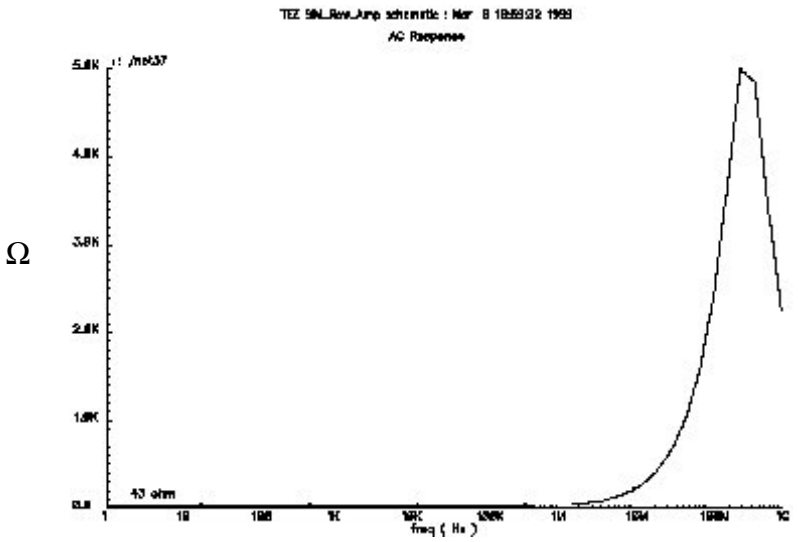

Figure 3.2-4Small signal input resistance of ROW_AMP

Simulated small signal output resistance of the block ROW_AMP can be seen in Figure3.2.5.

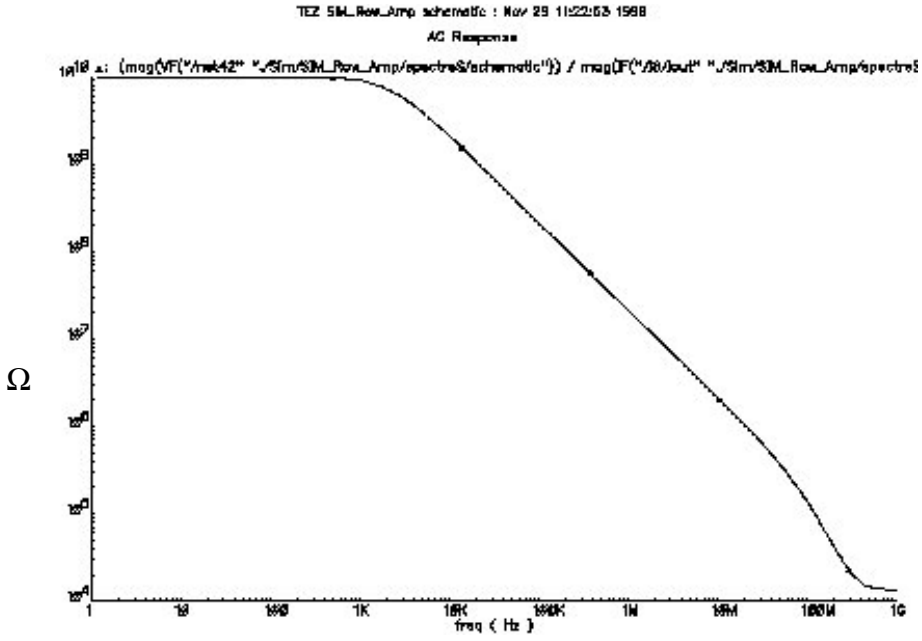

Figure 3.2-5 Small signal output resistance of ROW_AMP

I now continue my analysis by calculating of the transfer functions $\frac{I_O}{V_{DD}}$ and $\frac{I_O}{gnd}$ giving the measure of the effect of the noise introduced through the power rails. Small signal equivalent circuit of ROW_AMP used for calculating the transfer functions can be seen in Figure3.2.6.

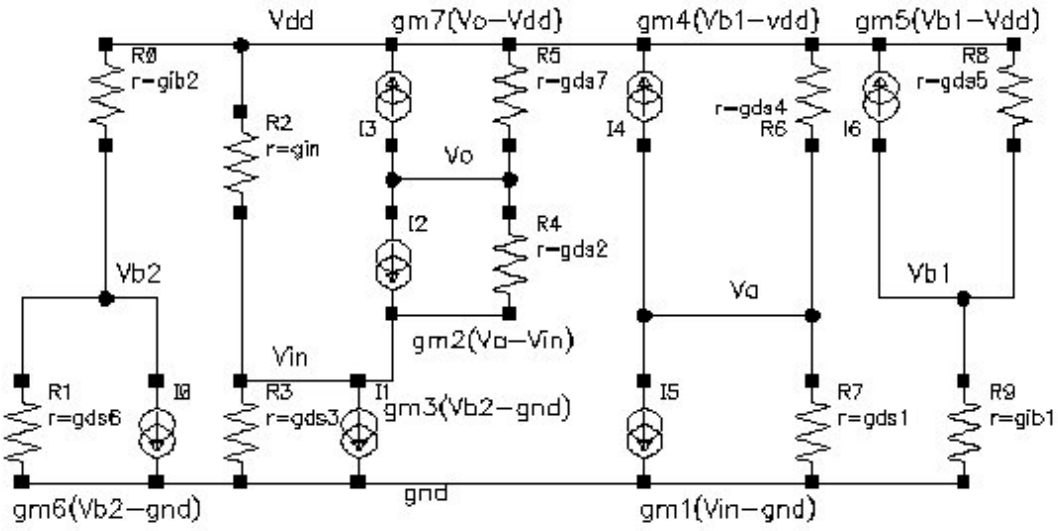

Figure 3.2-6 Small signal equivalent circuit of ROW_AMP for power rail noise effects.

Node equations of the circuit in Figure3.2.9 are

$$
\begin{aligned}
&1)\ g_{Ib2}(V_{DD}-V_{b2}) = gm_6(V_{b2}-gnd)+gsd_6(V_{b2}-gnd)\\
&2)\ -gm_5(V_{b1}-V_{DD})+gds_5(V_{DD}-V_{b1}) = g_{Ib1}(V_{b1}-gnd)\\
&3)\ -gm_4(V_{b1}-V_{DD})+gds_4(V_{DD}-V_A) = gm_1(V_{IN}-gnd)+gds_1(V_A-gnd)\\
&4)\ g_{IN}(V_{DD}-V_{IN})+gm_2(V_A-V_{IN})+gds_2(V_O-V_{IN}) = gm_3(V_{b2}-gnd)+gds_3(V_{IN}-gnd)\\
&5)\ -gm_7(V_O-V_{DD})+gds_7(V_{DD}-V_O) = gm_2(V_A-V_{IN})+gds_2(V_O-V_{IN})\\
&6)\ I_O = -gm_7(V_O-V_{DD})+gds_7(V_{DD}-V_O)
\end{aligned}
\qquad 3.2.11
$$

Thus, with respect to (3.2.11), DC output current can be expressed as follows:

$$I_O = \frac{(gm_7 + gds_7)[gm_1 gm_2 + (gm_2 + gds_2)(gds_1 + gds_4)]}{(gm_7 + gds_7)[gm_1 gm_2 + (gm_2 + gds_2)(gds_1 + gds_4)] + (gds_1 + gds_4)(gds_3 + g_{IN})}$$
$$\frac{}{(gds_7 + gds_2 + gm_7)}\left[\frac{gm_3 g_{Ib2} - g_{IN}(g_{Ib2} + gm_6 + gds_6)}{g_{Ib2} + gm_6 + gds_6} V_{DD}\right.$$
$$- \frac{gds_3(g_{Ib2} + gm_6 + gds_6) + gm_3 g_{Ib2}}{g_{Ib2} + gm_6 + gds_6} \text{gnd}$$
$$+ \frac{(gds_3 + g_{IN})[(g_{Ib1} + gm_5 + gds_5)(gm_2 gds_4 + gds_2(gds_1 + gds_4)) + gm_4 g_{Ib1}]}{(g_{Ib1} + gm_5 + gds_5)[gm_1 gm_2 + (gds_1 + gds_4)(gm_2 + gds_2)]} V_{DD}$$
$$\left. + \frac{gm_2(gds_3 + g_{IN})[(g_{Ib1} + gm_5 + gds_5)(gm_1 + gds_1) + gm_4 g_{Ib1}]}{(g_{Ib1} + gm_5 + gds_5)[gm_1 gm_2 + (gds_1 + gds_4)(gm_2 + gds_2)]} \text{gnd} \right]$$

3.2.12

The variation of the output current with respect to the noise introduced through V_{DD} rail can be seen in Figure3.2.7. The curve family in the Figure 3.2.7 is obtained by varying the output resistance of the current sources. For the curve gidc="500K";/I8/Iout, the output resistance of all of the current sources is 500 kΩ. The output resistances selected to plot the curve family are 500 kΩ, 2.924 MΩ, 17.1 MΩ and 100 MΩ. Typical value of the variation is below –105 dB.

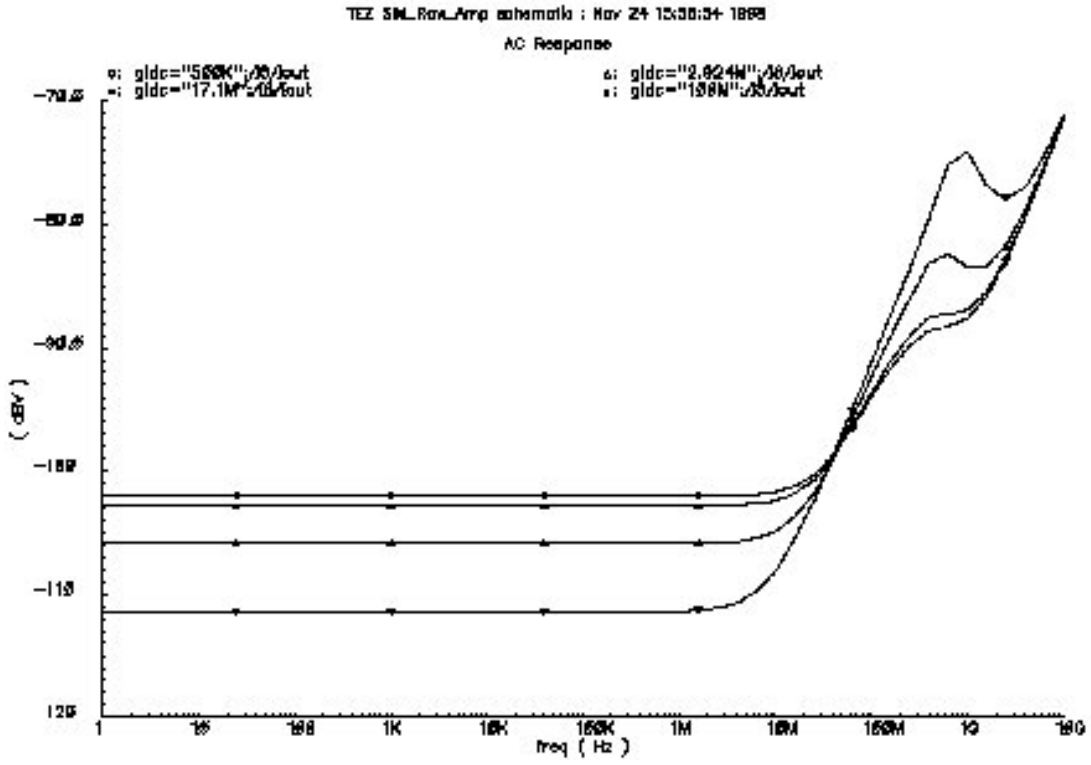

Figure 3.2-7 The variation of the output current with respect to the noise introduced through V_{DD} rail.

The variation of the output current with respect to the noise introduced through gnd rail can be seen in Figure3.2.8. The curve family is obtained the same way. The selected output resistances of the current sources are identical to the previous resistance values. Typical value of the variation is also below –105 dB.

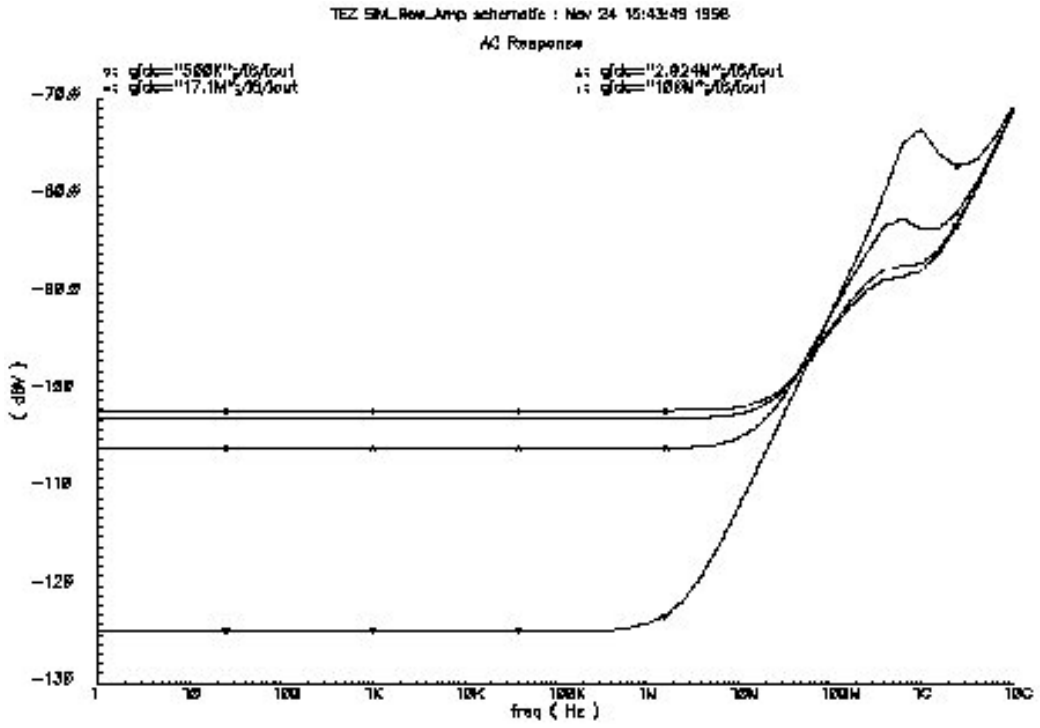

Figure 3.2-8 The variation of the output current with respect to the noise introduced through gnd rail

The stability condition of the block will be analyzed in detail in next section. We can summarize it as follows:

The block ROW_AMP has only one feedback loop formed by transistors M1 and M2, which contains two poles. The dominant pole is on node A where the drain terminals of the transistors M1 and M4 are connected. The non-dominant pole is on the input node. As there are only two poles, the block ROW_AMP is unconditionally stable. The only condition is that to avoid ringing, the non-dominant pole must be sufficiently far away from the dominant pole. The transistor sizes of the block ROW_AMP can be seen in table 3.2.1.

	W (μm)	L (μm)
M1	2	0.6
M2	10	0.6
M3	5.5	5.5
M4	2	0.6

Table 3.2-1 Transistors sizes of the block ROW_AMP

Transient simulation result of ROW_AMP can be seen in Figure3.2.9. Input source is a current pulse. In the Figure 3.2.9, the signal named /I8/Iin represents the input terminal current of the block and obviously, the signal /I8/Iout represents the output terminal current.

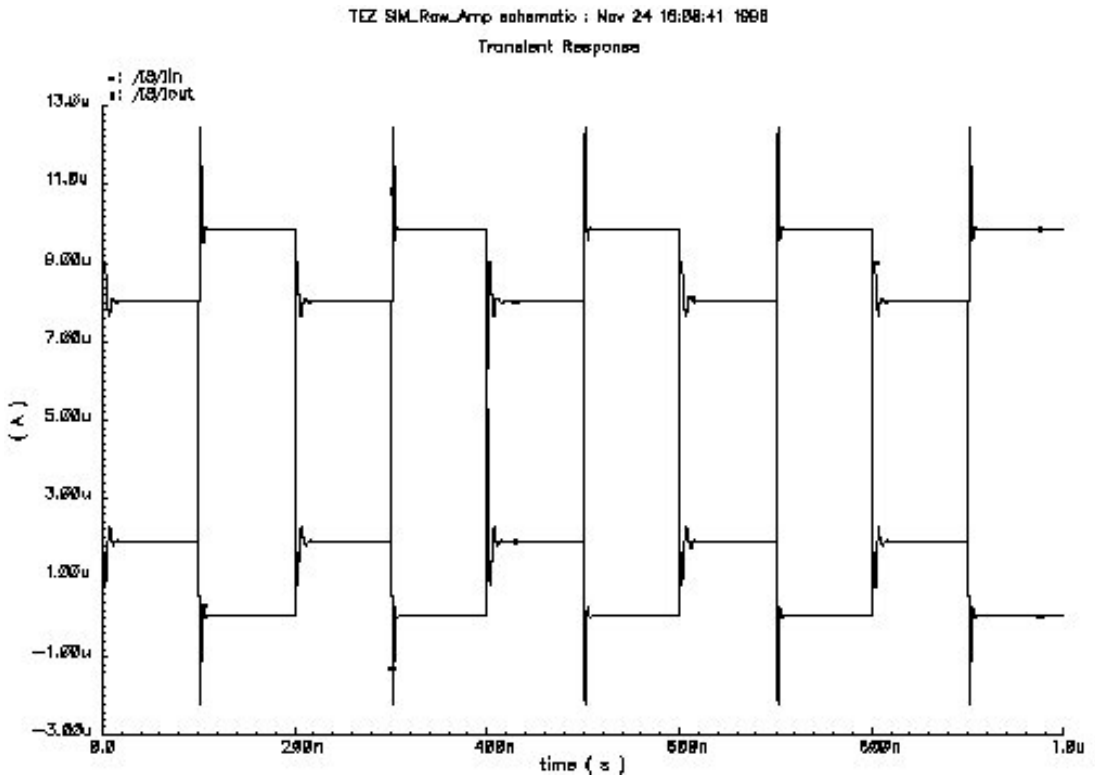

Figure 3.2-9 Transient simulation result of ROW_AMP

As we can see in Figure3.2.9. ROW_AMP output current settles very rapidly. Settling time for %1 to final output level is less than 12ns.

Layout view of the block ROW_AMP can be seen in Figure 3.2.10. In order to improve modularity, the height of the block is designed equal to the height of the block DCELL. The height of the block is 26.8μm and its width is 31.4μm. Like the DCELL block, there are 2 ROW_AMP block in the layout. Thus, ROW_AMP consumes a silicon area of 4.3332e-4mm^2.

Another design consideration that must be taken into account is the variation of the drain current of transistor M3 due to the process noise. The output currents of the blocks ROW_AMP are used into the classification process by Winner-Takes-All

networks (WTA). The variation of the bias current, I_B, reduces the precision of the WTA network, thus the precision of the Vector Quantizer system. In order to improve matching between the blocks ROW_AMP, the channel area of the transistor M3 must be as big as possible. Monte Carlo simulation result of the drain current of transistor M3 can be seen in Figure3.2.11. The mean value of the bias current is 29.71μA and the standard deviation is 163.036nA.

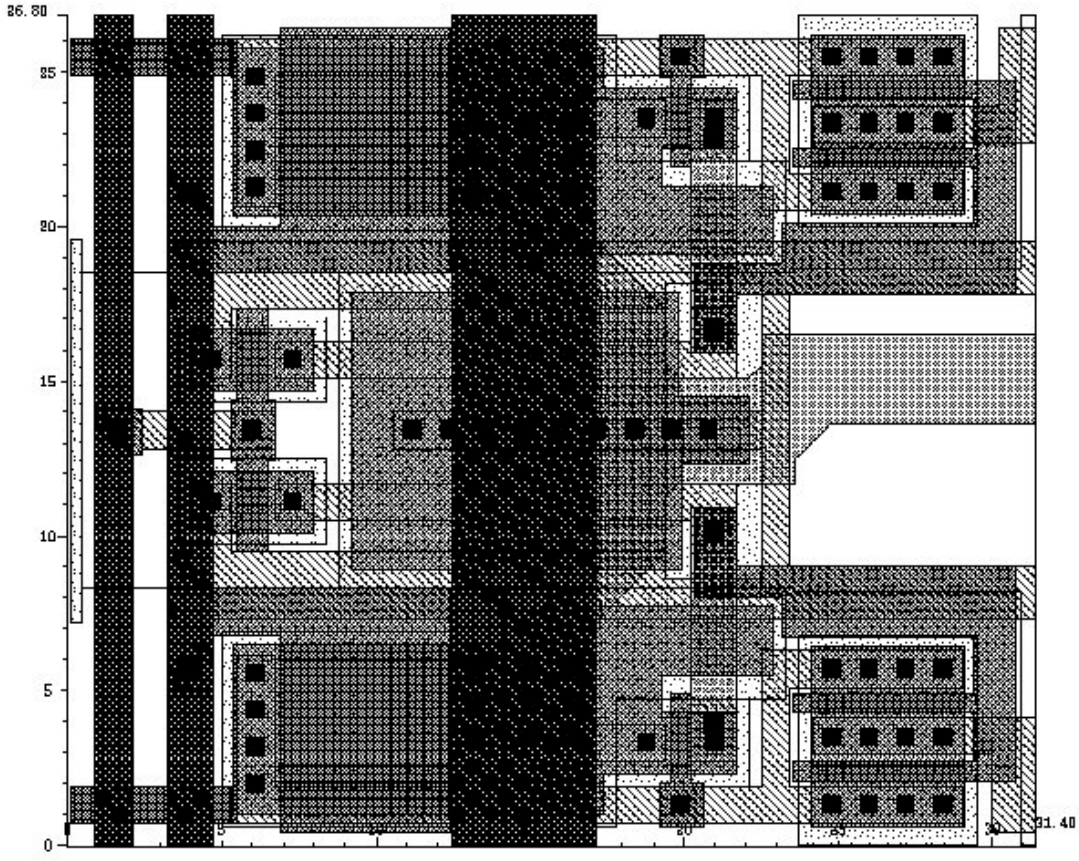

Figure 3.2-10 Layout view of ROW_AMP

Let me now calculate the power consumption of one DCELL row and all the DCELL matrix. The power consumption of one DCELL row is

$$P_{DCELL\_ROW} = (I_{BIAS} + I_K)V_{DD} \qquad 3.2.13$$

And the power consumption of the DCELL matrix containing n row is

$$P_{DCELL\_matrix} = (n+1)(I_{BIAS} + I_K)V_{DD} \qquad 3.2.14$$

For system level simulation, I developed a behavioral AHDL code. The behavioral code models only the equations of definition of the block described in (3.2.3). The behavioral AHDL code of the block ROW_AMP can be found in

Appendix G. The simulation result of the AHDL code can be seen in Figure3.2.12.

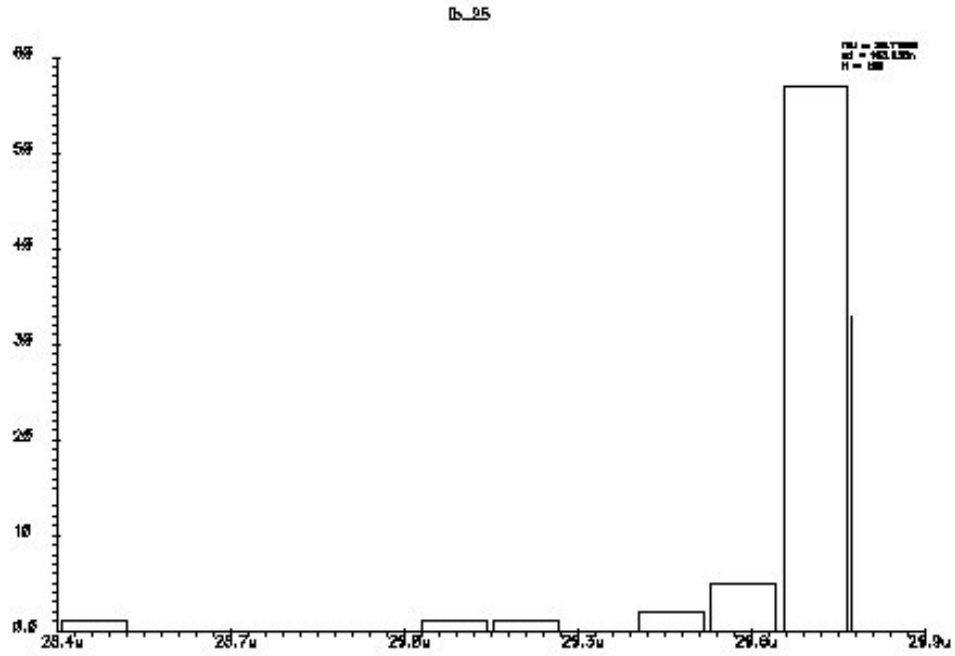

Figure 3.2-11 Monte Carlo simulation result of M3 transistor drain current.

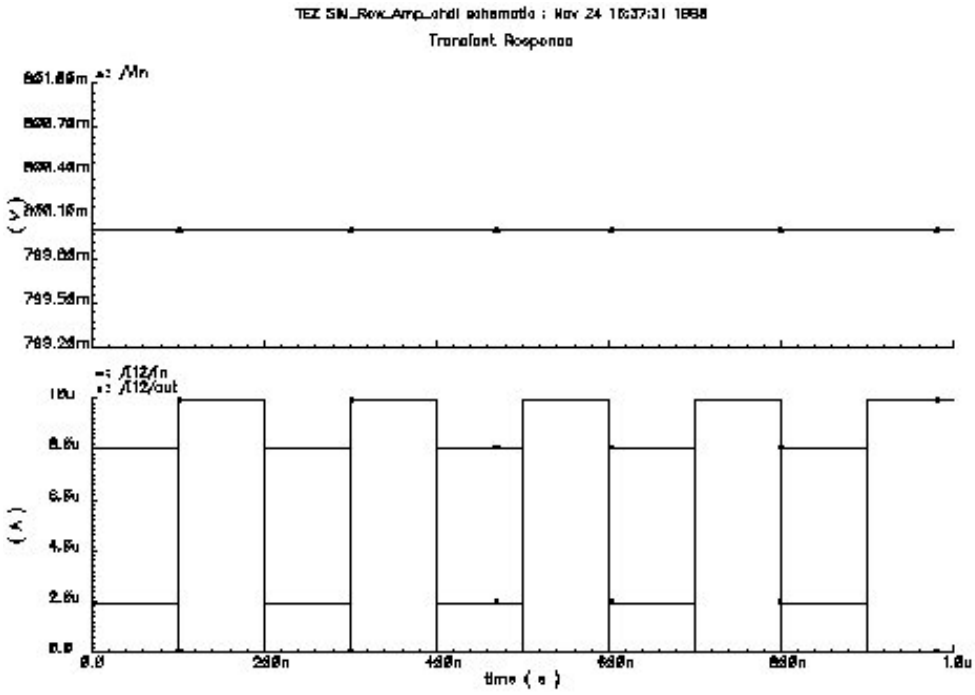

Figure 3.2-12 Simulation result of AHDL code of ROW_AMP.

Let me now summarize the design procedure of the block ROW_AMP, with respect to our previous analysis.

1. The bias current I_B is chosen with respect to the stability condition and it must be unconditionally greater than the maximum DCELL row current.

2. Aspect ratio of transistor M3 is chosen with respect to its saturation condition determined by the bias current I_B and the input terminal voltage.

3. Channel area of transistor M3 is chosen with respect to given matching properties.

4. The bias current of the transistor M1 and the aspect ratios of the transistors M1 and M2 are chosen with respect to stability conditions.

5. In order to increase modularity, layout height of the block must be equal to DCELL's layout height.