

3.4 Input Amplifier (IN_AMP)

In the previous sections, I have analyzed the building blocks that measure the distances and classify them. In this subsection I will study the analog building block that drives DCELLs' input terminals.

As shown in Figure 2.1, input signals must be applied concurrently to all DCELLs on the same matrix column for parallel computing of the distances. Thus, the terminals V_{IN+} and V_{IN-} are common terminals for each DCELL on the same matrix column. The block called 'IN_AMP' is an analog block that drives these common terminals V_{IN+} and V_{IN-} . It is obvious that we need one IN_AMP block for every column of the matrix. Schematic view of proposed IN_AMP block can be seen in Figure 3.49. Let us assume that the block drives the column i of the DCELL matrix.

The block has two input terminals. Input terminal called V_I is connected directly to the input pad where the i^{th} input vector element is applied. Input terminal called V_{DAC} is connected to the output of the digital to analog converter (DAC) that drives the i^{th} template-vector element. Thus, similarly, we need one DAC block for every column of the DCELL matrix. To separate the input terminals V_I and V_{DAC} , only one transmission gate is utilized because DACs' outputs can be brought to high impedance state internally.

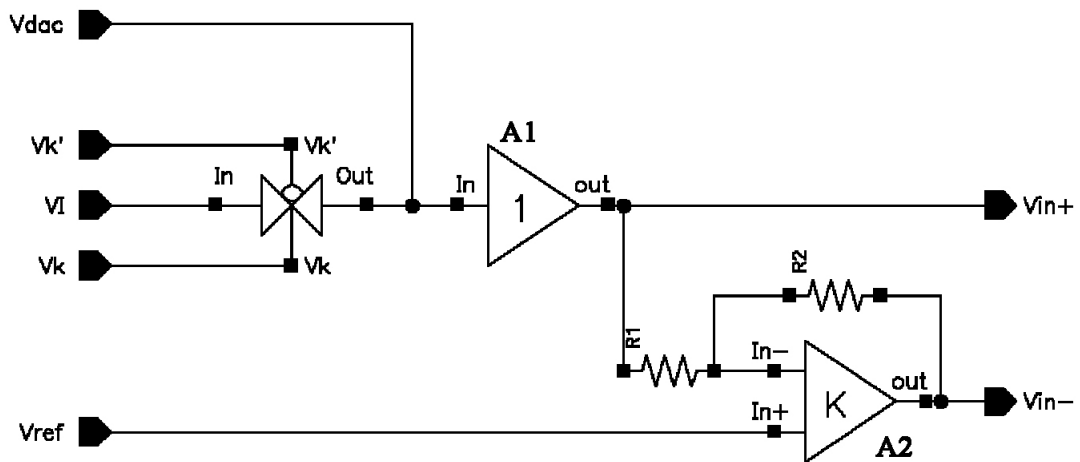


Figure 3.49 : Schematic view of IN_AMP block.

Total capacitance of node V_{IN+} (or V_{IN-}) is less than 1 pF for a matrix containing 64 rows (template-vector). We can easily remark that the amplifier A1 driving terminal V_{IN+} is loaded also resistively. Thus, Negative Amplifier (NA) formed by the amplifier A2 and two resistors, R1 and R2, sinks (or sources) current from its input terminal. Due to the large output resistance of the DAC blocks (approximately 5 k Ω), we need to utilize the amplifier A1.

The following parameters must be considered during the design of the block IN_AMP.

1. Linearity requirement of DCELL. This parameter determines the followings specifications:
 - a) Upper bound of matching property of resistors R1 and R2,
 - b) Minimum open loop voltage gain of amplifier A2 at operating frequency.
 - c) Upper bound of variation of amplifiers' voltage gains within the input signal range.

2. Settling time of the amplifier A2. This parameter determines the followings
 - a) Upper bound of input signal frequency
 - b) Clock frequency of system's digital blocks.

We have chosen that the input signal range of the block is 0-3V and the linearity requirement is less than %1, as calculated in section 3.1. We start our analysis with the amplifier A1.

In section 3.1, we have showed that the offset voltages of the Amplifiers A1 and NA have no impact on the operation of the block DCELL. Thus, we can utilize a simple source-follower (SF) circuit in place of the amplifier A1. Schematic view of the source-follower can be seen in Figure 3.50.

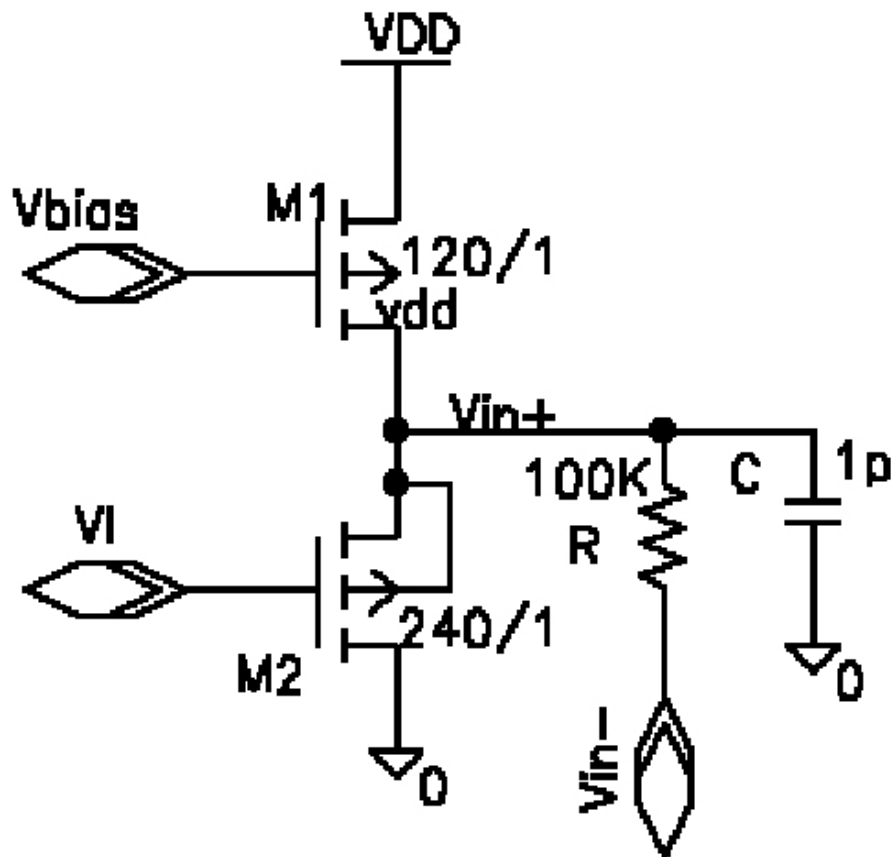


Figure 3.50 : Schematic view of source-follower

In Figure 3.50, the amplifier A2 is modeled by the resistor R and the terminal V_{IN-} , being equal to $V_{DD}-V_{IN+}$. This circuit topology is chosen because of its simplicity, speed, small area consumption. The main disadvantage of the source-follower structure is low power supply rejection ratio. The PSRR performance of the overall block IN_AMP is determined by the source-follower part of the block.

Bias current ($I_{D(M1)}$) of SF is determined with respect to resistive load's current (I_R). It is chosen $200\mu A$. Aspect ratios of the transistors M1 and M2 can be seen in table 3.4.

Table 3.4 : Aspect ratios of the Source follower's transistors.

	W (μm)	L (μm)
M1	120	1
M2	240	1

Let us now calculate the input and output voltage ranges of the block. Maximum output voltage level of the source follower is

$$V_{O \max} = V_{DD} - V_{DSsat(M1)} \quad 3.97$$

Minimum output voltage of the source follower can be expressed as follows:

$$V_{O \min} = -V_{TP(M2)} + \sqrt{\frac{I_{D2}}{\beta_2}} \quad 3.98$$

Yet, in (3.98), the current I_{D2} is a function of the output voltage. When output voltage is equal to its minimum value, voltage V_{IN} is equal to $V_{DD} - V_{O \min}$. Thus I_{D2} may be denoted as

$$I_{D2} = I_{D1} + \frac{(V_{DD} - V_{O \min}) - V_{O \min}}{R} \quad 3.99$$

Thus minimum output voltage is

$$V_{O \min} = -V_{TP(M2)} + \sqrt{\frac{1}{\beta_2} \left(I_{D1} + \frac{V_{DD} - 2V_{O \min}}{R} \right)} \quad 3.100$$

Maximum input voltage level of the source follower can be expressed as follows:

$$V_{IN \max} = V_{DD} - V_{DSsat(M1)} + V_{TP(M2)} - \sqrt{\frac{I_{D2}}{\beta_2}} \quad 3.101$$

The drain current of transistor M2 can be denoted as

$$I_{D2} = I_{D1} - \left(\frac{V_{DD} - 2V_{DSsat(M1)}}{R} \right) \quad 3.102$$

Thus maximum input voltage level is

$$V_{IN \max} = V_{DD} - V_{DSsat(M1)} + V_{TP(M2)} - \sqrt{\frac{1}{\beta_2} \left(I_{D1} - \frac{V_{DD} - 2V_{DSsat(M1)}}{R} \right)} \quad 3.103$$

And finally, the minimum input voltage level is

$$V_{IN\min} = g_{nd} = 0V \quad 3.104$$

Let us now calculate the small signal voltage gain of SF. Small signal equivalent circuit of source-follower can be seen in Figure 3.51.

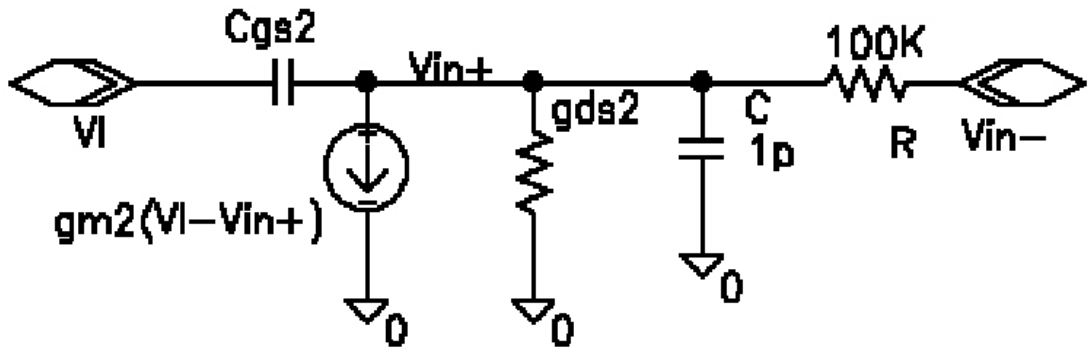


Figure 3.51 : Small signal equivalent circuit of source-follower.

Node equation of the circuit is

$$sC_{GS2}(V_I - V_{in+}) + gm_2(V_I - V_{in+}) = \left(g_{ds2} + sC + \frac{2}{R} \right) V_{in+} \quad 3.105$$

Thus, with respect to (3.105), the small signal voltage gain of the source-follower can be expressed as follows

$$\frac{V_{in+}}{V_I} = \frac{sC_{GS2} + gm_2}{s(C + sC_{GS2}) + \frac{2}{R} + gm_2 + g_{ds2}} \quad 3.106$$

The current sink from the output of the source-follower varies with voltage level of the output node. That is why the parameter gm_2 is a function of output node voltage V_{OUT} . In order to minimize the effect of the output node voltage on the parameter gm_2 , we have to increase the aspect ratio of the transistor M2 and the drain current of the transistor M1. The variation of parameter gm_2 with respect to voltage V_{IN+} must satisfy given linearity conditions. Small signal voltage gain of the source-follower can be seen in Figure 3.52. The linearity condition is satisfied up to 25MHz. However, I will show later that the system speed is determined by the settling time of the part NA.

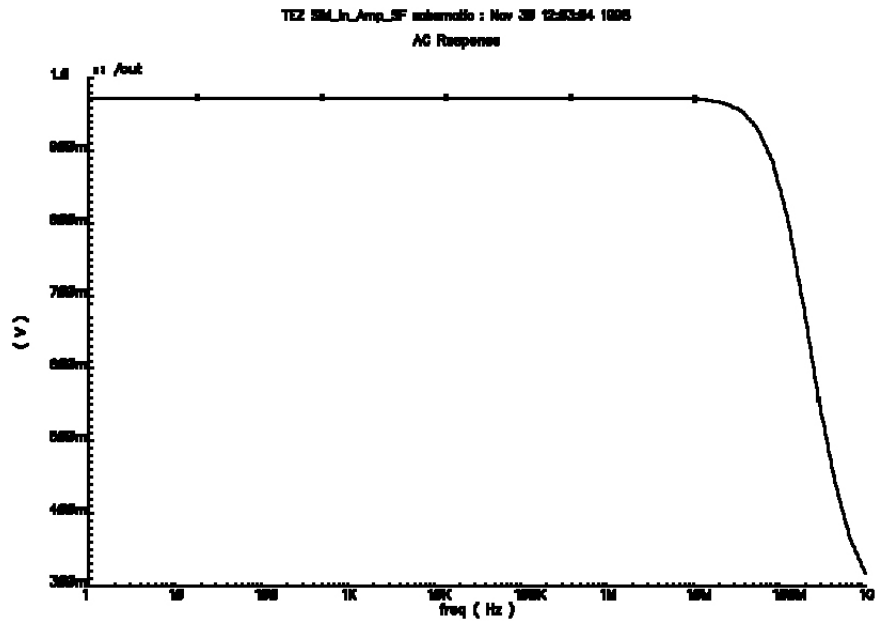


Figure 3.52 : Small signal simulation result of source-follower.

The variation of small signal voltage gain with respect to the input signal voltage level can be seen in Figure 3.53. Variation of the voltage gain is less than 0.3%. As mentioned previously, the main disadvantages of the SF is its low PSRR. To increase PSRR more complicated structures must be used [37]. -PSRR (V_{DD}) of SF, which is less than -40 dB, can be seen in Figure 3.54. And -PSRR (gnd) of SF, which is less than -35 dB, can be seen in Figure 3.55

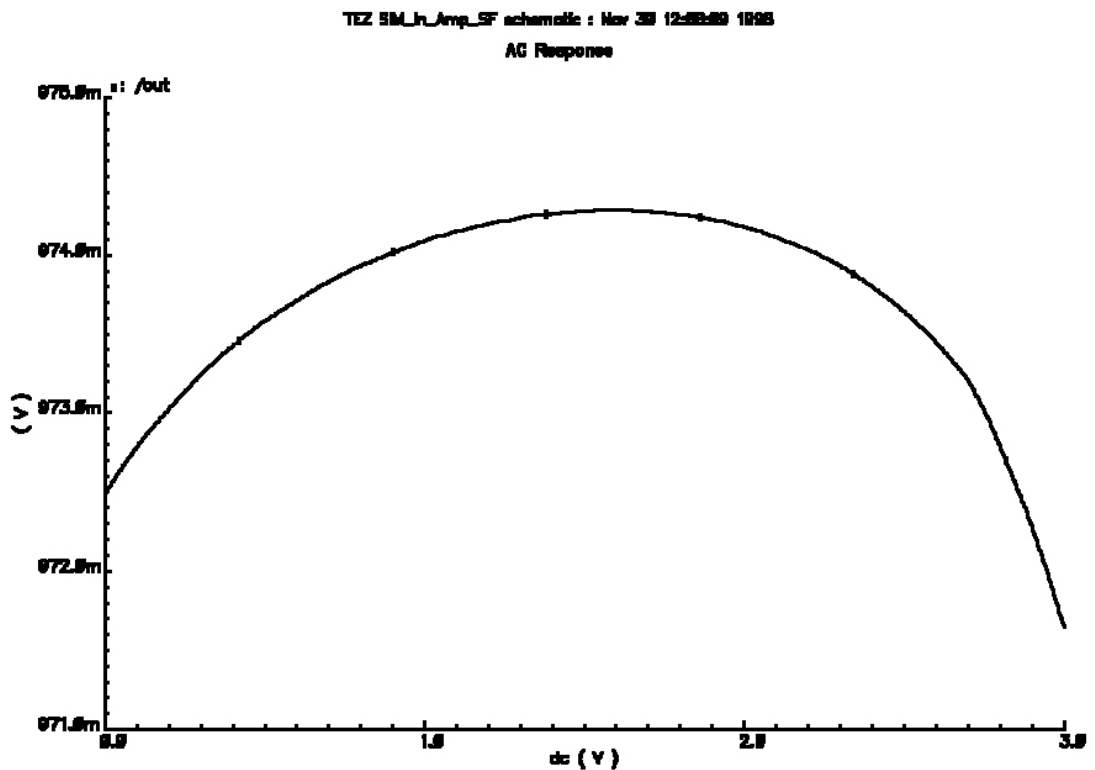


Figure 3.53: Variation of small signal voltage gain with input dc voltage level at 1

Hz.

TEZ 5M_In_Amp_SF schematic : Nov 30 12:18:20 1998
AC Response

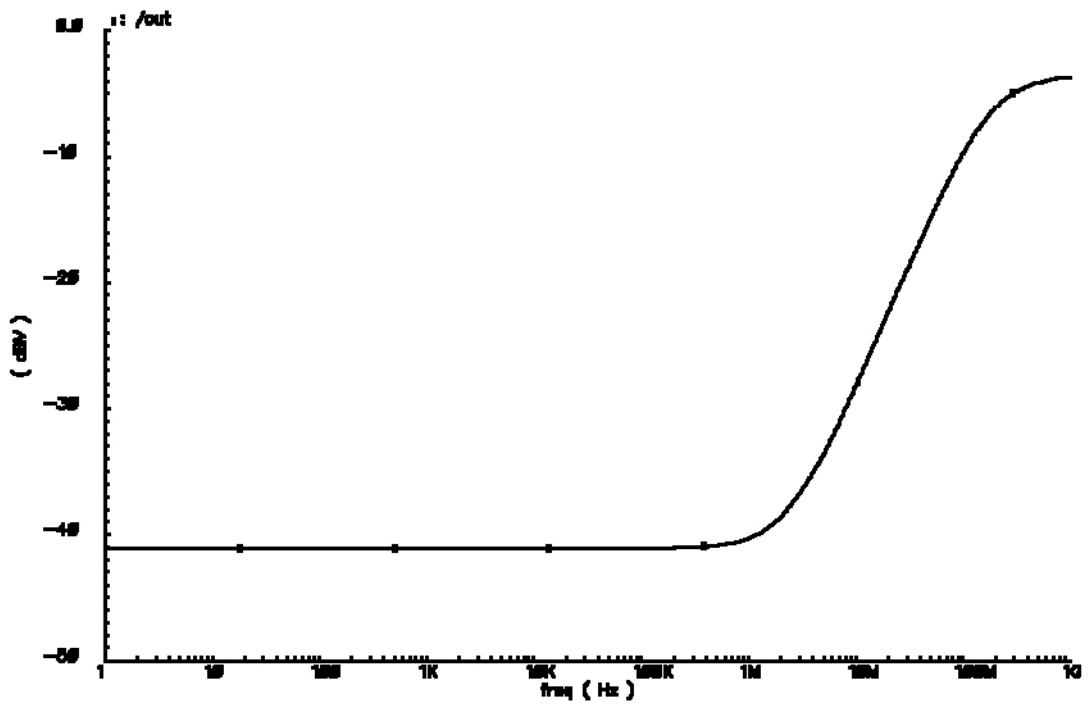


Figure 3.54 : PSRR (V_{DD}) of source follower

TEZ 5M_In_Amp_SF schematic : Nov 30 12:28:43 1998
AC Response

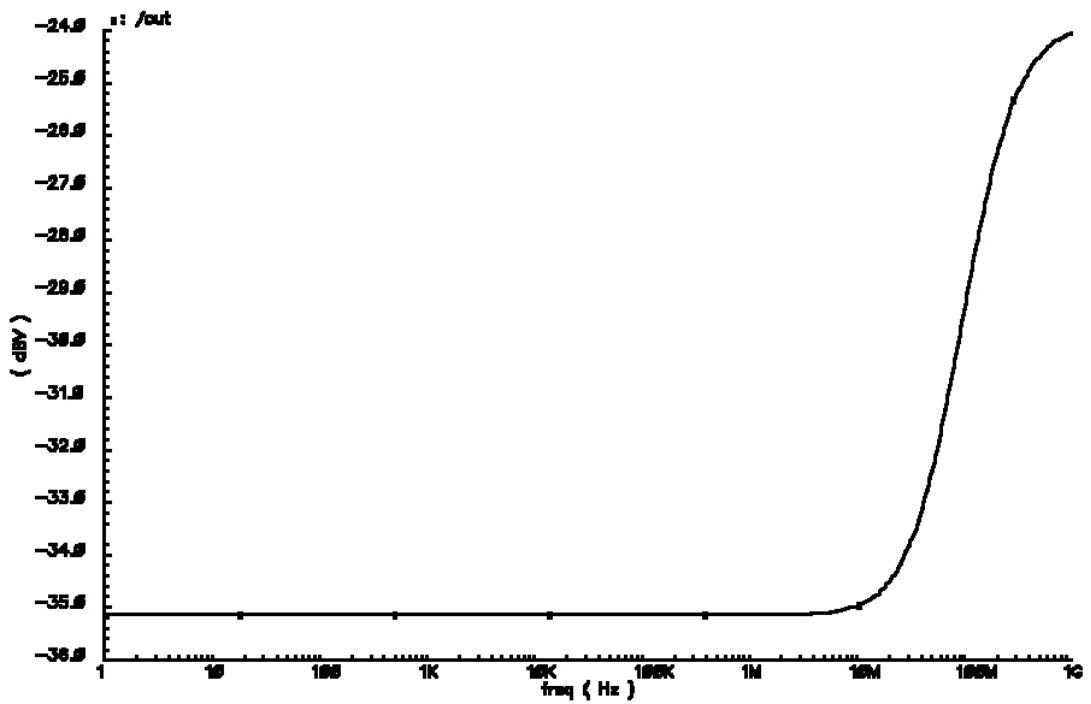


Figure 3.55 : PSRR (gnd) of source follower

Transient simulation result of source-follower can be seen in Figure 3.56. Input is a sinusoidal signal and its frequency is 1MHz. In Figure 3.56, /vin represents input signal and /out represents output signal.

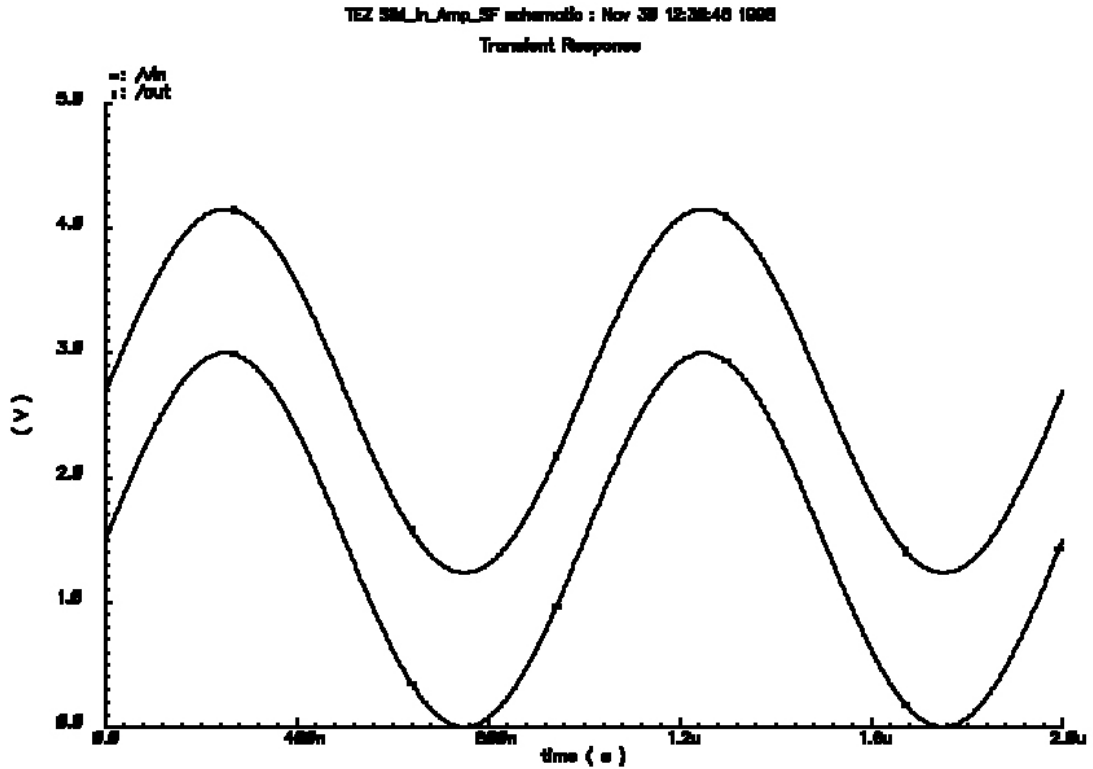


Figure 3.56 : Transient simulation result of source-follower

Let us now begin our analysis on the part NA of the block IN_AMP. The schematic view of the part NA that drives output terminal V_{IN-} can be seen in Figure 3.57.

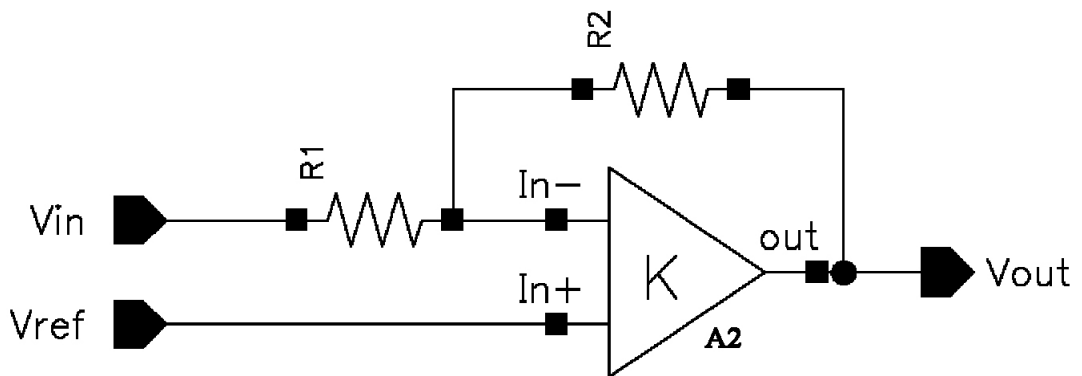


Figure 3.57 : Schematic view of the NA.

Disadvantages of this structure are

1. It sinks (or sources) current from its input terminal.

2. Due to the process noise, mismatch occurs between resistors R1 and R2. Thus voltage gain may vary.
3. Feedback resistor shifts the pole on the output node to higher frequency. Yet, because of the input capacitance of the amplifier A2, we introduce an extra pole in the feedback loop, which worsens phase margin of the amplifier A2.
4. Large silicon area consumption. In order to minimize mismatch effect we have to increase the silicon area occupied by the resistors. And to achieve required voltage gain, we have to utilize an amplifier containing 2 stages. Thus, we need a compensation capacitance...

With a straightforward calculation, the transfer function of NA can be expressed as follows

$$V_O = \left[\frac{KR_1}{(K+1)R_1 + R_2} \right] \left[\frac{R_2}{R_1} (V_{REF} - V_{IN}) + V_{REF} \right] \quad 3.107$$

where K is the open loop gain of the amplifier A2. Assuming that

$$K \rightarrow \infty, \quad R_1 = R_2 \quad \text{and} \quad V_{REF} = \frac{V_{DD}}{2}$$

(3.107) is simplified as follows:

$$V_O = V_{DD} - V_{IN} \quad 3.108$$

In Section 3.1, I calculated the linearity requirement of DCELL as 1%. In order to satisfy this condition, we have to reanalyze (3.107) and calculate the upper bound of matching properties of resistors R1 and R2 and minimum value of amplifier's gain K at operating frequency. We start our analysis by replacing $\frac{R_2}{R_1}$ by R in (3.107), which is ideally equal to 1. Thus (3.107) becomes

$$V_O = \frac{K}{(K+1)+R} [R(V_{REF} - V_{IN}) + V_{REF}] \quad 3.109$$

Under the ideal conditions denoted previously, the ideal value of V_O denoted as \bar{V}_O can be expressed as follows:

$$\bar{V}_O = 2V_{REF} - V_{IN} \quad 3.110$$

Thus the error (Δ) can be expressed as follows:

$$\Delta = \frac{V_O - \bar{V}_O}{\bar{V}_O} = \frac{K}{(K+1)+R} \frac{[R(V_{REF} - V_{IN}) + V_{REF}]}{2V_{REF} - V_{IN}} - 1 \quad 3.111$$

In (3.111), we replace R by

$$R = 1 + \Delta R \quad 3.112$$

where ΔR represents the mismatch effect. Thus (3.111) becomes

$$\Delta = \frac{K}{(K+2)+\Delta R} \left[1 + \frac{\Delta R(V_{REF} - V_{IN})}{2V_{REF} - V_{IN}} \right] - 1 \quad 3.113$$

The voltage V_{REF} is equal to $\frac{V_{DD}}{2}$. We select input voltage level in order to find maximum error within the input signal range. Thus output error can be expressed as follows:

$$\Delta = \frac{K}{(K+2)+\Delta R} \left[1 + \frac{1,7\Delta R}{0,8} \right] - 1 \quad 3.114$$

Output error plot of NA with respect to voltage gain K of the amplifier A2 can be seen in Figure 3.58.

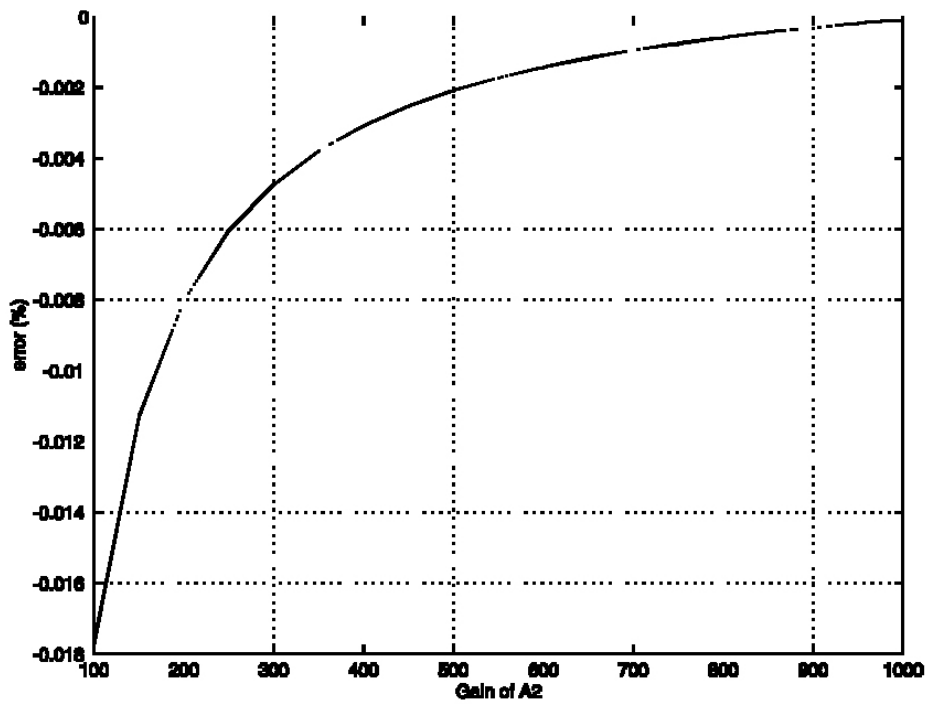


Figure 3.58 : Output error plot with respect to voltage gain K of amplifier A_2

Output error plot of N_A with respect to resistor mismatch ΔR can be seen in Figure 3.59.

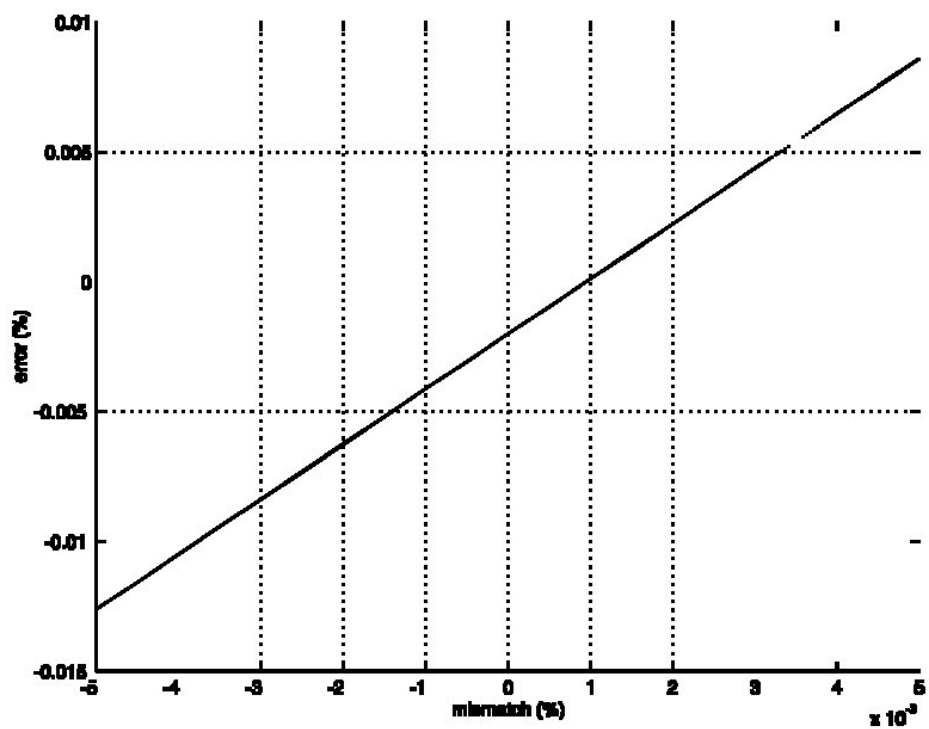


Figure 3.59 : Output error plot with respect to resistor mismatch ΔR

In order to satisfy the given 1% linearity condition, the open loop voltage gain K of the amplifier A2 at the operating frequency, must be greater than 200 and the mismatch ΔR must be smaller than 0.5%.

We have utilized cell OP01B of AMS 0.6 μ m CUQ process's analog standard cell library A_CELLS in place of the amplifier A2. Technical specifications of the operational amplifier OP01B can be found in Appendix F. Schematic view of the block OP01B can be seen in Figure 3.60.

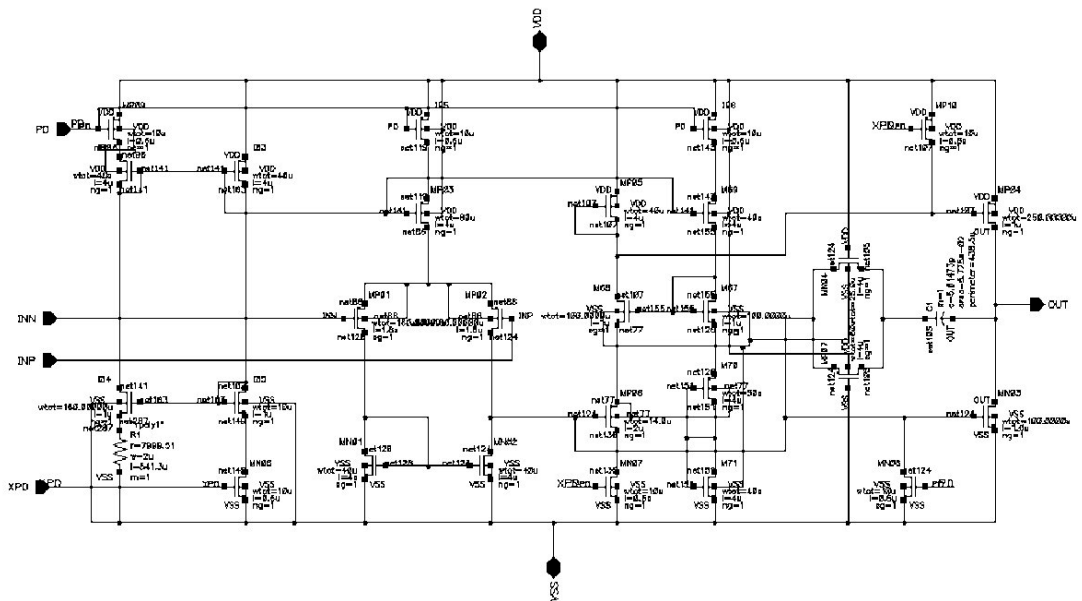


Figure 3.60 : Schematic view of OPAMP OP01B

Small signal simulation results (open loop gain and phase) of OPAMP OP01B without feedback load can be seen in Figure 3.61. Phase margin of the block is 78°.

Small signal voltage gain and phase margin have to be reexamined also with the feedback loop load due to the extra pole added into the feedback loop. This extra pole decreases the phase margin of the block.

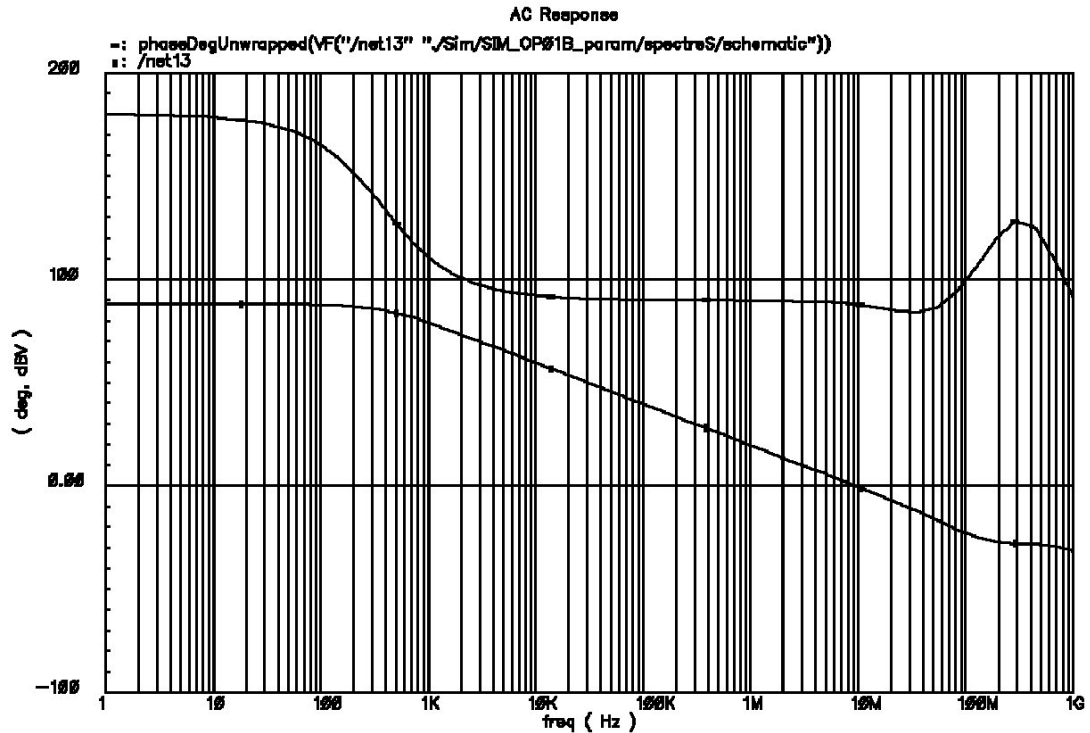


Figure 3.61 : Small signal simulation result of OP01B without feedback load

To increase phase margin that means shifting the pole to the higher frequencies, we have to use smaller feedback resistor that causes to consume more power. Thus, there is a trade-off between power consumption and phase margin. We have chosen $R1 = R2 = 50 \text{ k}\Omega$. Small signal simulation results (open loop gain and phase) of OPAMP OP01B with feedback load can be seen in Figure 3.62. In this case, Phase margin is 57° .

Variation of small signal voltage gain of the part NA with respect to input voltage level at 1 Hz can be seen in Figure 3.63. Obviously, acceptable input signal range is equal to the minimum of the common mode input ranges of the operational amplifier OP01B or SF.

TEZ SIM_OP01B_param schematic : Nov 30 14:14:41 1998

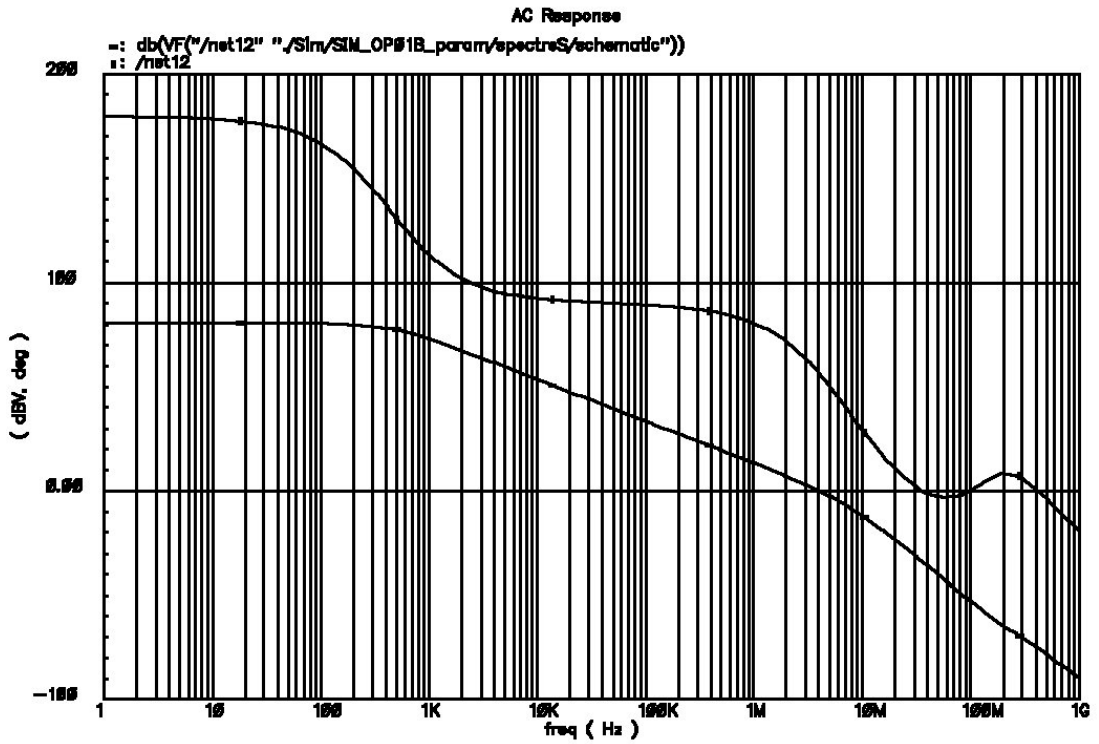


Figure 3.62 : Small signal simulation result of OP01B with feedback load

TEZ SIM_OP01B schematic : Nov 30 15:11:33 1998

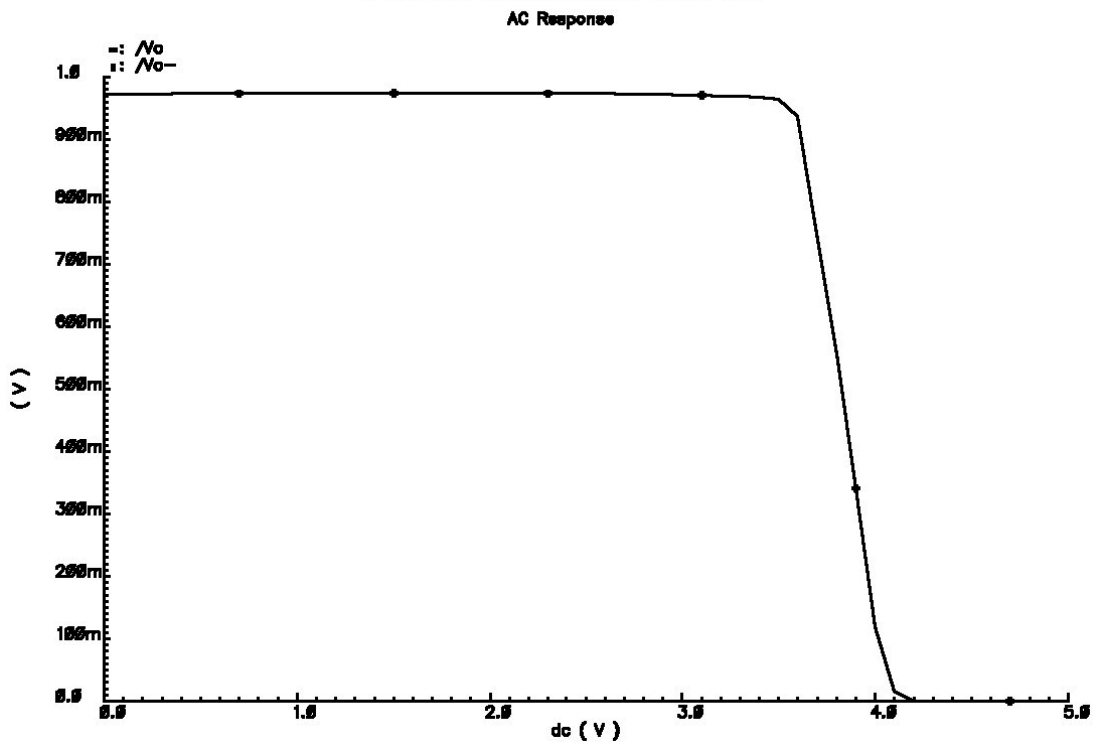


Figure 3.63 Small signal gain variation with respect to input dc voltage level.

DC simulation result of the block IN_AMP can be seen in Figures 3.64. Horizontal axis is the input signal. Signal /Vo represents the output V_{IN+} and obviously Signal /Vo- represents the output V_{IN-} .

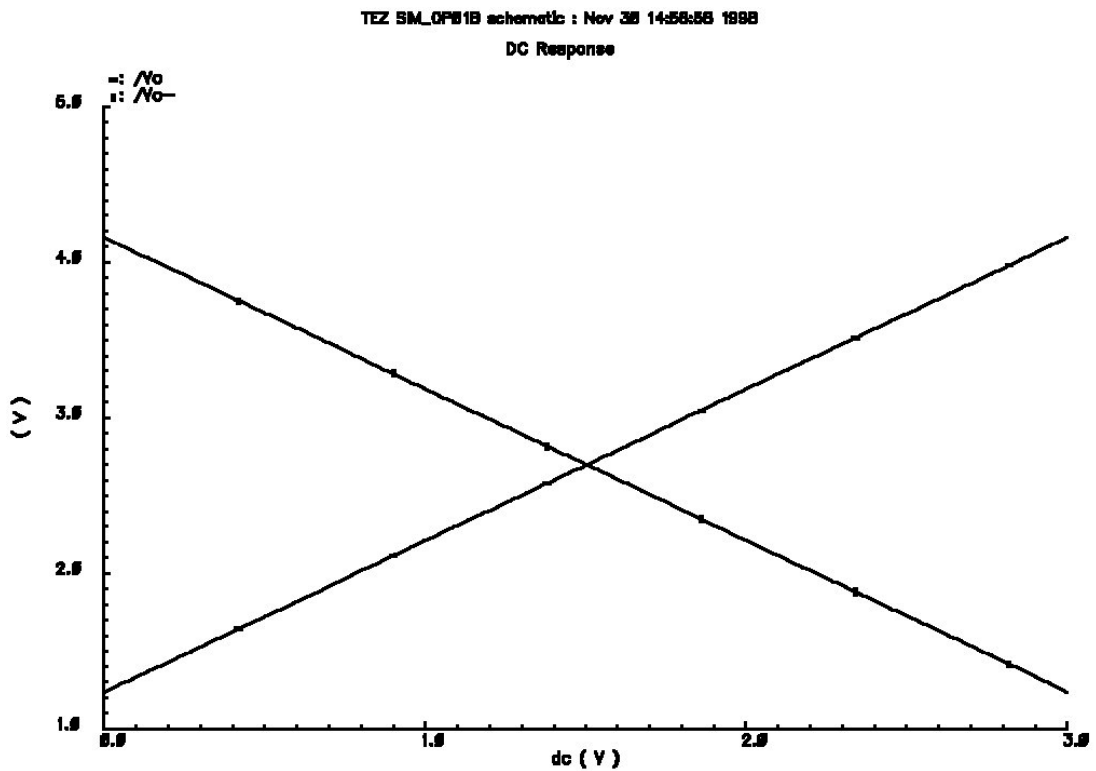


Figure 3.64 : DC Simulation result of the block IN_AMP

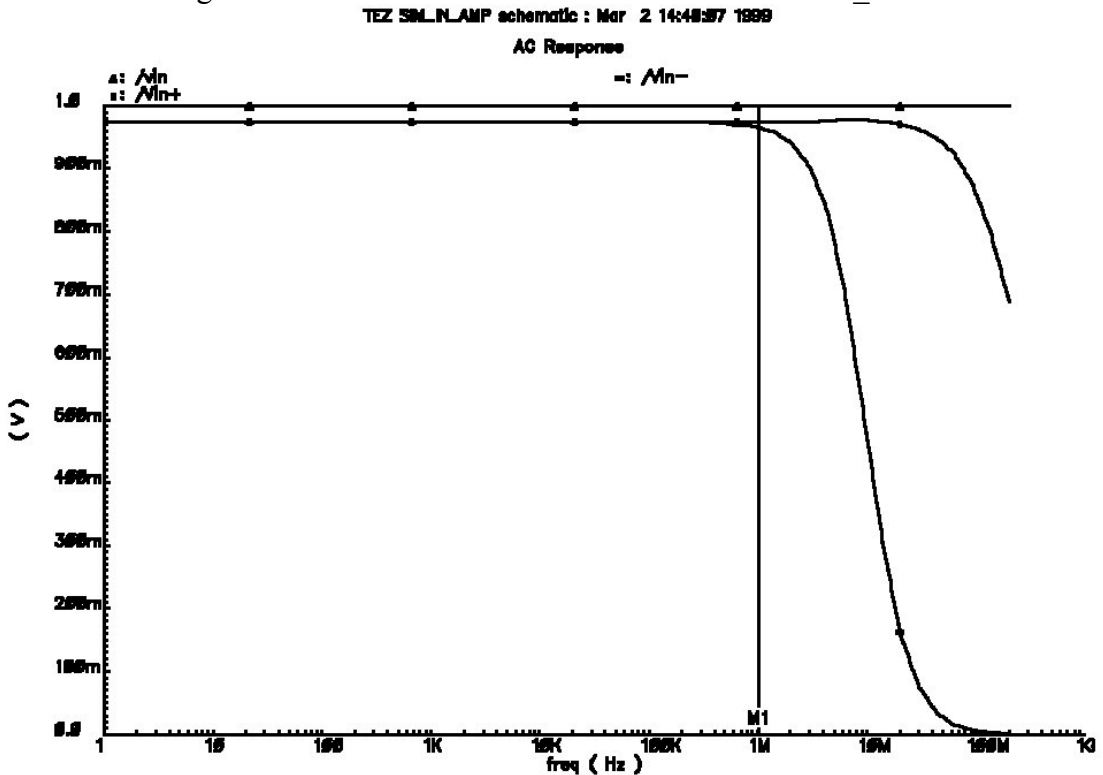


Figure 3.65 : AC Simulation result of IN_AMP

AC simulation result of the block IN_AMP can be seen in Figure 3.65. In the Figure 3.65, the signal /vin represents the input signal; the signal /vin+ represents the output vin+ and the signal /vin- represents the output vin-. The linearity condition can be satisfied with this structure up to 1MHz.

-PSRR(V_{DD}) of IN_AMP block can be seen in Figure 3.66. As before, the signal /Vo represents the signal on terminal V_{IN+} and /Vo- represents the signal on terminal V_{IN-} . We can easily remark that the PSRR performance is determined by the source-follower part of the block. We have not showed the PSRR(gnd) of the block because it has the same characteristic. PSRR(V_{DD}) is more than 40 dB and PSRR(gnd) is more than 35 dB.

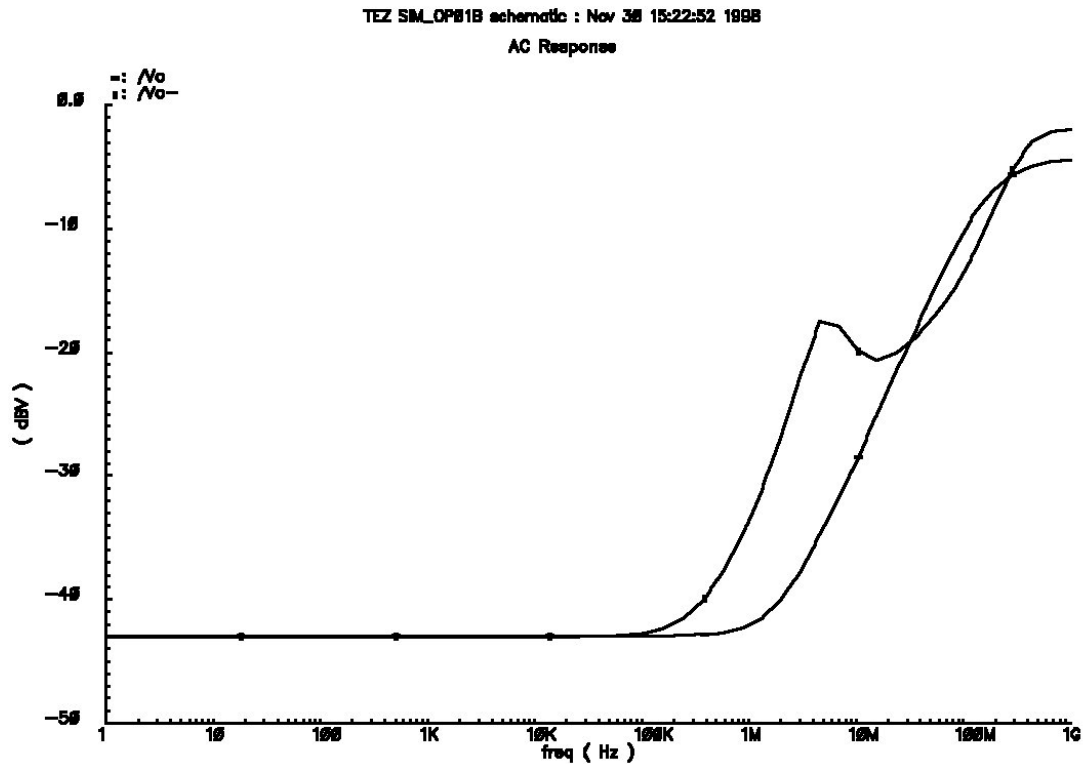


Figure 3.66 : PSRR (V_{DD}) Simulation result of IN_AMP

Transient simulation result can be seen in Figure 3.67. The input signal is a sinusoidal signal. Its amplitude is 3 V peak to peak and the frequency is 100 kHz. The signal /Vo represents the signal on terminal V_{IN+} and /Vo- represents the signal on terminal V_{IN-} . To compute settling time of the block IN_AMP, we have applied a pulse signal to the input. In the worst case the output signals of the block settle to 1% of their final value within 360ns. It can be slightly decreased by increasing phase margin (by increasing the power consumption).

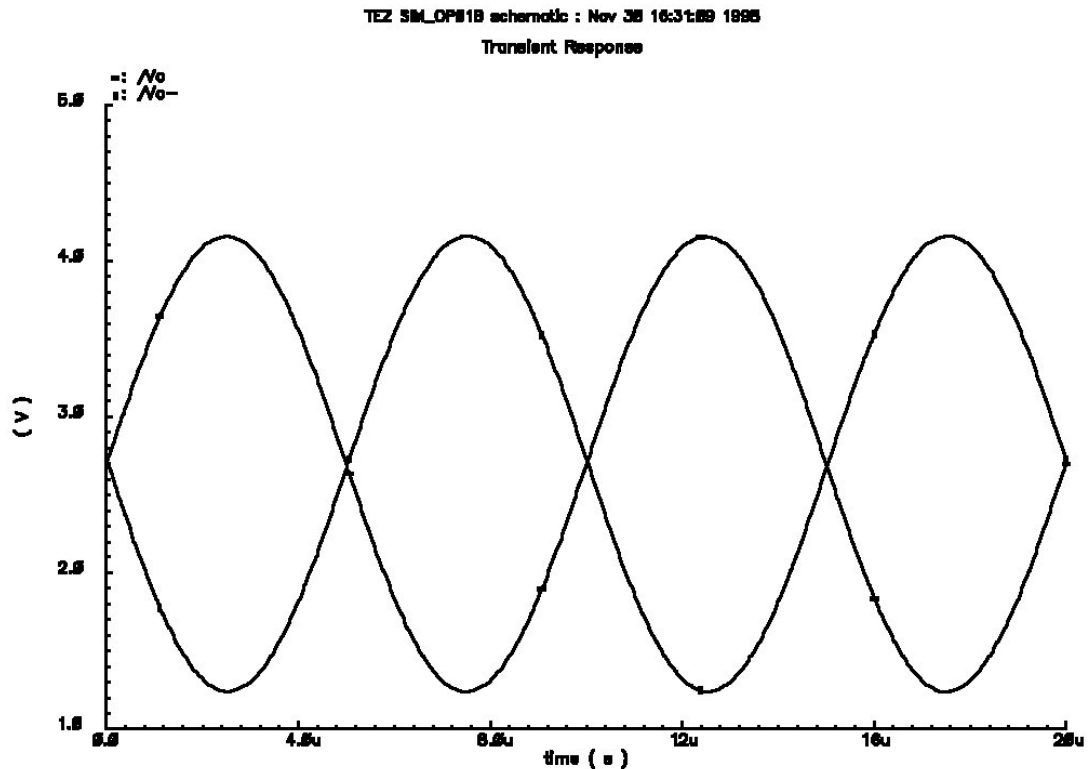


Figure 3.67 : Transient Simulation result of the block IN_AMP

Layout view of IN_AMP block can be seen in Figure 3.68. Compared to DCELL, the block IN_AMP consumes an immense silicon area. More compact and innovative solutions are needed for reducing silicon cost of overall Vector Quantizer system. To improve matching between resistors R1 and R2 dummy poly structures and inter-digitize layout techniques are used. Resistors are realized with poly layer because it is less sensitive to the temperature or the voltage level across its terminal than the other possible layers. As mentioned previously, we have to utilize one IN_AMP block for each column of the DCELL matrix. Thus, modular block layout is preferable in order to form an IN_AMP row. The height of the block is $397.6\mu\text{m}$ and its width is $139.6\mu\text{m}$. Thus, it consumes a silicon area of $55.491\text{e-}3\text{ mm}^2$.

For system level simulation, we have modeled the block IN_AMP by the simple schematic in Figure 3.69.

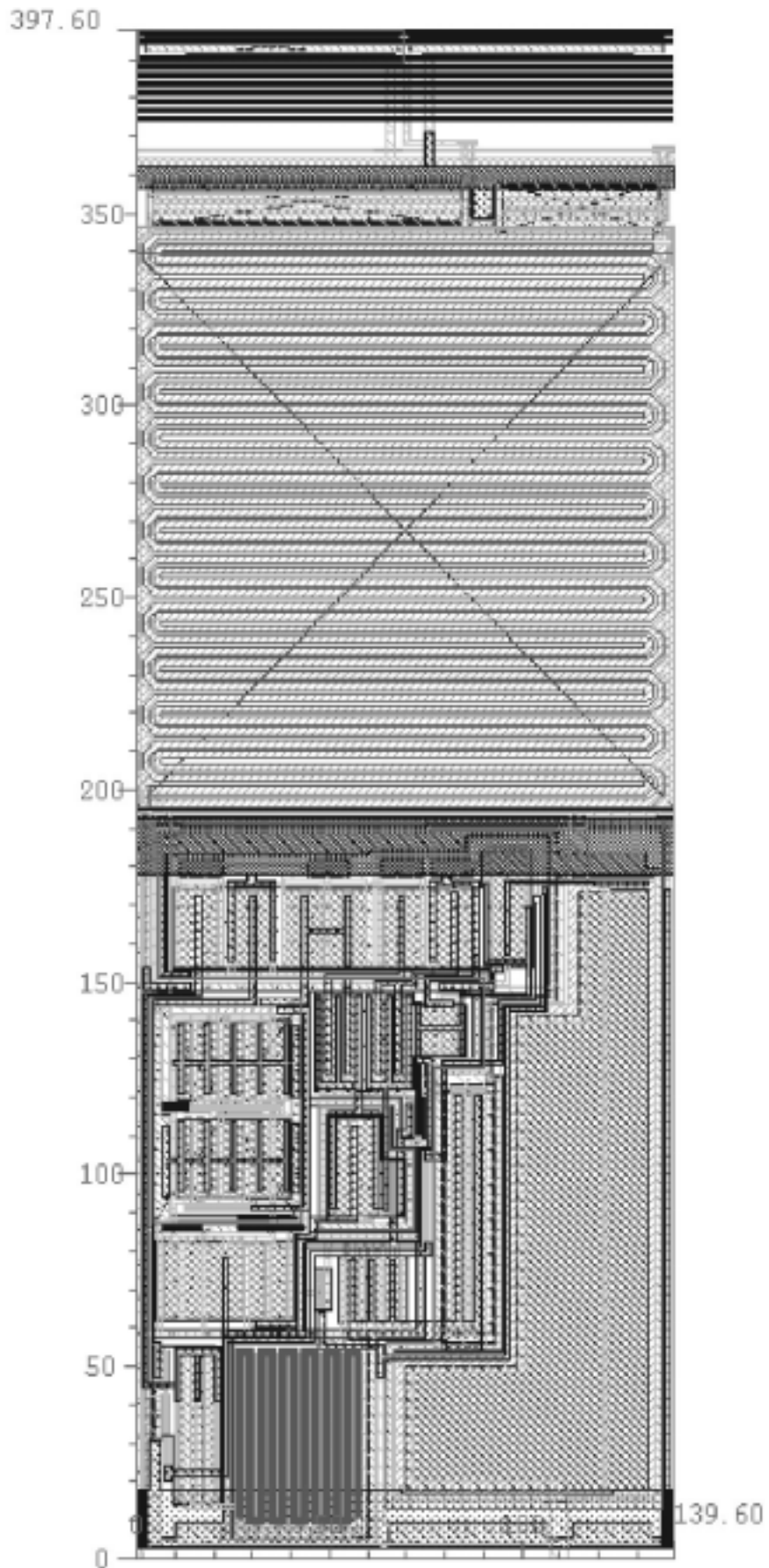


Figure 3.68 : Layout view of IN_AMP

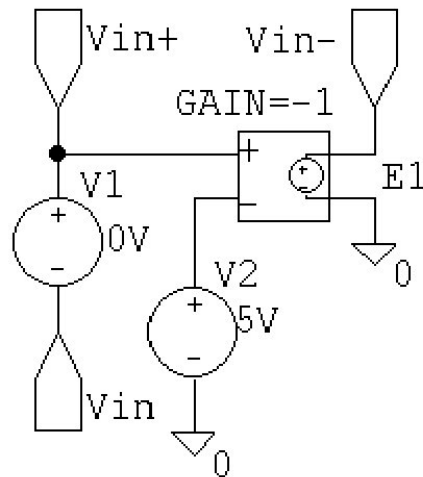


Figure 3.69 :The Ideal model of the block IN_AMP

For a final word, let us summarize the design procedure of the block IN_AMP:

Before all, to design an IN_AMP block, we must first determine the following system parameters:

1. The linearity requirement of the block DCELL
2. System's input signal range
3. Maximum input signal frequency
4. Digital block's clock frequency

After the above mentioned parameters are determined, if we decide to utilize the proposed block topology, we have to find out the following

1. Upper bound of resistor mismatch with respect to the linearity condition.
2. Resistor layer type and layout technique in order to satisfy given mismatch condition.
3. Lower bound of voltage gain of amplifier A2 with respect to the linearity condition.
4. The amplifier circuit topology in order to satisfy given gain condition and input signal range. The maximum input signal and digital block's clock frequencies are determined by the settling time of the selected amplifier topology. Thus it must satisfy these conditions too.