3.5 Digital to Analog Converter (DAC6)

Digital to Analog converters are used in VQ system to convert digitally stored template vector elements to analog template voltages. The input word length (resolution) of the DAC must be equal to (or greater than) the resolution of the block DCELL. As mentioned in Section 3.1, the resolution of the block DCELL is predicted 6 bits. Thus, voltage divider based 6 bits digital to analog converter (DAC6) is designed. The schematic view of the proposed DAC structure can be seen in Figure 3.70.

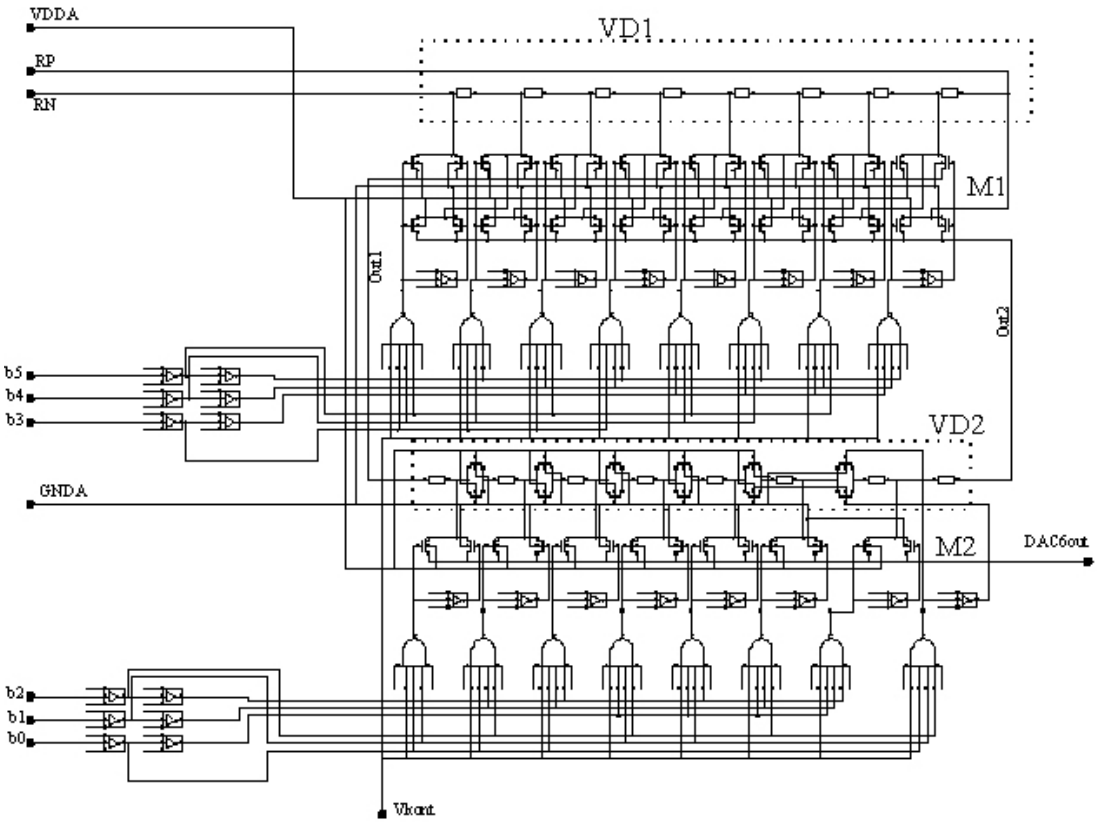

Figure 3.70 : Schematic view of DAC6

We can separate the block DAC6 into two stages. First stage consists of voltage divider VD1 containing 8 resistors of 500 Ω and multiplexer block M1. Positive reference voltage of the voltage divider VD1 is connected to the terminal V_P and negative reference voltage of VD1 is connected to the terminal V_N. Multiplexer M1 is controlled by the most significant 3 bits ($b_5b_4b_3$) of the block input. Output voltage levels of M1 can be expressed as follows:

$$\begin{aligned} Out_1 &= \frac{(V_P + V_N)}{2^3}\left(2^2 b_5 + 2^1 b_4 + 2^0 b_3\right) \\ b_5^{'} b_4^{'} b_3^{'} &= b_5 b_4 b_3 + 001 \\ Out_2 &= \frac{(V_P + V_N)}{2^3}\left(2^2 b_5^{'} + 2^1 b_4^{'} + 2^0 b_3^{'}\right) \end{aligned} \qquad 3.115$$

In (3.115) b_i represents i^{th}-input bit of DAC6. Alike first stage, the second stage also consists of a voltage divider (VD2) containing 8 resistors of 3115 Ω and a multiplexer block (M2). Positive and negative reference voltages of VD2 are connected to the first stage's outputs. M2 is controlled by the least significant 3 bits of the DAC6 input. With respect to the least significant 3 bits, M2 selects the desired analog output voltage. The analog output voltage of DAC6 can be expressed as follows

$$DAC6_{OUT} = \frac{(Out_2 + Out_1)}{2^3}\left(2^2 b_2 + 2^1 b_1 + 2^0 b_0\right) \qquad 3.116$$

The main disadvantage of this digital to analog converter structure is its high output resistance, approximately equal to 5 kΩ. This is the reason that we need an input buffer in the block IN_AMP. In order to connect the output of the DAC6 directly to the input buffer of the block IN_AMP, a control signal is added to set the block's output in high impedance state.

Voltage dividers' resistors are realized with poly layer resistance. To prevent the voltage changes at output of M1 due to the current stolen by the second stage, VD1's resistors must be smaller than VD2's resistors which implies more power consumption. To improve linearity of DAC6, we must improve matching property of voltage dividers' resistors which leads to more silicon area consumption.

We have to use one digital to analog converter for each column of DCELL matrix. Thus, the modularity must be taken into account for the design of DAC6's layout. Alike the block IN_AMP, the block DAC6 consumes much more silicon area compared to the block DCELL. Thus, in order to decrease overall system silicon area, we have to decrease silicon area consumption of the block DAC6 too. Layout

view of DAC6 can be seen in Figure 3.71. The width of the block is 133.5µm and its height is 205.7µm. The total silicon area is 27.46e-3mm^2.

The transient simulation result of DAC6 can be seen in Figure 3.72. The input stimuli of the block used during the transient simulation can be seen in Figure 3.73. In Figure 3.73 /net16 represents the control signal V_{KONT} of the output switch. The control signal is Logic 0 active. We can easily see the effect of the control signal on the output voltage in Figure 3.72 at the time 410µs. The signals /net55, /net24, /net22, /net12, /net18 and /net32 represent the input bits b_0, b_1, b_2, b_3, b_4 and b_5 respectively. During the simulations, the positive reference voltage V_P is equal 5V and the negative reference voltage V_N is equal to 0V. As the output resistance of DAC6 varies with the input code, the conversion time of the block also is a function of the input code. The conversion time is worst for the maximum output resistance occurring when the output voltage is equal to ½(V_P-V_N) 2.5V (respective input code is "100000"). In worst case, the conversion time is less than 20ns.

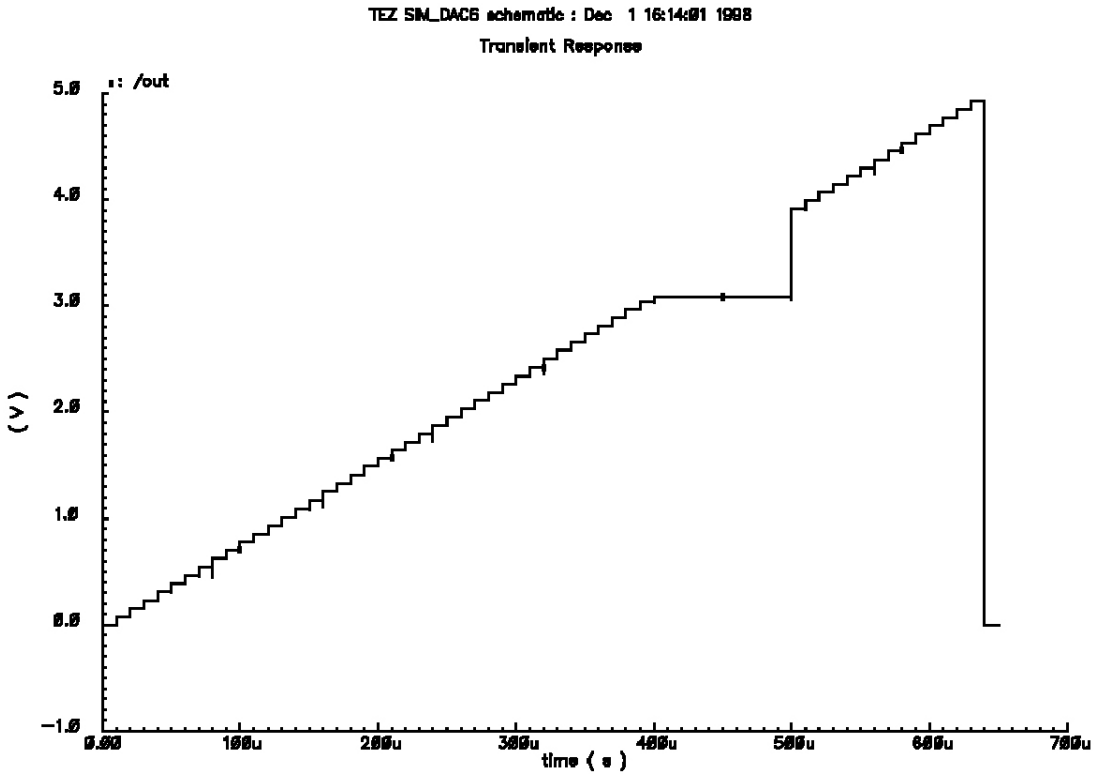

Figure 3.72 : Transient simulation result of the block DAC6

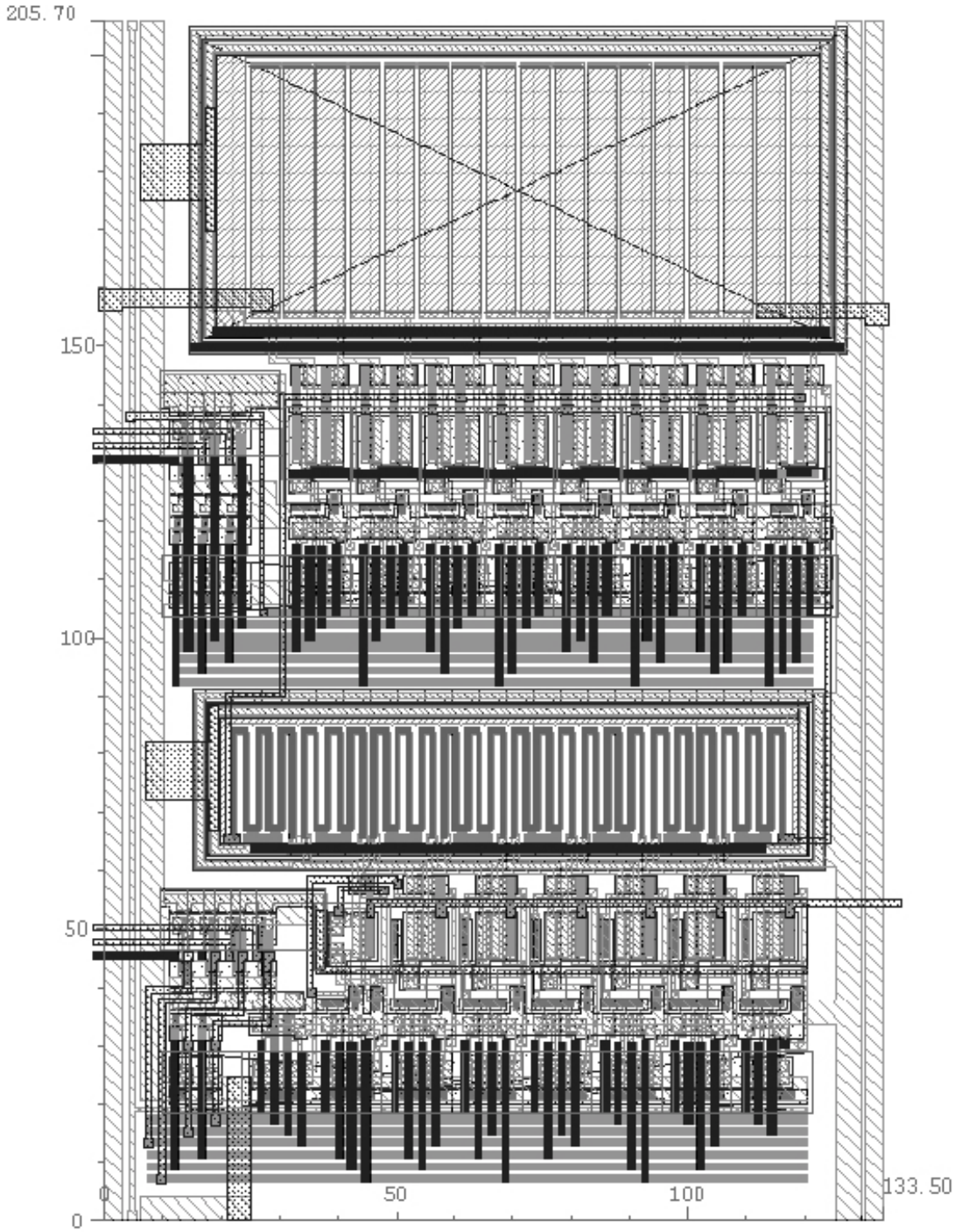

Figure 3.71 : Layout view of DAC6

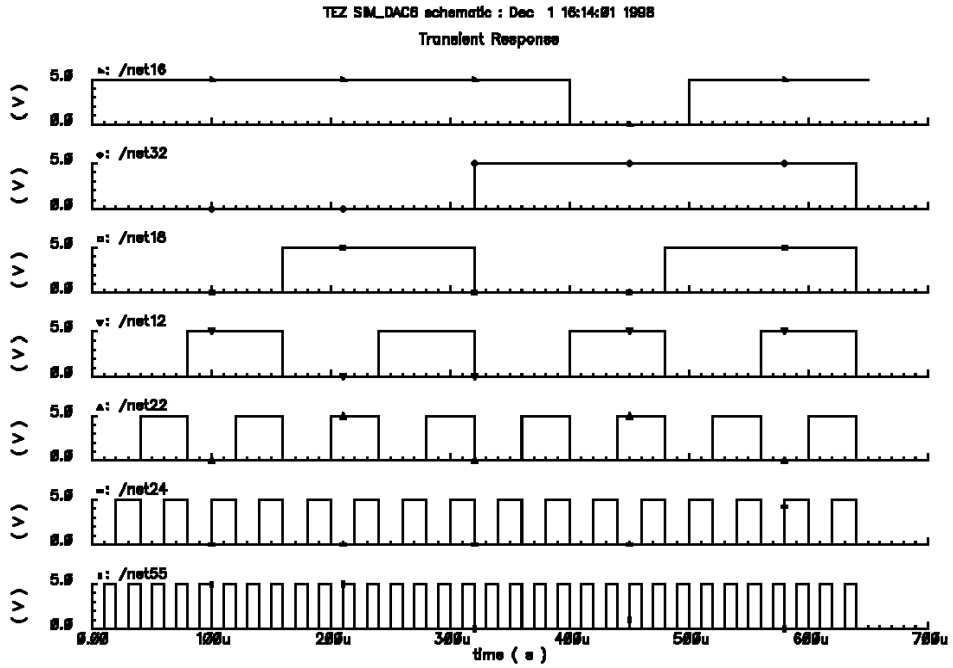

Figure 3.73 : Input stimuli of the block

As mentioned previously, the output resistance of the block is considerably large. The variation of the output voltage with respect to the output current of the block can be seen in Figure 3.74. The horizontal axis is the output current. During the DC simulation, input word is set to "100000". Thus, the output voltage must be equal to $\frac{1}{2}(V_P-V_N)$ 2.5V, which is the case when the output current is equal to 0. The output resistance is approximately equal to 5 kΩ.

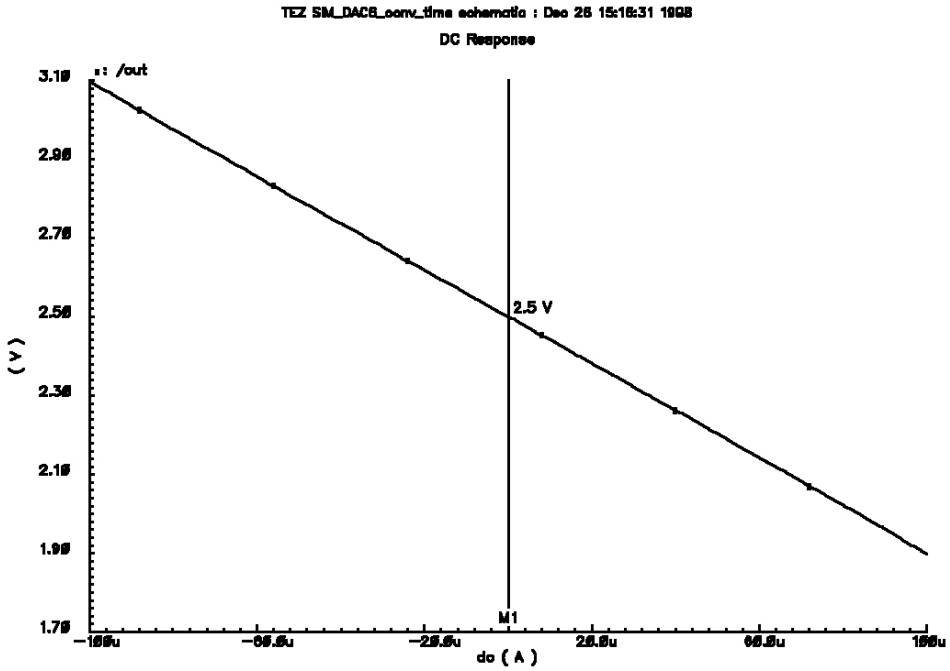

Figure 3.74 : Variation of DAC6's Output voltage with output current

For the system level simulation, a behavioral AHDL code is developed for the block DAC6. The behavioral AHDL code models the positive and negative reference voltages, the rise time and the fall time of the output voltage, the output switch and an ideal 6 bit DAC. The behavioral code can be found in Appendix G. The simulation result of the behavioral AHDL code can be seen in Figure 3.75. The input stimuli of the code can be seen in Figure 3.73.

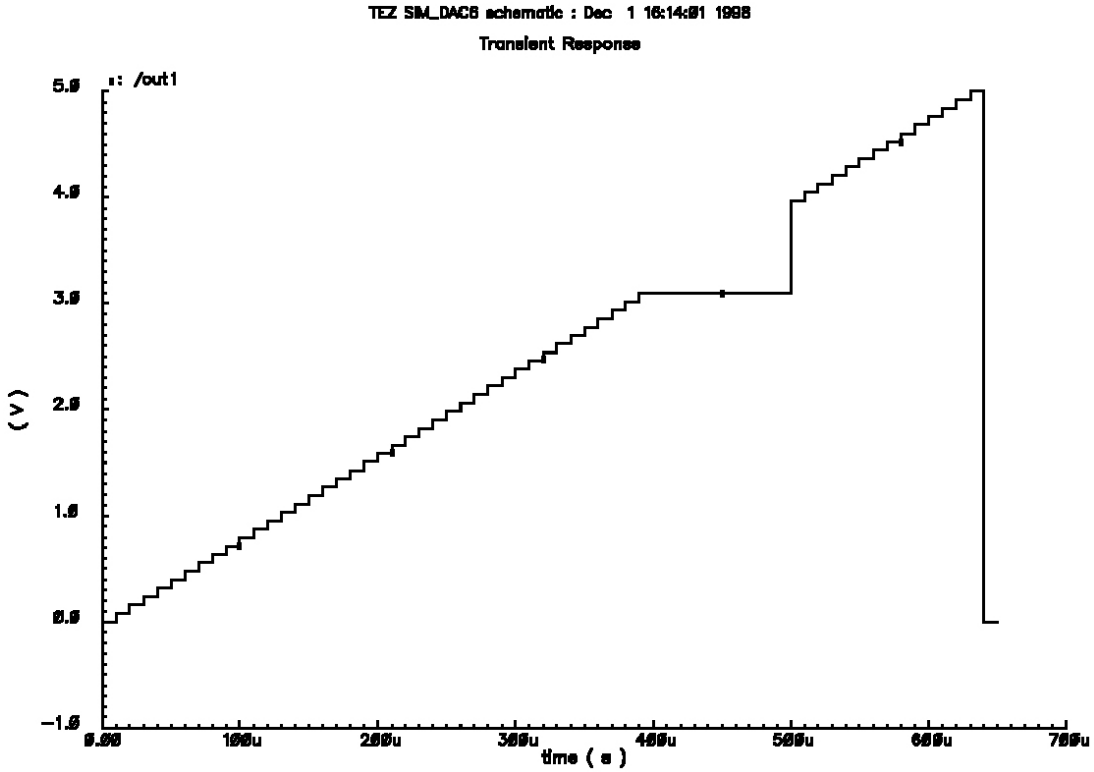

Figure 3.75 : Simulation result of DAC6's AHDL code

The integral non-linearity of the block DAC6 can be seen in Figure 3.76; The output of an ideal 6 bit DAC, the output of DAC6 and the errors are listed in Appendix J.

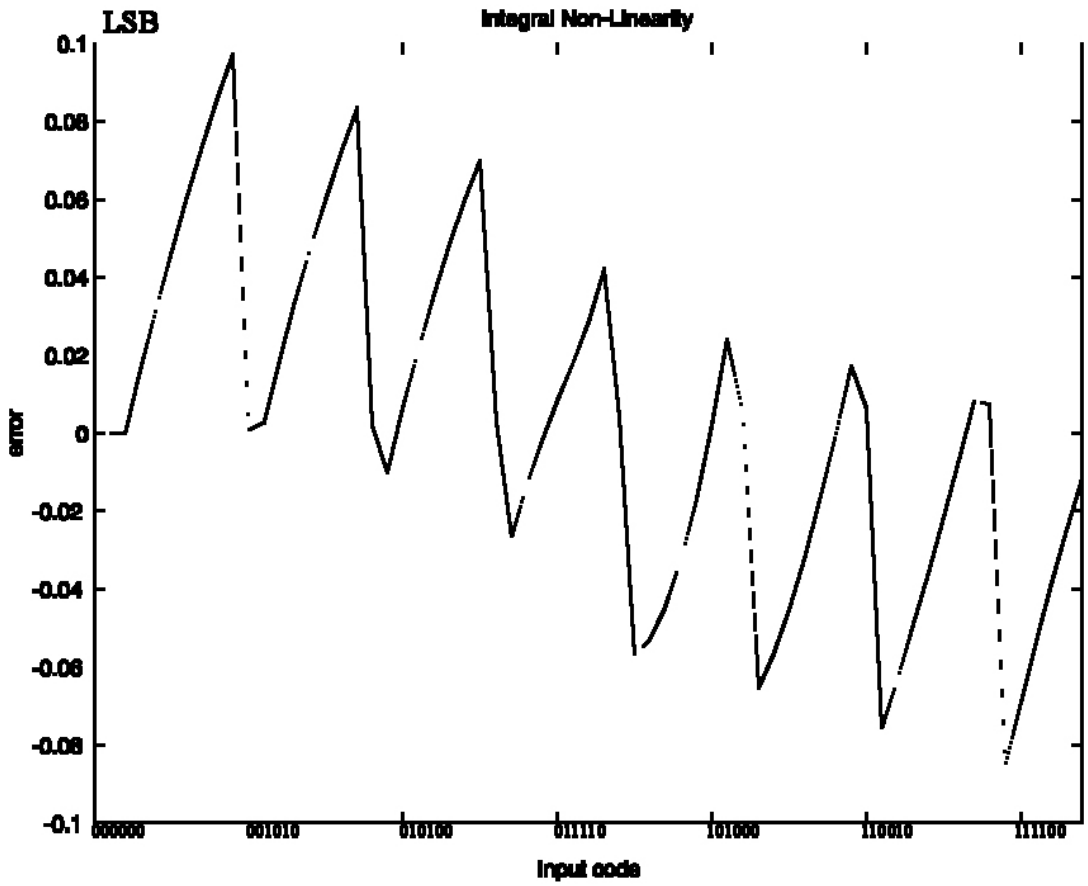

Figure 3.76 : Integral Non-Linearity of DAC6