5. CONCLUSIONS

Firstly, I will review the designed Analog Vector Quantizer system; Then I will summarize the Tree Search Structure (TSS) and the comments about the design of the Vector Quantizers whose input vector is digital. Finally, I will compare similar works with respect to their performance criteria described below.

Quantizer system can be examined with respect to 4 main criteria that are:

1. Silicon area consumption
2. Speed
3. Accuracy (resolution)
4. Power consumption

We will evaluate each building block in the Vector Quantizer system with respect to these 4 main and other system design criteria.

1. Distance Cell (DCELL)

This is the block that uses the silicon area most effectively. It is the smallest block among the system building blocks. It is convenient to high-speed applications because of its suitable circuit topology. Speed limit of the system will not originate from this block. Its input signal range is rail to rail. We can state that the resolution limit of the system will not originate too from this block. DCELL resolution is determined by the mismatch of the transistors M1, M2 and the input capacitors. Furthermore the classification process uses DCELL row's output whose resolution is multiple of number of DCELL in the row by unit DCELL resolution. If the number of DCELL in the row is not sufficiently big, we must improve the matching properties of the cell's transistors and capacitors. We must use one IN_AMP and one DAC block for

each column of DCELL matrix. Thus increasing number of DCELL in a row, that means increasing the vector size, may cause area problem. For efficient use of the system, the refresh period of DCELLs' must be sufficiently small than the operation period. We define the 'Refresh Time' as the maximum acceptable time period between two adjacent refreshing phase of the system for a proper operation and the 'Refresh Period' as refreshing phase period. Thus, the 'Efficient operation ratio' (EOR) that is defined as the ratio of Refresh Period to Refresh Time must be as small as possible. Refresh Period can be calculated as the multiple of the number of DCELL row with the clock period of the digital blocks. Clearly, increasing number of DCELL row, that means increasing the number of template-vector in template-book, increases EOR ratio. EOR is equal to 0.016 for the implemented system.

2. ROW_WTA

We must use one ROW_WTA block for each DCELL row. It consumes relatively small silicon area. ROW_AMP block of the circuits is very suitable for high-speed applications. Yet the speed of the Winner-Takes-All part depends on the number of DCELL row and the bias current I_{TAIL} of the WTA network. For high speed applications, either we must correctly select this two parameters or we must find a new WTA network topology. The resolution of the ROW_WTA block is determined by the mismatch between WTA cell's transistors and the transistors that flows bias current I_B. The resolution limit of the system can originate from this block. For the application that need higher resolution, we must increase the channel area of the transistor that flows I_B and we must either change the WTA network topology or improve the matching properties of the WTA part's transistors. The power consumption of the DCELL matrix may be calculated as follows

$$P = V_{DD}.[N.(I_B + I_K) + I_{TAIL}]$$

Where V_{DD} is the power supply voltage level, N is the number of DCELL row and finally $I_{B,}$ I_K and I_{TAIL} are the biasing current of the block.

3. IN_AMP

We must use one IN_AMP block for each column of DCELL matrix. It consumes considerably large silicon area with respect to the blocks DCELL and ROW_WTA. The settling time of amplifiers in the block can be the speed limit of the system. On the other hand, it limits also the maximum clock frequency of digital blocks. Clearly, if the settling time increases, the Refresh period increases, that means EOR ratio increases too. The open-loop gain of the OPAMP in the block decreases with increase of the frequency. Thus, the resolution of the block decreases with increase of the frequency. To determine the overall system resolution, DCELL, ROW_WTA and IN_AMP blocks must be considered together. The power consumption of the block is very high compared to blocks DCELL and ROW_WTA. With the block DAC6, they consume more than 80% of the total system power. For the applications that need higher performance, new and innovative circuit topology is needed for IN_AMP block.

4. Digital to Analog Converter (DAC6) Block

We must use one DAC block for each column of DCELL matrix. It consumes large silicon area like IN_AMP block. The conversion speed of the DAC block is the second important criteria for determining the digital blocks' clock frequency. Thus, lower conversion speed means higher EOR ratio. The resolution (input word length) of DAC block must be equal to the resolution of DCELL block. Alike the block IN_AMP, the block DAC6, due to its structure containing voltage dividers, consumes too much power compared to the blocks DCELL and ROW_WTA.

5. Digital Blocks

There are very few standard cells in the digital blocks. They do not pose any problem about system speed and silicon area. Also, they do not affect to the system resolution. The main advantage of digital Control block is its capability of asynchronous reading and writing of template-book.

6. RAM Block

The storage requirement of the system is equal to unit DCELL resolution multiplied by the number of the DCELL in DCELL matrix. The read access time of the block is the third term to determine system clock frequency. RAM block does not affect to the system resolution. Yet, as we can easily note from the system layout, RAM block consumes more than 70% of the active silicon area. We can propose 2 suggestions for implementation. The first one is leave the RAM block out of the chip, which seems very ineffective due to the large data bus and the system speed requirements. The other one is find out a new system and/or circuits topology that eliminates the need of RAM block.

As mentioned above, the block ROW_WTA mainly determines the system resolution. Especially, it is very difficult to satisfy high resolution with increasing number of template-vector (WTA input signal number). Thus, we have limited by the acceptable number of input signal (template-book size) of WTA for a given system resolution. To overcome this problem, we can use Tree Search Structure (TSS). TSS allows us to achieve easily the required system resolution and classification time for a cost of silicon area and small amount of power. Let me now briefly explain design procedure of TSS.

First, we start with designing an N input Winner-Takes-All network satisfying given resolution and speed conditions. Obviously N is smaller than the template-book size M. Then, we group template-vectors into subsets containing N of them. Thus, we obtain M/N new subsets. We represent each of them by a new template-vector calculated as weighted average of their template-vectors. Therefore, we obtain a new template-book containing M/N template-vector. We repeat this grouping procedure with the new template-book until the last template-book contains less than (or equal to) N template-vector. Each division represents a new hierarchy in the tree. For example, let's say our initial template-book contains 256 template-vector (M=256 and the required resolution is 8 bits) and designed WTA has 4 input (N = 4). Thus, the tree has 4 hierarchies. Figure 5.1 illustrates TSS for the given example.

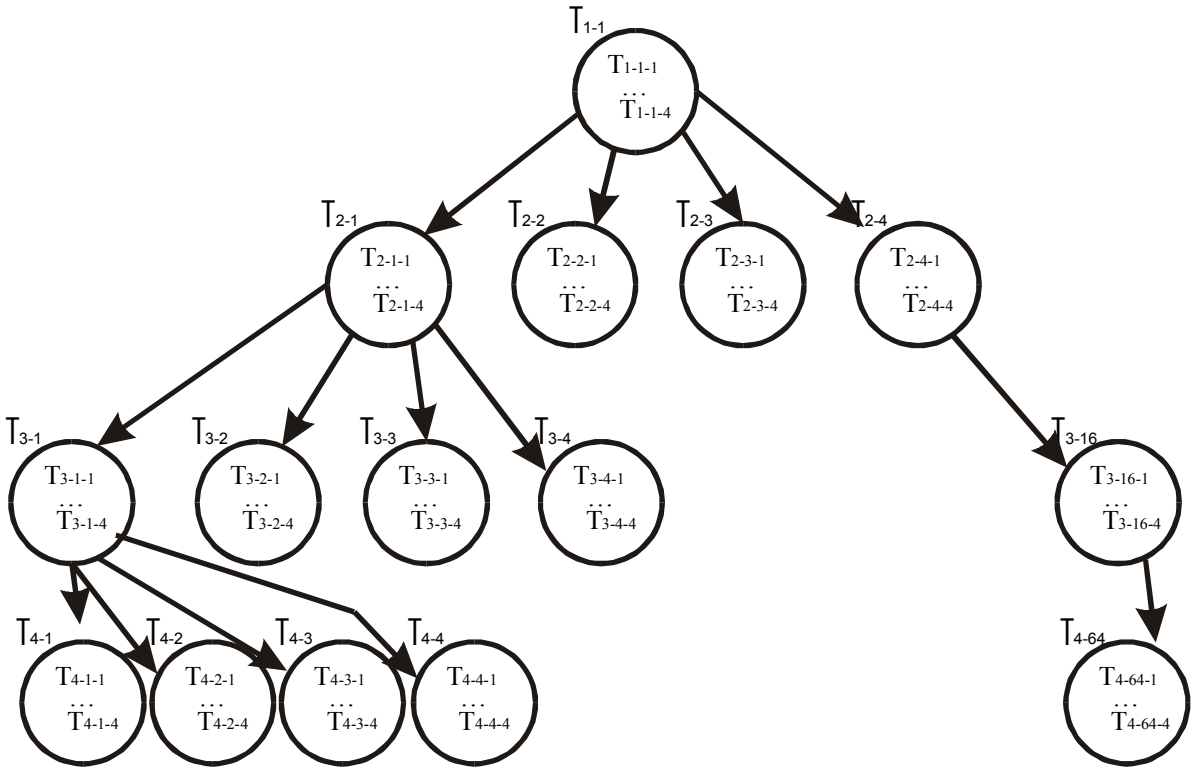

Figure 5.1 Tree Search Structure for N = 4 and M = 256

In Figure 5.1, T_{I-J} represents the j^{th} template-book in the I^{th} tree hierarchy. T_{I-J-K} represents the K^{th} template-vector of the j^{th} template-book in the I^{th} tree hierarchy. Thus, at the end, we face with 85 (64+16+4+1) sub-template-books (WTA network) and each of them contains only 4 template-vectors. Globally, there are 340 template-vectors. Therefore, we have added 84 new template-vectors. The original template-book constitutes last hierarchy of the tree. Let me now explain the search mechanism of the structure.

All of the computations are concurrent. Thus, once the input vector is applied to the inputs of the matrix, each individual WTA network selects the best-matched template-vector among its 4 inputs. Then, a digital block determines the correct winner by following the tree structure. I must note that lower WTA resolution can be tolerable except at the last hierarchy of tree. In our example, required resolution for the first hierarchy is only 2 bits, for the second hierarchy 4 bits, for the third hierarchy 6 bits and for the last hierarchy, it is 8 bits.

As we go to higher hierarchies, the distances between template-vectors increase. Therefore, input signal differences of the WTA networks increase too and the networks respond faster. Thus, assuming that the delay of the digital block can be

neglected with respect to the delay of the WTA network, we can say that the classification time of the system is equal to the classification time of a single 4-input (N), 8-bits ($\log_2(M)$) resolution Winner-Takes-All network.

For large number of template-vector, Tree Search Structure allows us also to use multiple Vector Quantizer chips concurrently. Obviously, tree structure is constituted with the multiple identical VQ chips containing one of the template-books of the structure.

Let us now examine the VQ system whose input signals are digital. With respect to the silicon cost and the speed limits of the Vector quantizer system, digital input signals are preferable. Assuming that input and template-vectors have n elements and each vector element is constituted by m bit, new system DCELL matrix row size is $n.m$. The input and template-vectors are constituted by $n.m$ bit too. Thus new system DCELL matrix is (m-1) times larger than the old one. However, this cost is tolerable with the other benefits of the modification. Firstly, the analog block IN_AMP that drives V_{IN+} and V_{IN-} terminals of DCELLs on each column of DCELL matrix becomes to a simple digital block that contains an inverter and a buffer. It is obvious that inverters and buffers work faster than an amplifier that contains a feedback loop. Furthermore, as the template-vectors are digital signals too, we do not need the DAC blocks at the output of the RAM.

With that new configuration, the system can classify inputs with respect to the Hamming distance between input and template-vectors without any other modification. Yet with some small modifications on the system architecture and properly selecting the template voltages written on the DCELL, classification can be made with respect to the digitally coded 'Manhattan distance' between input and template-vectors. The weightiness of vector elements' bits is realized by correctly selecting template voltages. At this point, we have to make a distinction between template-vector and template voltage. Template-vector is a digital vector in the template-book and composed by n vector elements that has m bits. Template voltages are the voltage levels written in the DCELLs with the procedure described in section 3.1 (first phase) to realize vector element bits' weights at the output of DCELL blocks. To prevent mistakes, we define template voltage as 'Programming Voltage'

(PV). Let me now explain the procedure to measure the distance between input and template-vectors.

We will write the same PV to the DCELLs that process the template bits that have equal weight. For the reason that vector elements have m bits, we need m different PV level. If the template-vector's bit in the DCELL that we examine is Logic1 (LH–5V) and the weight of the bit is $2^{(i-1)}$ and $i \in [1..m]$, during the refresh period, we have to apply PV_i and Logic0 (LL–0V) to the terminals V_{IN+} and V_{IN-} respectively. If the template-vector bit of the DCELL that we examine is LL and the weight of the bit is $2^{(i-1)}$, during the refresh period, we have to apply LL and PV_i to the terminals V_{IN+} and V_{IN-} respectively. Programming voltages PV_i $i \in [1..m]$ can be calculated as follows:

$$PV_i = \frac{C_T}{C}\sqrt{\frac{2^i}{\beta_{M1}}}I$$

In the previous equation, C represents the input capacitance of DCELL, C_T represents total capacitance of node N1 (or N2) in DCELL, I represents the precision current of WTA network at the output of DCELL rows. Under these conditions, the DCELL row current can be calculated as follows:

$$I_{DCELL\_ROW} = \left[\sum_{j=1}^{m} \left(\sum_{k=1}^{n} \left| b_{IN(k,j)} - b_{TEMP(k,j)} \right| \right) 2^{(j-1)} \right] I$$

In the previous equation $b_{IN(k,j)}$ represents the j^{th} bit of k^{th} input vector element and $b_{TEMP(k,j)}$ represents the j^{th} bit of k^{th} template-vector element. This is Binary Coded Manhattan Distance between input and template-vectors.

It is obvious that the refresh time calculated in Section 3.1 is invalid because of the different weights of DCELLs. The refresh time must be recalculated with the condition that the error current caused by the most significant bit's DCELLs must be equal to (or less than) ½ I.

If we reexamine how DCELL work during the operation (second) phase under the previous conditions, we will remark that only one of the cell's output transistors flows current with respect to if DCELL's template-vector bit is LL or LH. With a new DCELL circuit topology, this situation allows us to evaluate to the new VQ system that has not got RAM block and its refresh time is as short as one single clock cycle.

Implemented system can be easily converted to Kohonen's Self-Organizing Feature Map. Obviously, extra circuits are needed to calculate neighborhood function and update template-book. The comparison between similar works can be seen in the following tables. VQ core size includes Distance matrix, WTA network and the Encoder block.

Table 5.1 Comparison between similar works

Reference Number	[32]	[11]	[9]	[10]	[12]
Technology (CMOS)	1μm	2μm	2μm	2μm	2μm
VQ Core Size (mm^2)	8.7 x 7.7(1)	4.6 x 6.8	2.2x 2.25	--(2)	2.2 x 2.2
Code Book Size	256	64	16	--	10
Vector Size	16	25	16	--	12
Resolution (bit)	8	7.5	5	7½	3
Classification Time	678ns	500ns	3us	--(NM)	30 μs
Distortion Measure	SED	SED	MD	MD	MD
Power Consumption (mW)	500	>0(NM)	0.7	--(NM)	→0(NM)
Synapse Densities (mm^{-2})	--	200	213	33	190
Design Methodology	DIG	CT	SA	SA(3)	SA(CB)

Table 5.2 Comparison between similar works

Reference Number	[16]	[33]	This work
Technology (CMOS)	2μm	2.4μm	0.6μm
VQ Core Size (mm^2)	0.414	--(NM)	0.714x0.891
Code Book Size	10	10	64
Vector Size	10	15	18
Resolution (bit)	1	1	6
Classification Time	90ns	100ns	100ns
Distortion Measure	HD	HD	SED, MD, HD
Power Consumption (mW)	→0(NM)	11	10.2
Synapse Densities ($mm^{-2)}$	190	--(NM)	4723
Design Methodology	SA(CB)	SA	CT

SED : Squared Eculidean Distance
MD : Manhattan Distance
HD : Hamming Distance
DIG : Digital
CT : Continous Time
SA : Sampled Analog
SA(CB) : Sampled Analog,Charge Based
NM : Not Mentioned

(1) Including system RAM block used to store template-book and other system control circuitry
(2) Only the distance cell is presented. Vector Quantizer system is not implemented
(3) Proposed system operates with the pulse stream representation of the input and template signal

Finally, in this thesis, a Programmable CMOS Analog Vector Quantizer system was designed and implemented with AMS 0.6μm CUQ double-poly, double metal technology. The chip area including the bonding pads is 4.1mm x 3.7mm (15.17 mm^2). The implementation faces the classical problem: The lack of a practical analog memory. The active area is considerably small with respect to other implementations. We tried to show the directions for the future works. Performances, functions, advantages and disadvantages of each building block of the system are analyzed. Block level and system level design procedures are summarized.