3. BUILDINGS BLOCKS

Up to here, I have examined the architectural structure of the Vector Quantizer system. I defined the functions realized by the building blocks of the system. In the sections of this chapter, I will analyze in detail the functions, performance limits and the implementations of the building blocks. I start to analyze with the key block of the system, which is Distance Cell (DCELL). Then, I will continue to analyze the blocks in the sections Row Amplifier (ROW_AMP), Row Winner-Takes-All (ROW_WTA), Input Amplifier (IN_AMP), Digital to Analog Converter (DAC6), Digital blocks & RAM block and finally Test blocks.

All the analog simulations are run on the extracted view of the blocks. I used simulator SpectreS© of Cadence® for analog simulations. Digital blocks are designed using VERILOG Hardware Description Language (VERILOG-HDL©) and the codes are synthesized using SYSNOPSY®. VERILOG-XL© of Cadence® was used for digital simulations. Components' typical mean and Monte-Carlo model parameters for AMS 0.6 m CUQ double-poly double-metal process can be found in Appendix I. All the numerical computations were done using MATLAB© of MATH WORKS® and all the symbolic computations were done using MATEMATICA© of Wolfram Research®.