11-BITS SUB-RANGING ANALOG TO DIGITAL CONVERTER AND SSATOOL

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I would like to dedicate this work to my parents,

Nermin and Ibrahim AKSIN.

11-BITS SUB-RANGING ANALOG TO DIGITAL CONVERTER AND SSATOOL

by

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DISSERTATION

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PREFACE

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In this work, an 11-bit Sub-Ranging Analog to Digital converter (ADC) is proposed for power management applications. Designed converter implements all important design specifications of an ADC used in such applications should satisfy, i.e. low power consumption, noise immunity, being able to measure voltage quantities above the power supply voltage such as battery. Proposed ADC can sample voltage quantities above supply voltage using a new bootstrapped sampling switch. A new passive subtractor circuit is also implemented to reduce total silicon area and improve noise performance of the converter. Proposed passive subtractor inherently implements filtering which is very suitable when a DC voltage quantity should be measured in a noisy environment, such as power management systems where high-power switching voltage regulators are generally present. The 11-bit ADC is designed using Texas Instruments LBC7 0.35 μm technology. Consistent with the application, designed analog-to-digital converter does not contain any sample and hold amplifier, hence it is intended to monitor DC voltage quantities. The conversion time is specified as 10 μs with an expected duty cycle of 0.1%. The converter draws 140 μA average current during conversion from 2.75V single power supply, including reference buffer. Full scale range of

the converter is twice of the power supply voltage, i.e. 5.5V. The main design challenges addressed with this design are: 1. the development of very low-power circuit techniques that enable precise sampling of input signal exceeding supply voltage without forward biasing any parasitic body diodes, 2. guaranteeing reliable operation of the devices within this system in which high voltage levels are present, 3. achieving true rail-to-rail signal processing in a single-ended system, 4. achieving 11-bits resolution in a very noisy environment, 5. low power consumption.

The second topic that this dissertation will address is the development of a symbolic small signal analysis program for linear and non-linear analysis of arbitrary circuits and systems. Symbolic Small Signal Analysis Tool (SSA Tool) is a general purpose tool that calculates small signal response of any given circuit or system symbolically. Matlab and Cadence DFII environments are used as design environment of the tool. The stability analysis of the low drop out voltage regulator designed for the reference signal generation of the analog to digital converter is carried out using SSA Tool. Basically, SSA Tool extracts symbolic node equations from the input that contains the circuit description, and solves the symbolic linear node equation system. The tool is also capable of solving second and third order harmonic and/or inter-modulation distortion responses of any given circuit, provided that the netlist contains required non-linearity calculation related coefficient variables. Using SSA Tool, it is possible to analyze linear and/or non-linear responses of any discrete time systems such as switched capacitor (SC) filters or sigma-delta ($\Sigma\Delta$) modulators. SSA Tool contains several analysis modules to ease sigma-delta modulator analysis, transfer function analysis, impedance/admittance analysis, etc... Developed modules and analysis tool is capable of analyzing symbolically the effects of the linear circuit non-idealities such as finite DC gain of the amplifiers or mismatch error, as well as non-linear large signal errors such as amplifier slew-rate or DAC non-linearity.

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CHAPTER 1

INTRODUCTION

1.1 Motivation and Focus
or A Prayer for the Digital World

The *digital revolution* of late 20th century brought fast, reliable, flexible and very cheap signal processing to electronic systems, thanks to Digital Signal Processors (DSP). Actually, digital technologies took over a wide range of applications that are classically implemented with analog circuit techniques.

There are, of course, a lot of good reasons for the widespread acceptance of the digital technologies by the electronic industry and by all of us as consumers. Better noise immunity, easy IP reusability, easy and very systematic design (thanks to hardware description languages - HDLs), mostly automatic layout generation with digital cell library concept and Place & Route algorithms and tools, shorter time to market and easy design and debugging using Field Programmable Gate Arrays (FPGA) are just few examples that helped digital technologies to become the legend that they are now. With every new integrated circuit fabrication technology node, the efficiency, the speed and the integration level of the digital systems improved at a breath taking rate as predicted by Moore's law.

The main challenge facing the modern digital system design is the exponential growth of the power consumption with increasing complexity, integration and operating frequency. For a modern micro processor, a power consumption of tens of watts is an accustomed number. This brings us to the famous switching power consumption equation with which the power dissipation of a digital system can be estimated:

$$P = \frac{1}{2} C_{tot} f_{clk} V_{dd}^2 \tag{1.1}$$

where C_{tot} is the average load capacitance that change state with clock frequency f_{clk} and V_{dd} is the supply voltage. Since, it is desirable to increase the clocking frequency to operate the system faster and faster, the other two parameters are traditionally used to reduce the system power dissipation. Reducing C_{tot} is addressed with improving technology nodes (faster and smaller transistors and lower parasitic capacitance) and with use of proper circuit techniques (such as disabling idle blocks). Reducing power supply voltage is particularly attractive in this battle because of its quadratic dependency to the power consumption. Hence, the trend

is to operate the digital systems with as low power supply voltage level as possible.

Despite their reliability, competency and all the wonderful features that I already mentioned, digital systems have to coexist together with analog circuits, at least within the data converters, for foreseeable future. The need for mixed-signal circuit design arises simply because *the world is analog.* A typical signal processing path is shown in Fig. 1.1. The real world analog signal, continuous in time and amplitude, is first sampled and quantized, in other word digitized, using analog to digital converter (ADC). After processed by DSP, the digital output signal is converted back to analog domain using digital to analog converter (DAC) to interface again with the real world. Thus, the data converters are essential parts of the digital signal processing path. Of course, the global accuracy of the output signal is set by the block having the worst accuracy within the path. In reality, the accuracy is bounded either by the accuracy of the DAC at the back-end or the accuracy of the ADC at the front-end. Hence, the current work is to improve the performance of the data converters in terms of resolution, as well as speed and power.

Figure 1.1. Typical signal processing path

The domination of the digital systems and their ultimate shortcoming of power consumption are forcing the coexisting analog systems and sub-blocks to operate under, so called *digital* conditions. With the inevitable shift of the signal processing from analog domain to the digital domain with the help of the data converters and DSPs of course, the integrated circuit (IC) fabrication processes are optimized more and more for digital resulting very poor transistors for implementing analog blocks. I already mentioned about decreasing supply voltage level, which does not necessarily mean lower power consumption for the analog blocks (in fact the opposite is true for most of the cases). The analog blocks should endure and provide required accuracy under heavy noise created by the digital circuitry and injected from the rails and the bulk of the IC. Improving the resolution or getting similar resolution while the supply voltage is decreasing and the noise level is increasing is an enormous challenge for data converter systems. Ironically, the very same technology for which the data converters exist today is their worst foe in terms of performance.

Under such harsh operating conditions, the main design tools of the analog designers are of course circuit simulators. Growing complexity of the implemented systems that

contain both digital and analog blocks and the pressure of time-to-market force the designer community to use the available analysis tools more effectively. This is simply due to the fact that the transistor level simulation time of even moderately complex system is unacceptably long. System level abstraction or high level functional modeling is widely used for speeding up the numerical simulation while keeping the accuracy compromises in acceptable level. Today, system level simulation methodologies and system level modeling are playing major role within mixed signal design flow, especially in data converter design, and it is still a very hot research topic.

In short, modern digital technologies require: fast, high resolution, low power, noise immune analog to digital converters designed for cheap digital processes and reliable design tools to facilitate their design for harsh environmental conditions.

The ever decreasing supply voltage level is a particularly troublesome constraint for data converter designers. The reason is that, as will be clearer later on, most of the performance parameters of the data converters are directly related to the supply level and having higher supply voltage gives designers an extra freedom during the optimization of the performance (i.e. linearity, speed, resolution, etc...) and the cost (power consumption, silicon area, etc...) of the systems.

Increasing the effective number of bits of data converter becomes especially difficult with lower supply voltage level. Apart from few special circuits, traditionally, the signal amplitudes within circuits are bounded in between the rails. Parasitic body diodes of the transistors act as a signal clamper and limit allowable maximum input signal level. The data converter designers that are already restricted with an upper bound set by the power supply level have nothing but to seek the extra bit (extra resolution) by decreasing the least significant bit (LSB) level which is more and more difficult to obtain with increasing level of noise.

The content and the motivation of this work are the design of an analog to digital converter that will solve above mentioned dynamic range improvement problem using a new approach and the development of a circuit/system analysis tool that is integrated to standard IC design flow and is capable of design and optimization of data converters. In summary

The focus of this dissertation will be first, on the development and the design of a concept analog to digital converter (targeted primarily for very noisy power management ICs or PICs) that solves power, input signal range and resolution (accuracy) trade-off[1] and improves the ADC's noise immunity and next, on the development of a symbolic circuit analyzer for linear and nonlinear analysis of circuit and systems, with special emphasis on analog to digital converter design (particularly $\Sigma\Delta$ modulator design).

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[1] *this trade-off will be discussed in more detailed within the section 1.3.1*

1.2 Content of the Work
and Design Challenges

As mentioned above, the focus of this dissertation will be on two distinct problems of data converter and in general, analog circuit design:

The first problem is the design of an ADC that is capable of sampling and converting input signal levels beyond the power supply range without any signal conditioning (i.e. attenuating the input signal) and reliability problem. This is achieved using novel high voltage bootstrapped sampling switch and high voltage passive subtractor circuitry. Main application field of the designed ADC is the precise battery monitoring/gauging within a very noisy power management IC. Even though current application aims at power management systems in which input signal bandwidth is generally very low, proposed sampling switch can also be used for high sampling rate ADCs, such as pipelined ADCs. The input signal range of the proposed high voltage switch is limited with the drain-bulk breakdown voltage of the used transistors; hence using special design techniques and/or drain extended devices if available, it can be made very large.

A modern power management IC (PIC) system and its floor plan are shown in Fig. 1.2. The PIC contains several switching voltage regulators (i.e. buck, buck-boost, etc...), linear voltage regulators (i.e. LDOs), high power switches (i.e. hard disk drive switch, LCD switch, etc...), analog to digital converter, time reference and voltage reference circuitry, digital control core. The data converter within the system is designed for monitoring on chip as well as off chip signals. The range of these signals can exceed on chip supply voltage level (for example while monitoring off chip supply line). A closer look to the chip floor plan will reveal that most of the real estate is occupied by the power transistors and the voltage regulators.

The requirements and the relevant performance parameters of the analog to digital converters designed for power management systems are quite different than the ones designed for signal processing systems. These converters are mostly designed for monitoring (precise battery gauge, precise temperature monitoring, etc...) and detecting (accessory detection, DC signal detection, etc...) purposes. The input signal of the ADC in most of the case is DC. Hence, generally speaking, there is no need for sample and hold amplifier at the input. Typical conversion time of these converters may vary from 50 microseconds to 100s of milliseconds. Required dynamic range also is not very high compared to modern signal processing ADCs. Typically, required resolution of the power management ADCs ranges from 8 to 11 bits. The design challenges regarding to the design of power management ADCs are

Off Chip Power Sources

uP

On Chip Inputs

Off Chip Inputs

I2C Interface

ADC

Voltage & Time References

Battery Charger

Digital Supervisor

Buck Regulators

Boost Regulators

Linear Regulators

(a)

Buck Reg.1

Buck Reg.2

Boost Reg.1

Battery Charger

I2C + Digital Core

POWER SWITCH

Boost Reg.2

ADC LDO

EEPROM

BIAS

RTC LDO

ADC

LDO1

LDO2

LDO3

LDO4

RTC

(b)
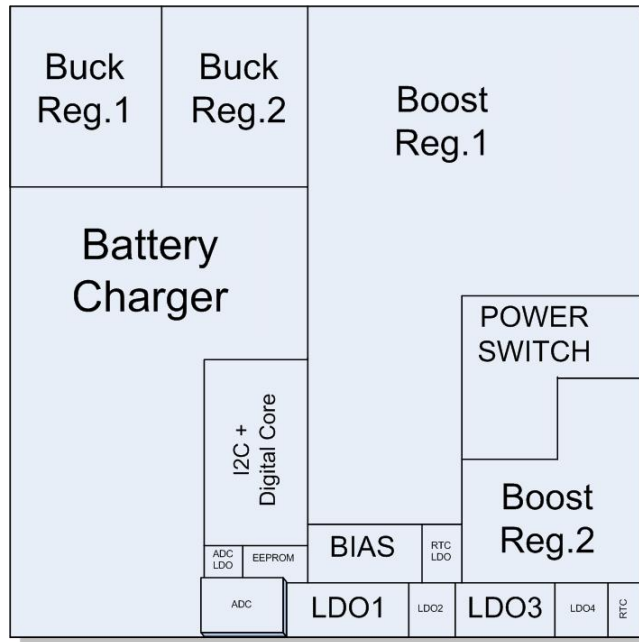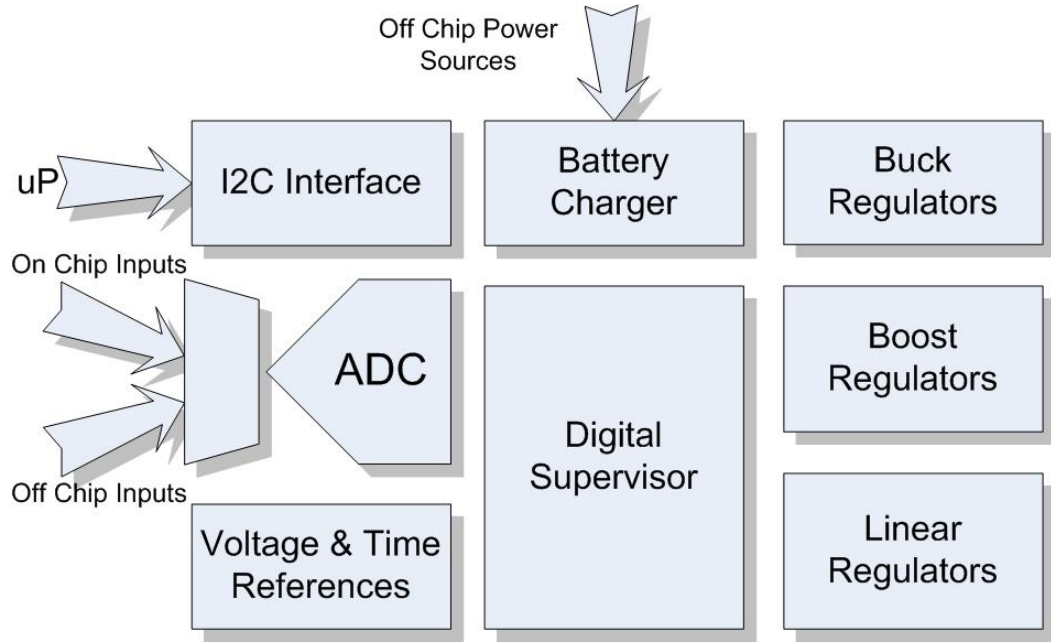
Figure 1.2. A modern Power Management IC, (a) Typical System Block Diagram, (b) Typical Floorplan

1. Sampling input signal that may exceed Supply Voltage

   This need arises from following facts: First, as discussed previously, in order to improve power efficiency it is highly desirable to operate the system with as low of a power supply level as possible. Hence, power management system's supply voltage levels are generally chosen much lower than the surrounding systems to decrease the power consumption or equivalently improve the efficiency. Second, in modern power management systems, there are no one single power line that can be identified as the maximum voltage within the system. The power of the system might come from one of multiple batteries, USB port or AC wall power, etc... Therefore, there is no definite identifiable supply line. It should be noted that the ADC has to monitor all these signals at the same time.

   Sampling and digitizing input signal exceeding supply voltage, on the other hand, is not as easy as it is said. The input switch (or whole ADC) should sample the input without forward biasing any parasitic body diodes, without any reliability problem and of course without degrading the input signal itself. As it will be detailed in chapter 2, traditionally, this problem is solved by attenuating the input signal so that attenuated signal fits within the rails. Here, a more fundamental approach adopted to solve this problem. Proposed ADC samples and digitizes the input signal as it is without any problem cited above.

2. Achieving targeted resolution within a very noisy environment

   In general, power management systems, as seen from Fig. 1.2(a). contain several high-power switching voltage regulator, linear voltage regulators (i.e. LDOs), high-voltage power switches, charge-pumps, of course, a digital control core. All these blocks act as a noise source within the system. They inject noise to the supply lines; they inject noise to the die bulk. It is easy to estimate the seriousness of the noise problem by simply comparing the silicon area of the data converter[2] in Fig. 1.2(b) with the remaining of the system. In such a noisy environment, it is not trivial to achieve millivolt level resolution. The task becomes even more difficult, if the input signal is attenuated to fit within the rails because the LSB becomes even smaller for a given resolution (or number of bits).

3. Low power consumption

   Typically, the power consumption of the data converter is not as important as the other two parameters within power management systems. Since their main role is monitoring of near DC signals, the duty cycle of the ADCs are generally very low, typically 0.1 % or even less. However, for the next generation power management systems in which the

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[2]the block slightly raised

signal processing is needed more and more (for power line communication for example), the duty cycle of the data converters expected to get higher. That will certainly put more emphasis on the average power dissipation of the ADC which determines ultimately the efficiency of the whole system.

Second part of the work presented here consists of the development of symbolic small signal circuit analysis tool or in short, *SSA Tool*. The domination of the numerical simulators created the misperception that the numerical results are good enough for proper design of analog circuit and system. Although the importance of numerical results is undeniable, the numerical results can never provide the deep insight that symbolic analysis can, about the circuit that is analyzed. Small signal analysis and signal flow graph analysis techniques can be used to analyze and optimize a wide range of circuits and systems, such as amplifier, continuous or discrete time analog filter, matching network, $\Sigma\Delta$ modulator, etc... Nowadays, analog designers tend to use small signal analysis technique less and less due to the facts that obtaining the results is very lengthy and rather error prone process. Therefore, it is necessary to develop a user friendly and graphical symbolic analysis environment to reintroduce symbolic analysis techniques to standard circuit/system design flow.

Special effort spends on integrating the SSA tool with standard IC design softwares, i.e. Cadence DFII design environment and Matlab. The tool is developed using Matlab symbolic toolbox. Interface software developed within Cadence to export the data to Matlab. The tool uses Cadence Virtuoso Schematic capture tool as main interface to enter circuit netlist. Alternatively, it is also possible to use Matlab Simulink interface or custom circuit netlist text file to describe the circuit to the tool. The circuit netlist, after created, is post processed by the SSA tool to extract symbolic node equations and to solve obtained linear equation system. The tool can also calculate distortion and intermodulation distortion transfer functions of arbitrary circuit and systems provided that the circuit netlist contains appropriate nonlinearity parameter set.

One of the fundamental issue of the symbolic analysis is the complexity of the final results. The solutions of even moderately large circuit can be extremely complex. The symbolic analysis is generally carried out to obtain better understanding of the circuit dynamics. Of course, it is impossible to interpret or understand the behavior from pages long expressions. One of the hot research area related to symbolic analyzers is the development of suitable simplification techniques. There are several approach addressing this problem. One approach, for example, to use circuit's DC operating point analysis results to eliminate or to ignore some of the parameters before hand during the analysis. Although, this approach is very effective in analyzing small size circuits, such as amplifiers, it is ineffective for analyzing systems in which sub-blocks are rather defined with high level parameters (such as gain

bandwidth product) and not with the operating point parameters.

SSA tool approaches to this problem from a different angle. Analog designers use their a priori knowledge and expertise to solve specific problems. Classification is a very important step in this process. Classification narrows the solution space and allows the designer to select proper approach to the problem. This is the approach adopted here. SSA tool will show how powerful can be the a priori knowledge of the circuit (or system) during the simplification. A special module as a part of SSA Tool is developed to ease $\Sigma\Delta$ modulator analysis and design. It is possible to use this automated tool to analyze arbitrary modulator as well as its circuit nonidealities. SSA tool simplifies the analysis results significantly by exploiting the properties of $\Sigma\Delta$ modulators and extracts relevant high level performance parameters, such as in band noise power, modulator order, etc...

SSA tool is also used during the stability analysis of the Low Drop-Out Voltage regulator (LDO) of the proposed ADC.

1.3   Contributions

As pointed out within the section 1.2, the content of this dissertation is first, design of a low-power, wide input signal range analog to digital converter for power management ICs and second development of symbolic circuit analyzer tool for linear and nonlinear analysis of arbitrary circuit and system with special emphasis on ADC design. The contribution of the designed PIC ADC to the state-of-the-art will be in two levels:

- Circuit Design Level

- System Design Level

At circuit level, two novel circuits designed for high-voltage sampling, i.e. high-voltage bootstrapped sampling switch, and high voltage signal processing, i.e. high-voltage passive subtractor (HPS). Between these two circuits, high-voltage sampling switch is especially important because of the unforeseen implications that it created at system level design simply by its existence. I will review these new concepts in more detail within subsection 1.3.1.

The passive subtractor on the other hand is somewhat an exotic circuit proven to be extremely useful and accuracte in high-voltage single-ended signal processing. Main feature of this simple passive circuit is that it operates rail-to-rail with the true meaning of the word.

In differential systems, the input signal is defined as a difference of two complementary signals, as a consequence of this, the common mode level (or equivalently ground level) of the input signal can be chosen arbitrarily so that the amplifiers within the system can be properly biased. For single-ended systems, on the other hand, the input ground level is

literally the ground of the whole system and obviously, it is impossible to process any signal at close proximity of the ground with a feedback amplifier circuit. The passive subtractor circuit, as its name suggests, is a passive circuit that takes the difference between two input signals and its output can vary between literally rail-to-rail[3]. Passive subtractor uses also novel high-voltage bootstrapped switch.

The contribution of the SSA tool will be rather indirect. There are several symbolic circuit analyzers presented in the literature. While these stand-alone engines are optimized to solve a broader range of generic problems in terms of circuit and system or in terms of simplification and processing methodologies, SSA tool's main target is the development and integration of the tool to the standard IC design flow and the development of knowledge based specialized extension module development, such as $\Sigma\Delta$ modulator design module, noise analysis module. I can cite the symbolic nonlinear analysis of arbitrary $\Sigma\Delta$ modulators as the main indirect contribution of the SSA tool to the state-of-the-art. Using the nonlinearity analysis module of SSA tool, it is possible to calculate symbolically the effect of any weak nonlinearity present within the modulator topology, such as feedback DAC nonlinearity, sampling switch nonlinearity, amplifier slew rate, amplifier DC gain nonlinearity, etc... in terms of Signal to Noise Ratio (SNR) and Spurious Free Dynamic Range (SFDR) degradation. Proposed nonlinear analysis technique allows the designer to optimize the modulator in terms of area (matching of the DAC capacitors), in terms of power (amplifier slew-rate), in terms of circuit topology (amplifier DC Gain nonlinearity), etc... and provide a starting point to system level numerical simulations.

1.3.1 High-Voltage Bootstrapped Sampling Switch: New Horizon in ADC System Level Design

Generally speaking, power supply voltage levels are the ultimate boundary of the signals within a circuit. The basic reason for this fact is that while a signal goes below negative supply voltage level, since the NMOS transistors within the system share the same bulk biased with the negative supply voltage, the parasitic body diodes of NMOS transistors turn on and start conducting huge amount of current. Similarly, the body diodes of PMOS transistors are forward biased while a signal goes above positive supply voltage. Hence, classically, the power supply voltages put an upper limit to the maximum swing of any given signal within the circuit.

System engineers while optimizing different parameters and selecting some others have to consider the signal swing. The input signal swing of the system, for instance, cannot be

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[3]The output of the circuit is clamped at one diode below the ground level. The upper limit is the drain-bulk break down voltage of the used transistors.

larger than the supply voltage as it is in the case of the power management system ADC because the parasitic diodes associated with the transmission gates used to sample the input will be forward biased.

The designer, classically, has two choices to overcome this problem: 1. Increase the power supply voltage of the whole system to match the input signal range; or 2. Attenuate the input signal so that attenuated signal fits in between rails. Although, any one of these options can help to fix signal clamping, they are not elegant solutions to the problem because of the classical trade-off among power dissipation, input signal range and input signal resolution.

It is obvious why the system designer would not like to increase the power supply voltage to match the input signal range. The overall power consumption of the system goes up together with power supply voltage. This is especially troublesome for battery operated systems, such as Mp3 players, for which power efficiency has the ultimate importance due to the fact that it is the main marketing feature of these devices. Of course, increasing power supply level of the ADC does not necessarily means that every blocks within the system will have higher supply level. It is possible to have multiple power domain within the chip. But even so, this choice yields higher power consumption, at least by the ADC and extra device(s) and complexity (and therefore cost) for the overall system.

Attenuating input signal is the other classical option to fix the problem. The system designers prefer this alternative in general because: 1. power supply voltage is a global parameter that will affect every sub-block design of the system. Therefore it is desirable to determine it with respect to some global design constraint, such as power consumption, system speed, technology node, etc... and 2. signal conditioning is relatively easy and local solution to the problem.

Unfortunately, attenuating input signal has its own drawbacks. First, as pointed out earlier, the power management systems are very noisy systems because of their natural constituents, i.e. high power switching regulators. For a given input resolution specification, attenuating input signal corresponds to decreasing (or attenuating) the least significant bit of the ADC with the same factor. Obviously, this is highly undesirable because the design bottleneck right now is shifted to being able to obtain targeted resolution within a very noisy environment. Second, there is no ideal attenuator. As a consequence, the quality (or the accuracy) of the input signal degrades significantly at the output of the attenuator. As it will be pointed out in chapter 2, this is the major cause of the resolution loss in the state-of-the-art power management ADCs. Finally, third, extra attenuation stage, generally speaking, loads the input and burns extra power.

An alternative system level design problem may be the following: assume that the power supply voltage of the system is given. Since the upper limit of the input signal range is

fixed by the supply voltage, the only way to increase the resolution of the ADC is to decrease the LSB level. Hence, in such a design paradigm, the resolution improvements can be done only towards LSB by decreasing it more and more. Decreasing the LSB to improve the resolution, on the other hand, becomes very difficult due to the fact that the relationships are exponential for every single bit resolution improvement in terms of area, power, etc... Therefore, resolving smaller LSB levels is a very demanding task.

In light of the analysis done so far, we can conclude that during the system level design and optimization of the ADC, the designer has to solve the trade-offs among the power consumption, input signal range and resolution. In other word, classically, it is not possible to optimize the power consumption (or supply voltage level, equivalently) independent of input signal range and targeted ADC resolution.

The high-voltage bootstrapped sampling switch solves this trade-off. As it will be clear while analyzing the switch later on, HVB switch is capable of sampling input signals, as they are[4], regardless of the positive supply voltage level. Minimum acceptable supply voltage level is twice the NMOS threshold voltage to guarantee minimum gate-overdrive of the switch transistor and the input signal can change between the ground potential to the drain-bulk breakdown voltage of the technology. As I will point out next, the implications of this freedom are revolutionary.

If the input signal range is given as in the case of power management ADC, it is possible to reduce the overall power dissipation of the ADC and the system n times by simply choosing the supply voltage level n times smaller without attenuating (or degrading) input signal. This dissertation is the proof of this concept for n equal to 2.

If the supply voltage is given, as in the case of high performance ADC system such as pipelined ADCs[5], the input signal of the system can be chosen higher than supply voltage which will result higher LSB level for a given resolution. The implications of being able to multiply the input signal range regardless of the supply voltage level is enormous for pipelined ADCs in terms of power, area and resolution.

The title of this sub-section was the new horizon: The new horizon in system level ADC design is _to seek the extra resolution of the ADC towards most significant bit_. This dissertation is the proof that this goal is achievable.

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[4]like a transmission gate

[5]The supply voltage level of the high performance ADCs are generally chosen as the maximum voltage level rated for the used technology

1.4 Results and Achievements

11 bits analog to digital converter for power management ICs along with its reference buffer is designed using Texas Instruments LBC7 0.35μm technology. Along with the regular 3.3V devices, the process design library contains also 5V and 7V CMOS devices as well as, high-voltage drain extended MOS transistors (7V, 12V, 20V, 24V, 28V, 30V and 33V drain extended MOS transistors.). Consistent with the application, designed analog-to-digital converter does not contain any sample and hold amplifier, hence it is intended to monitor DC voltage quantities.

The converter draws less than 140μA average current during conversion from 2.75V single power supply, including reference buffer. The ADC can operate at supply voltage levels down to 1.8V. The signal range of each one of the 8 input channels of the converter is twice the supply voltage, i.e. 5.5V. Novel high-voltage bootstrapped sampling switch allows to extend the input range of the converter higher than the supply voltage. Although the switch and the converter system is designed for 2.75V supply voltage and 5.5V single-ended input signal range, measurement results show that the switch can successfully sample an input signal changing between 0 to 6 volts with a supply voltage level as low as 1.2V. Therefore, power dissipation can be reduced by 5 times with respect to the classical approach.

Proposed high-voltage passive subtractor circuit also operates as expected. Furthermore, passive subtractor circuit inherently implements low-pass filtering which is very suitable when a DC voltage quantity should be measured in a noisy environment, such as power management systems where high-power switching voltage regulators are present. The output code of the converter can change between 0 to 2046 (2047 codes), resulting 2.688 mV least significant bit.

The conversion time of the converter is less than 10μs for input signal above the supply and less than 5μs for the input signal in between the rails with a 2MHz system clock frequency. Expected duty cycle of the converter is 0.1%. Maximum measured differential and integral nonlinearity errors (DNL and INL) of the converter within the full input signal range are less than 0.45 LSB and 0.38 LSB, respectively. Designed ADC occupies a silicon area of only 560 by 560 μm^2. All relevant specification of the designed ADC are summarized in Table 1.1

Symbolic Small Signal Analysis Tool (SSA Tool), a general purpose circuit analysis tool that calculates small signal response of any given circuit or system symbolically, is implemented using Matlab Symbolic toolbox. Basically, SSA tool extracts symbolic node equations from the input netlist and solves the symbolic linear node equation system.

Cadence DFII Virtuoso schematic capture environment is the main schematic entry

Table 1.1. Specifications of the 11-bit Sub-Ranging ADC

Parameter	Value	Unit
Number of Channel	8	
Input Signal Range	0 - 5.5	V
Supply Voltage	2.75	V
Supply Current	120	μA
Conversion Time	< 10	μs
Clock Frequency	2	MHz
Resolution	11	bits
LSB	2.688	mV
DNL	0.45	LSB
INL	0.38	LSB
Silicon Area	560×560	μm^2

interface of the tool. Required Cadence Skill codes for data export is developed along with the Cadence design library named *SSALIB*. Developed design library contains 103 custom models. Along with basic device models (such as resistor, capacitor, inductor, transformer, controlled voltage and current sources, etc...), the design library contains also block level macro models (such as crystal oscillator, on chip inductance model, discrete time integrator model, ideal OPAMP model, quantizer model, discrete time filter model, etc...) to ease system level modeling, design and optimization. Using SSA tool, it is possible to model and analyze continuous as well as discrete time systems. The tool allows the user to develop full custom device or macro models either using hierarchical schematic design feature of the Cadence Virtuoso capture environment or by developing full custom SSA tool device model card. The development of a custom device model card is explained in detail with an example model (MOS transistor model).

The tool is capable of calculating linear as well as nonlinear transfer functions of arbitrary circuits or systems. The background and the methodology of nonlinear analysis, as well as numerical evaluation of the transfer functions, are extensively explained within chapter 4. Current version of the tool is capable of calculating harmonic and intermodulation[6] distortion transfer functions of up to third order. Although the technique used for obtaining the nonlinearity transfer function can calculate up to an arbitrary harmonic order, this limitation is simply because of the fact that the second and the third order nonlinearity

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[6]Hence, it is possible to calculate mixer gain or equivalently stimulate the circuit/system with multiple source at different frequencies.

components are generally the dominant terms at the output of single-ended and differential circuits, respectively.

SSA tool provides several extension modules, i.e. $\Sigma\Delta$ modulator analysis module and Transfer function analysis module. The effectiveness of these modules, especially $\Sigma\Delta$ modulator analysis module, in design and optimization of circuit and systems is shown again in chapter 4. Nonlinear analysis feature of the tool combined with $\Sigma\Delta$ modulator analysis module allowed us to analyze and optimize symbolically arbitrary modulator topology's SNR and SFDR with respect to several circuit nonlinearities, such as feedback DAC nonlinearity, sampling switch nonlinearity, amplifier's slew-rate and DC gain nonlinearities.

1.5 Organization of the Dissertation

Chapter 2, after briefly discussing the power management ICs and their specific needs, summarizes the performance levels of the state-of-the-art power management IC's analog to digital converters and discusses/shows their main flaws/limitations in terms of precision. The state-of-the-art symbolic analyzers will also be discussed in this chapter.

Chapter 3 will reintroduce basic requirements of power management ADCs together with the main features of the designed 11-bit Sub-Ranging ADC. The block diagram of the whole ADC architecture and the justification of the choice of architecture will be given next. Basic building blocks of the ADC, such as high-voltage bootstrapped sampling switch, high-voltage passive subtractor and 10-bit SAR ADC will be analyzed in detail. Finally, the simulation results of the ADC will be presented in this chapter.

Chapter 4 can be considered as the manual of the SSA tool. The analysis flow will be presented together with the different processes of the tool. The nonlinear analysis technique used by the tool will be briefly described together with its limitations without going into to much detail. Different modules of the tool will be presented. Development of custom device model card will be explained.

Chapter 5 contains the details of the ADC measurement. The measurement setup and the techniques will be discussed here. The measurement results of the basic sub-blocks will be given. The integral nonlinearity and differential nonlinearity measurement of the whole ADC within the full input signal range will be shown in this chapter.

Chapter 6 will show the efficiency of the SSA tool using examples. Several complex $\Sigma\Delta$ modulator topologies will be analyzed. The nonlinearity analysis of a modified switched emitter follower circuit will also be presented.

Finally, in chapter 7, conclusions will be drawn.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The first part of this dissertation consists of the design of an 11-bits Sub-Ranging Analog to Digital converter designed for power management ICs.

Due to the inherent need of every electronic circuits/systems of one form of power source/management, the power management ICs attract more and more interest. The trend toward a mobile world also reinforces this interest. With the push of higher and higher expectations from the power management systems, their complexity together with the number of different specialized electronic blocks increased. Integrated data converters are introduced into these systems first for accurate monitoring and then for data processing.

Generally speaking, although the resolution and speed requirements can be considered relatively easy to satisfy, the analog to digital converters used within the power management applications have their own design challenges that I will review later in this chapter.

Therefore, in the first half of this chapter, I will review the relevance and the requirements of the analog to digital converters for power management applications. I will briefly describe available solutions to existing application related problems and their shortcomings.

The second part of the dissertation consists of the introduction of a symbolic circuit analyzer tool. The main emphasis on the developed tool, i.e. SSA tool, is its integration with existing symbolic solver softwares and IC design tools and not the development of a generic symbolic equation solving methodology.

During the second half of this chapter, I'll provide a brief summary of the literature and state of the art in this research area, together with other available commercial or academic symbolic circuit analysis tools for interested readers.

2.2 Power Management ICs (PIC) and Analog to Digital Converters

2.2.1 Market Demand and Requirements

Power management systems become more and more important in modern electronics. Total market size for power management ICs (PIC) was around $5.1 billion dollars by the end of year 2000 and estimated to be over $7 billion dollars by year 2006 with an average compound

annual growth rate of 35% [1, 2, 3].

With every new generation of technology node, electronic industry expects higher accuracy and functionality from PICs; higher global efficiency, wider load range, power input from multiple power sources, regulated power output to multiple blocks and sub systems, very low sleep current, monitoring (i.e. keeping track of different voltage outputs and load current), surveillance (i.e. shutting down blocks having problems such as short to ground etc...), signal processing(very limited), just to name a few of them.

Mixed signal applications requiring on-board precision analog functions and efficient power capabilities are the driving force behind the large PIC market [4]. With ever increasing emphasis on energy conservation requirements, the need for better and more capable (or smart) power management circuits/systems (in terms of data pocessing, implementation of power aware communication protocols, battery life time, communication over the supply line, etc...) will enlarge the power management IC market even further.

With the help of the consumer drive toward the wireless world, among the diverse PIC products, battery charging and battery management segment of the market is the fastest growing in both dollar amount and unit volume because of the expansion of portable and/or mobile applications; especially notebook computer applications are the horsepower behind this dynamic [1].

Again, the market dynamics force the mobile systems to increase functionality for the end user by increasing battery life time, power efficiency, improving interface quality and compatibility and decreasing weight and form factor of the system [5].

2.2.2 PIC system Sub-blocks

Consistent with the market trends and requirements, the system complexity of the commercial PIC increased rapidly. Since the driving power is the mobile sector, a quick survey of the available battery power management IC systems reveal the following general sub-blocks and circuits [1, 4, 5, 6, 7]:

- Digital Core / Micro Processor / DSP / Digital Interface to communicate, supervise and implement power aware system.

- Input Power source management (multiple battery, different types of battery, USB, wall)

- Output Power Management, i.e. Voltage Regulators and Switches (High Efficiency DC-DC converters, Linear Voltage Regulators, High Power Switches)

- Input and Output Power monitoring (Battery fuel gauge, coulomb counter, load current monitor, supply level monitor, Data converters)

- Time and voltage reference circuits (RTC and BandGap Reference)

A typical PIC system subblocks are also shown in Fig. 1.2. Among these blocks, precision subblocks, such as time/voltage reference circuits and analog to digital converter, occupy negligible amount of silicon area compared to voltage regulators, as it is clear from Fig. 1.2(b).

The diversity of the different sub-blocks within the PIC system, in terms of functionality, operating principle, power level, precision, etc.. makes the design of this mixed-mode system very challenging. Solving the problems related to temperature gradient within the die, substrate and supply noise signals due to the high power sections of the system are the main issues during the design. Noise isolation efficiency and layout are crucial to be able properly operate microwatt power level circuits such as data converters together with several watt power level switching regulators.

2.2.3   Analog To Digital Converter Requirements

I will concentrate on the requirements and problems related to the implementation of the ADC for the rest of the section since the subject is the design of an analog to digital converter for power management ICs.

Modern highly integrated power management systems contain analog to digital converters to monitor on-chip and off-chip voltage quantities, temperature sensing, battery gauge and signal processing [5, 6, 7, 8, 9, 10].

As pointed out previously in section 1.2, the resolution and speed requirements of the power management ADCs are moderate to low compared to the ADCs aimed for signal processing. Typical conversion rates for such data converters may change from 50 microseconds to 100s of milliseconds. The resolution requirement can vary from 8 to 11 bits. Since these converters are used mostly for monitoring and supervising purposes, the static linearity and absolute accuracy (DNL and INL, gain and offset) of the converter are the most important parameters rather than dynamic linearity (SNR or SFDR). The current trend pushes the data converter performance for higher resolution because of the higher control and efficiency expectations.

The ADCs in such systems are required to sample input voltages that are greater than their power supply range. The need arises from several different requirements [8, 11, 12, 13, 14, 15, 16]:

- There are multiple power inputs each of which can go down all the way to ground potential. There is not a definite absolute high voltage in the system.

- The supply voltage of the converter itself is ultimately derived from one of these power input sources.

- It is desirable to keep the supply voltage of the converter as low as possible to improve the global efficiency of the system.

The third item is the most important one for the system designed for high efficiency. For such systems, global power budget dictates the choice of supply voltage level, regardless of the input signal levels[11, 12, 13, 14, 15, 16].

Sampling a signal higher than the supply voltage is harder than it is said. The main problem is that there is not an absolute maximum voltage level present within the system. Hence, it is not possible to use PMOS transistor on the signal path without forward biasing its parasitic body diode. We will review available solutions to this problem in the next section, but it is fair to conclude that this is the most challenging task, especially for high-resolution designs.

In addition to sampling input signal levels higher than supply voltage and low power consumption, the analog to digital converters designed for PICs have to be resilient to noise because they not only have to operate within a very noisy environment due to high-power switching regulators [6, 7, 17, 18, 19], but also they have to resolve very small voltage quantities with high resolution, such as in the case of temperature measurements [20, 21, 22] from a single ended input source.

2.2.4   Monitoring Input Signals Exceeding the Supply Voltage: Solutions, Problems, Trade-offs

Within the section 1.3.1, I analyzed in detail the trade-off among the power consumption - input signal range - resolution and the system level implications of determining the input signal range and selecting power supply voltage level. Among the different options, increasing the supply voltage level is the least likely solution to extend input signal range of PIC ADC because of the system level issues and power consumption implications.

Classically, the problem of monitoring input signals beyond the supply range is solved using signal conditioning, meaning before digitizing, the input signal is rescaled and shifted so that it fits within the converter signal range which is, again, bounded by the system supply voltage. Signal conditioning is necessary mainly because it is not possible to sample those inputs with conventional circuit techniques without forward biasing any parasitic body
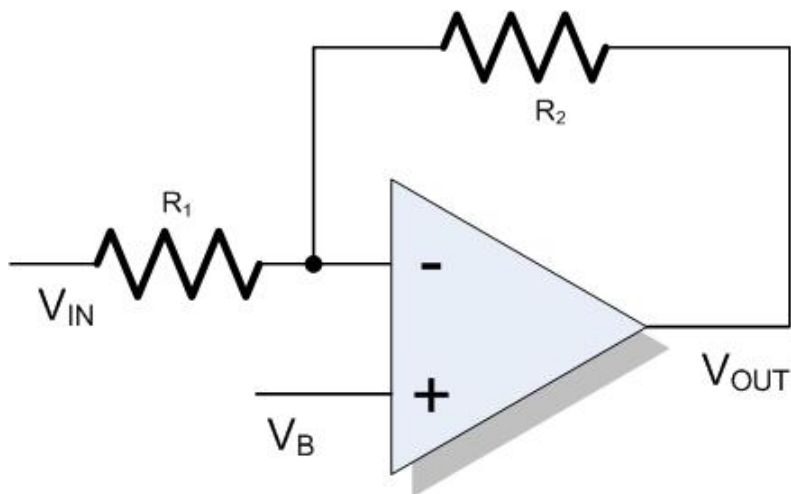
Figure 2.1. Input Rescaling Using Feedback Amplifier for Low Output Impedance

diodes [23, 24, 25, 26, 27, 28]. In this subsection, I will review different options available with classical approach and their shortcomings.

Aforementioned signal conditioning can be achieved by using active feedback amplifiers or simply by resistive dividers [8, 11, 12, 13, 14, 15, 16, 18, 19, 29, 30, 31]. Figs. 2.1 and 2.2 show these two widely used circuits to recondition the input signal. In principle both circuit convert the input voltage to a current to solve high voltage related issues and then convert back to voltage. The first solution, feedback amplifier, provides low output impedance to drive easily cascaded analog to digital converter. Its transfer function can be expressed as

$$V_{OUT} = \frac{R_1 + R_2}{R_1}V_B - \frac{R_2}{R_1}V_{IN} \tag{2.1}$$

As it is clear from the equation, by properly choosing bias voltage V_B and the resistors R_1 and R_2, it is possible to recondition the input signal so that the input signal fits within the supply range.

The transfer function of the second circuit, simple resistive divider, can be expressed as shown below. The resistive divider acts like a simple gain stage.

$$V_{OUT} = \frac{R_2}{R_1 + R_2}V_{IN} \tag{2.2}$$

The input signal is attenuated[1] in both of the cases. The accuracy of the input signal conditioning circuitry directly affects the global accuracy of the converter. This necessary preprocessing stage is the main reason of the accuracy lost.

One can argue that it is possible to trim the error introduced by the input stage after production. Since, the analog to digital converter used within PICs have to monitor typically

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[1]Although this is not clear from eq. 2.1
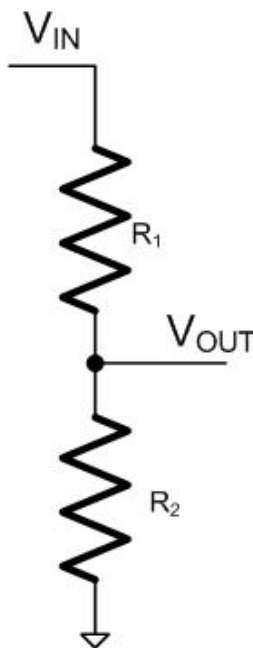
Figure 2.2. Input Rescaling Using Resistive Divider, High Output Impedance

multiple input sources, it becomes very costly to trim the error for all input channels. The unadjusted accuracy parameter list shown in Table 2.1 clearly shows that. The problems associated with attenuating the input signal are summarized below. Some of the items apply to both circuits shown above and some apply only to one of them.

- Input channel dependent offset voltage . The offset of the amplifier due to the device mismatches directly appears at the output of the input stage.

- Input channel dependent gain error. The variation of the gain coefficients, i.e. $\frac{R_2}{R_1}$ or $\frac{R_2}{R_1 + R_2}$, due to the resistor mismatch, creates gain error. This error is especially dominant because large resistors are generally used in order to limit the power consumption. On the other hand, matching of two resistors degrades more and more with increasing value of the resistors [8, 32, 33].

- Input signal is distorted by the input stage amplifier. Since both attenuation options require current flow or equivalently variable voltage drop across the resistors, the non-linearity of the resistors distorts the signal. Furthermore, since the voltage coefficients of the high-sheet resistance layers are generally higher than the low-sheet resistance layers [33], there is a trade-off between distortion and input load (or power consumption of the signal conditioning block).

- Signal conditioning circuitry noise (device noises such as shot, thermal, flicker or deter-

ministic noises such as power supply noise, substrate noise etc...) appears at the output. Plain resistive divider circuit is very susceptible to noise simply because its output is high impedance and requires special layout technique and circuit technique to protect the input signal from degrading.

- As pointed out earlier, for the same resolution of the input signal, the least significant bit (LSB) of the converter should be scaled (attenuated) with the same gain (attenuation factor); but, reducing LSB level makes the design of the converter even more difficult in terms of area, power and noise, for fixed resolution of the input signal.

- The input source is loaded. Extra power is consumed by the amplifiers or passive resistive divider. Typical input load current is on the order of 120 to 500 μA just for signal conditioning [8, 18, 19].

In short, the fidelity of converted signal to the actual signal is degraded because of the signal conditioning. Aforementioned problems severely limit achievable resolution of ADCs. Available PICs in the market typically has 8 to 32 LSB uncorrected error [8, 11, 19]. The error increases also if the targeted load current is very low.

2.2.5   Noise and Isolation strategy and Circuit/System Level Design Issues

As mentioned previously, noise isolation strategy at system/circuit/layout levels are key to achieve targeted resolution.

System/circuit level options to improve the noise immunity of the converter are: 1) Selecting larger LSB level and signal range [29, 34], 2) Filtering 3) Fully differential circuit design. Especially, fully differential circuit design is a must to suppress the noise injected by the switching regulators to the substrate and to the supply lines. These noise signals are common mode signals; they can be suppressed further by the common mode rejection of the differential circuits.

Another widely used system level approach to reduce the noise sensitivity of the converter is the multiple measurement averaging technique [6, 7, 9, 10]. Multiple measurement averaging technique is essentially based on the well known principle that the noise power in a signal obtained using the average of N parallel identical measurement (ensemble) is inversely proportional with N [35]. Of course, practical PIC ADCs use time averaging instead of ensemble averaging assuming that the system is ergodic [36, 37]. On the other hand, time averaging increases greatly the conversion time of the ADC [14, 15, 16, 20].

Proper layout is an integral part of the converter design. Isolation tank p-type substrate formed with the help of Sinker Nwell layer together with NBL layer, as shown in
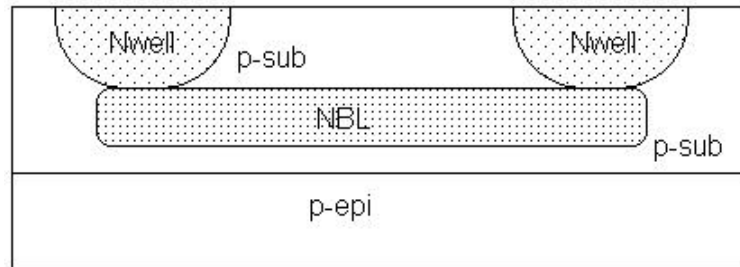
Figure 2.3. NBL - NWell Tank Isolation

Fig. 2.3. can be used to isolate the N channel devices. Of course minority carrier collecting guard rings should be placed, first around the noise injector devices and then around the sensitive analog to digital converter. The layout of the fully differential circuits has to be drawn completely symmetrical with respect to the symmetry axis to be able get full benefit of the differential circuit in terms of common mode signal suppression. Finally, sensitive analog signal nodes have to be properly shielded. These design guidelines are all engineering best practices and related detail can be found extensively in the literature [38].

2.2.6 Comparison of the Designed ADC with the Performance of the Available PIC ADCs.

Critical performance parameters of the ADC of available PICs together with the performance of the designed ADC are summarized in Table 2.1. The data presented here is collected from the component data sheets. Comparison in terms of silicon area and technology cannot be added to the table because of the lack of data. Most of the converters use multiple conversion averaging technique to reduce the noise power in the conversion result. This is the main reason for very large conversion times.

The conversion time data marked with an asterix in the Table 2.1 refer to the total conversion time at the end of 16 measurements. These converters use data averaging technique to reduce noise power within the conversion result. The total unadjusted resolution of the data converter gives the measure of the absolute accuracy of the converter degraded from the ideal resolution for any reason. Some of the supply current given in the Table 2.1 are total IC supply current rather than ADC supply current. A separate ADC current is not provided within those devices' data sheets.

The comparison table proves that designed ADC consumes at least 37% less power than the most power efficient converter in the table. Notice that although the converter is designed for 2.75V, it is still operational at 1.8V supply voltage level. The absolute accuracy of the designed converter is of course much higher.

Table 2.1. Performance parameter list of available PICs in the market together with presented ADC.

Ref.	Power Supply	# of Chan.	Supply Current	Res. and Unadjusted Res.	LSB [mV]	Conversion Time	Input Stage
[8]	2.5V	19	2·5mA	8 - 4 bits	2	273 ms*	Resistive divider
[9]	3.3V	2	225μA	8 - 6 bits	2	115 ms*	-
[10]	3.3V	2	1·4mA	10 - 7 bits	0.5	9.6 ms*	-
[11]	3.3V	9	400μA	10 - 4 bits	2	9.6 ms*	Resistive divider
[12]	5V	6	160μA	8 - 5 bits	2	9.6 ms*	Resistive divider
[13]	5V	5	3mA	10 - 6 bits	0.5	11.38 ms*	Resistive divider
[14]	3.3V	8	400μA	8 - 5 bits	2	11.6 ms*	Resistive divider
[15]	3.3V	8	400μA	8 - 5 bits	0.5	11.38 ms*	Resistive divider
[16]	3.3V	5	400μA	8 - 6 bits	0.5	11.6 ms*	Resistive divider
[18]	-	-	-	10 - ? bits	-	-	Resistive divider
[20]	3.3V	1	2mA	8 - 5 bits	2	273 ms*	-
[21]	3.3V	2	400μA	10 - 6 bits	0.5	9.6 ms*	-
[22]	3.3V	2	160μA	8 - 6 bits	2	9.6 ms*	-
[29]	10V	3	60μA	10 - 7 bits	10	3.4 ms	Resistive divider
[30]	5V	4	1mA	N/A - 5 bits	-	-	Programmable Attenuation
[31]	5V	2	1mA	N/A - 5 bits	-	-	Programmable Attenuation
[34]	10V	1	60μA	10 - 7 bits	10	3.4 ms	Resistive divider
This Work	2.75	8	120μA	11 - 11 bits	2.7	$< 10\mu s$	Direct Sampling

2.3 Symbolic Circuit Solvers

2.3.1 History

Symbolic analysis of electronic circuits draws researchers' attention since late 1960's [39]. Here, I will provide a brief survey of this quest.

A brief search of the available literature reveals a wealth of research reports regarding to the best suitable methodology to solve equation systems describing the electronic networks [40, 41], different simplification algorithms [42, 43, 44, 45], error control mechanism [46] and implemented software tools for symbolic circuit analyses such as ISAAC[47], ASAP[48], SSCNAP[49], CASCA, SAPEC, SSPICE, SCYMBAL, GASCAP, NAPPE and more [50]. Some of them are developed to analyze continuous time analog circuits, some others developed for digital filter design, some of them specialized on switched capacitor circuit analysis [49, 51] and finally some attempts to provide a generic solver that is capable of handling all these different circuits[47, 48].

It is easy to understand the focus of the research effort since the major drawback of the symbolic circuit analysis is the exponential growth of the symbolic terms in the transfer function with the number of nodes and circuit components included to the design which quickly makes it impossible to analyze even moderately large circuits. For instance, the denominator of the network function of a BICMOS OTA presented in [46] contains more than 10^{11} symbolic terms in expanded format. In short, the dream of every researcher who spent time and energy in this area is to find the ultimate algorithm that will extract a simple and accurate expression representing the true essence of the analyzed network. An expression like $E = mc^2$, very simple yet very powerful and explanatory.

Together with aforementioned academic research, there are lots of available dedicated stand alone symbolic circuit analysis softwares [52, 53, 54, 55] or toolboxes developed within software packages such as Maple, Mathematica and Matlab [56, 57, 58, 59].

The early versions used brute force approach. This approach of course restricted the capability of the tools to only very small circuit complexities due to the exponential relation of the symbolic terms to the circuit complexity and limited computational resources in terms of memory and processing time. Since then the solving and simplification algorithms have evolved drastically.

Again the early focus of the symbolic analysis was of course linear analysis. The focus was then extended to the analysis of the weakly nonlinear circuits [60, 61, 62] and finally to the analysis of analog circuits with hard nonlinearities [63, 64]. There are also linear analysis techniques to extract symbolic pole and zero expressions of the network function [65].

Let us now proceed with the survey.

2.3.2 Definiton

Definition of the symbolic analysis is[50]:

> Symbolic analysis at the circuit level is a formal technique to calculate the behavior or a characteristic of a circuit with the independent variable (time or frequency), the dependent variables (voltages and currents), and (some or all of) the circuit elements represented by symbols.

The symbolic analysis research is mainly concentrated on lumped, linear time-invariant circuits. The result of the analysis is a transfer function or a network function in frequency that is a rational function of two polynomial of the complex frequency variable (s or z) and the coefficients of the polynomials are symbolic expressions of the circuit components.

2.3.3 Applications of Symbolic Analysis: What is it good for ?

The symbolic analysis is considered complementary to the numerical analysis. It is possible to itemize the major applications of the symbolic analysis as follows [50, 66]

- First and foremost application of the symbolic analysis is that it provides insight into the circuit behavior. The numerical simulator can provide very accurate result of the circuit only for a particular set of parameter values. Therefore, using numerical simulation, it is possible to verify very easily the function of the circuit. But the results, i.e. sets of data points, do not show which component or parameter is responsible for that result. Symbolic analysis may reveal this secret [67].

- It is possible to use the analytic expression for modeling in order to decrease simulation time [68]. Of course, evaluating an expression with different sets of parameter values is much faster than obtaining the circuit response numerically for each case separately. It is also possible to use this model expression for design automation.

- Symbolic analysis is used for circuit exploration [67]. The effects of a small modification of the circuit can easily be tracked from the expression. Therefore, the symbolic analysis can be used for concept proof. In other word, it can prove[2] that the very good numbers obtained from the numerical simulator is (or is not) accurate (or simulator error).

- If a circuit response has to be evaluated multiple times for different sets of parameter values, such as in the case of Monte Carlo analysis, fault diagnosis, yield estimation, discrete time system analysis, use of symbolic analysis can speed up this process drastically.

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[2]For a set of problem and circuit
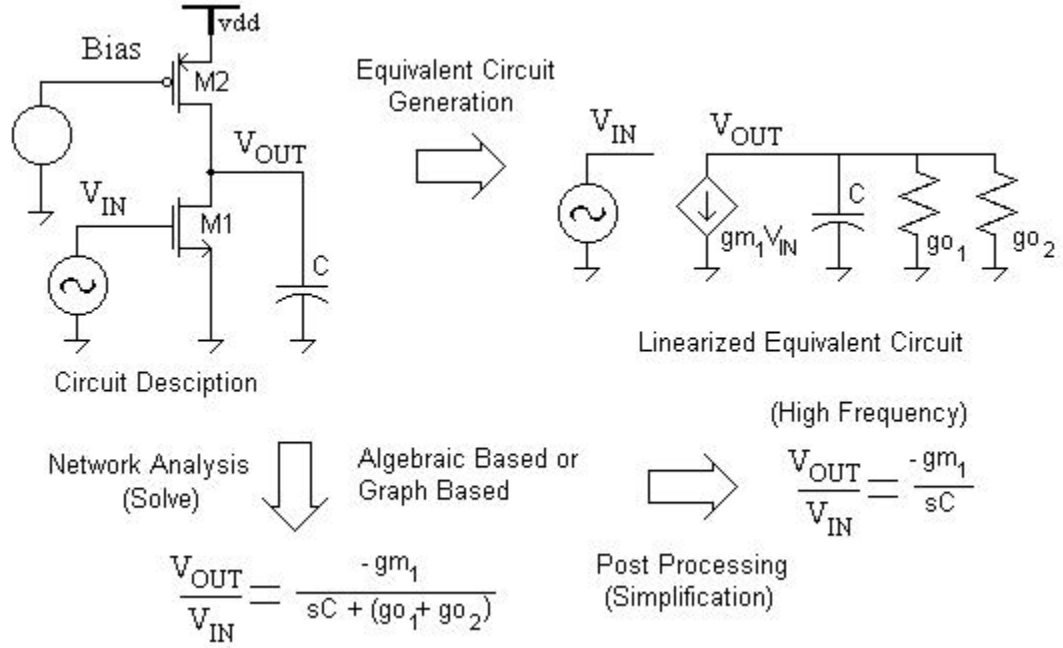
Figure 2.4. Basic Process Flow of Symbolic Circuit Analyzer From Circuit Description to Symbolic Transfer Function

- With recent development, it is possible to use symbolic analyzer for nonlinear analysis of the circuits (Weak nonlinearity[60] or Hard nonlinearity[63, 64]). The analysis of weakly nonlinear behavior of the analog circuits is based on the assumption that the magnitude of the increasing order of harmonic is decreasing so that N^{th} order response of a nonlinear circuit is a function of only circuit's N^{th} and lower order harmonic behaviors. This condition allows sequential computation of the nonlinear transfer functions of analog nonlinear circuits. The method used to compute hard nonlinearity is based on piecewise linear analysis.

2.3.4   Symbolic Analysis Process Flow and Performance

Different steps of the basic process flow of a generic symbolic circuit analyzer are shown in Fig. 2.4. The symbolic analysis process flow can be summarized with the following steps:

1. The input is a netlist describing the connection information and the component type and its parameter values[3].

2. The circuit is then replaced by its linearized equivalent according to predetermined equivalent circuits for nonlinear components.

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[3]The parameter can be symbolic or numerical. Notice that numerical analysis is a subset of the symbolic analysis.

3. The linearized equivalent circuit is solved. It is possible to separate the solving algorithms to two major categories (both of them have several sub categories.):

   (a) Algebraic methods (Matrix or determinant based)

   This solving method uses a set of equations describing the behavior of the linear equivalent circuit. The coefficients of the equations are of course symbolic. It is also know that although, LU decomposition and Gaussian elimination performs best on numerical evaluation of the linear circuits, symbolic computation of the circuits is better performed using Cramer's rule. Numerical interpolation method, parameter extraction method and determinant expansion method are the names of few solving algorithms based on algebraic methods.

   (b) Topological methods

   This solving method first generate equivalent signal flow graph of the linear equivalent circuit. The branch weights of the graph are symbolic expression. The two-graph method, The directed-tree enumeration method, the signal flow graph method, the coated flow graph method are the names of few graph based circuit solving techniques. The signal flow graph contains node voltages and branch currents. The network function is then extracted from this graph.

It is also possible to regroup solving methods by the way they incorporate the simplification algorithm. As it will be clearer next, a class of circuit solving (or symbolic term generation) algorithms implements simplification by:

   (a) Starting to generate symbolic terms in decreasing magnitude meaning the symbolic terms having larger magnitude are generated first so that an error control mechanism can be introduced to the generation.

   (b) Not generating any term that will be ignored.

   (c) Not generating any term that will be canceled.

These algorithms belong to so called simplification during generation class. Equal coefficient approximation, error bound propagation, magnitude threshold method and sensitivity driven term generation with global error control are the names of few simplification during generation based solving algorithms. Detailed analysis of these methods can be found in [46].

Another interesting solving algorithm is based on hierarchical problem solving[40]. The Diakoptics solving technique is based on tearing the analyzed circuit into smaller and manageable part. After solving the network function of these subblocks, the results are

further post processed (modified) to remove the unbalanced conditions at the interconnection nodes/branches. These type of algorithms are classified as hierarchical and they are very effective in solving large circuits.

The efficiency of a solving method can be quantified with respect to two criteria. The first one is the running time limit of the algorithm and the second one is the number of needlessly generated terms, i.e. canceling and/or ignored terms. Detailed analysis of different solving algorithms and their comparison in term of performance can be found in the literature [69].

4. Finally obtained network function is simplified or post processed. There are many different simplification techniques, but generally speaking, they can be classified in four different classes:

   (a) Simplification After Generation
   (b) Simplification Before Generation
   (c) Simplification During Generation
   (d) Goal oriented simplification

Before analyzing further aforementioned techniques, it is worth noting that the simplification process, in general, is strongly dependent on the operating conditions of the circuit in terms of operating frequency, bias, etc... Therefore, the simplification processes, together with the solving algorithm incorporating simplification during generation technique, are closely coupled with the numerical evaluation of the circuit [43].

Historically, the simplification after generation algorithms appeared at first. The symbolic analyzers incorporating this technique calculate first the exact expression and then remove the insignificant terms from the obtained expression according to some predetermined error threshold. As pointed out earlier, since the number of terms within the expression grow exponentially with the number of nodes and the number of elements within the analyzed circuit, in other word with its complexity, required memory and computer performance become quickly unachievable even for moderately large circuits [46].

Due to the shortcoming of the simplification after generation technique in terms of handling moderate size problems, the simplification during generation is developed at about the same time frame with the development of the simplification before generation technique. Those are mostly topology based algorithms. The simplification during generation methods generate the simplified expression in step by step manner starting from

the dominant term. In general, simplification during and before generation techniques have to be combined in order to obtain reasonably large results for large analog circuits.

Finally, the goal oriented simplification techniques use before hand knowledge to simplify obtained transfer function very much like an expert system [42].

CHAPTER 3

11-BITS ANALOG TO DIGITAL CONVERTER FOR POWER MANAGEMENT ICs

3.1 Introduction

In this chapter, a novel ADC architecture that is capable of sampling and digitizing an input signal exceeding power supply voltage without any input signal conditioning and forward biasing parasitic body diodes will be presented. Two novel high-voltage signal processing circuits, i.e. high-voltage bootstrapped sampling switch and high-voltage rail-to-rail passive subtractor, are designed for this purpose. I will analyze these sub-blocks in detail later on within the chapter.

Designed ADC has 8 input channels each of which has 0 - 5.5 V signal range. The resolution of the converter is 11 bits. Of course, integral and dynamic nonlinearities of the converter are less than an LSB throughout the whole input signal range. One LSB is around 2.688 mV. The conversion time is specified as less than 10 μs with 2 MHz system clock frequency.

Although it can be chosen much smaller, the supply voltage level of the power domain of the ADC is 2.75 V. Therefore, the input signal can go twice as much as the supply voltage. The supply current is kept minimal[1] since it will ultimately effect the efficiency of the whole system.

The ADC is implemented using Texas Instrument Inc.'s LBC7 0.35 μm technology. LBC7 has also high-voltage LDMOS and drain-extended MOS devices for high-voltage designs.

As it is clear from the specification, shown in Table 3.1, the challenges facing the power management ADCs are very different than regular signal processing ADCs. Targeted conversion time and resolution are well within the capabilities of todays technologies. The challenges in this design are, as pointed out earlier: 1. converting within a wide input signal range exceeding the supply, 2. obtaining the targeted resolution within a very noise environment.

The floorplan of a typical PIC system is given here again in Fig. 3.1 to understand the severity of the noise problem. The converter occupies a negligible amount of real-estate.

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[1] Power consumption of the ADC was not a major issue for this design because of the fact that expected duty cycle of the converter is around 0.1 %

Table 3.1. 11-bits ADC Design Specifications

Parameter	Value	Unit
Number of Channel	8	
Input Signal Range	0 - 5.5	V
Input Signal Bandwidth	DC	Hz
Reference Voltage	2.75	V
Supply Voltage	2.75	V
Conversion Time	10	μs
Clock Frequency	2	MHz
Resolution	11	bits
LSB	2.688	mV
Technology	LBC7 $0.35\mu m$	
Target Application	Power Management	

The majority of the silicon area is occupied by the switching regulators, linear regulators, high-power switches and the power transistors. Of course, while operating each one these blocks will inject noise to the substrate and to the power rails.

3.2 Architecture selection for 11 bits Analog to Digital Converter

Among different possible analog to digital converter architecture, Successive Approximation Register ADC proves to be the most suitable architecture to implement targeted ADC. The rationals behind the selection of SAR architecture are given below.

1. SAR converters are very low power.

2. Specified 11 bit resolution can be achieved with SAR converter topology.

3. System clock frequency is high enough to finish conversion using SAR topology for targeted resolution.

4. They are area efficient.

5. This topology is relatively easy to implement.

The fact that the SAR converters are inherently low power is the main reason why this kind of data converter used widely within the systems requiring moderate conversion rate, moderate resolution and high power efficiency, such as power management systems
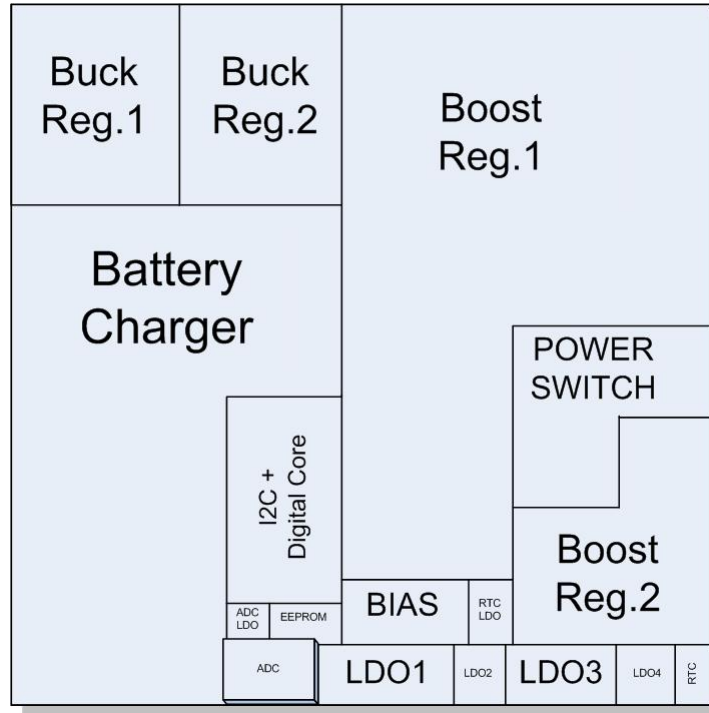
Figure 3.1. A modern Power Management IC's Typical Floorplan

or sensor nodes of distributed sensor networks, etc... SAR topology contains one single comparator that burns static power. The power consumed by the SAR logic is negligible. The remaining of the converter consists of some switches and capacitors. In summary, low power consumption property of the SAR converters is the main reason for the selection of this basic topology.

Desired 11 bit ADC can be implemented using two alternative ways. The first option, although it is simpler to implement and somewhat more obvious, has poorer noise performance compared to the second one. After briefly reviewing the basics of SAR converters, first structure will be analyzed for the sake of completeness and before proceeding to the analysis of the ADC's sub-blocks, the implemented structure, i.e. the second structure, will be presented.

3.2.1 Successive-Approximation Register (SAR) Analog to Digital Converter Basics

SAR ADCs are one of the most popular ADC topology used to implement moderate resolution converter due to their reasonably fast conversion time and simplicity[70]. This type of converters are based on so called *binary search* algorithm where the decisions are made upon

the answers that can be either *yes* or *no*. Consider the game of guessing a random number between 1 to 64. The first question would be whether the number is greater than 32, if the answer is *yes* then the next question is whether it is greater than 48. On the other hand, if the answer is *no* then the next question is whether it is greater than 16. The algorithm proceed this way until the solution is obtained. Because of the nature of the decision making, the binary search algorithm divides the solution space to two subspaces sequentially till the solution with desired accuracy is obtained. In general, the algorithm is capable of finding desired solution after N steps from an organized data set of size 2^N.

SAR converters implements the binary search algorithm to determine the best match digital word to the input signal. The N bit converter determines each bit sequentially starting from the most significant bit to least significant bit by comparing the corresponding digital word with the input signal in N steps. The flow graph showing the successive-approximation logic is shown in Fig. 3.2. Here, the comparison is based on the error signal, i.e. V, that is equal to the difference between the input signal and the output of the digital to analog converter. As a consequence, the error signal is compared each time with the ground potential.

SAR ADCs are widely implemented using switched capacitor technique. A possible implementation of a 6 bits SAR converter[2], excluding the digital SAR logic, is shown in Fig. 3.3.

The circuit works as follows: Initially, the converter logic configures the capacitor matrix switches so that the input signal V_{IN} is sampled on all of the capacitors. After, the initial phase, C_7 is grounded to compensate the offset. The digital logic applies the reference voltage, i.e. V_{REF}, to the capacitor matrix starting from C_1 by properly configuring the switches. If the result of a given comparison is logic one, corresponding digital bit is set to 1, otherwise it is set to zero. The algorithm proceed with the comparison phase of the next bit in the digital word. Once every single bit of the converter is compared and set, the digital word that best matches the input signal is obtained.

3.2.2 Extending the Input Range of a Regular SAR ADC

Let us now, proceed with the implementation details of the wide input signal range ADC. During the development of both architectures, it is assumed that a high-voltage sampling switch[3] exits to sample input signals exceeding supply voltage level. Particularly, for the ADC system specified in the Table 3.1, the input signal range is twice of the reference (and supply) voltage level.

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[2]This circuit is also know as Charge-Redistribution ADC

[3]Of course, such a switch should be build with an NMOS transistor and should not contain any PMOS transistor within the high-voltage signal path.
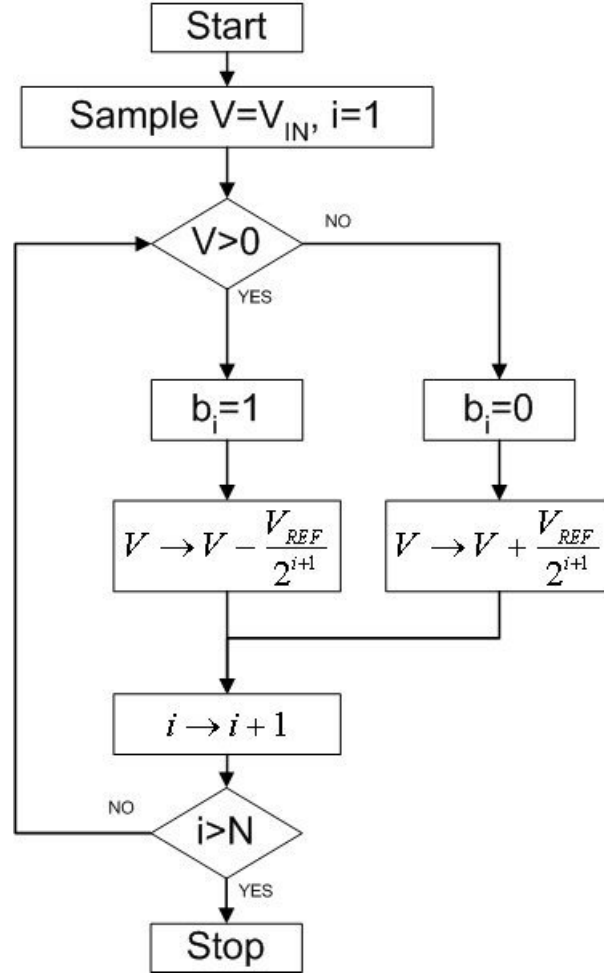
Figure 3.2. Successive-Approximation Algorithm

A strait-forward implementation of the SAR ADC with an input signal range twice the reference voltage V_{REF} is shown in Fig. 3.4 [71]. This is a simple 4-bit charge-redistribution ADC with extended input range. All the switches that connect ground to the bottom plate of the sampling capacitors should be realized using simple NMOS switch; and the switches that connects the reference voltage, except the HVB switches, should be realized using transmission gates. As it is clear from the Fig. 3.4. only two of all switches have to be high-voltage sampling switch. During the evaluation of the bits and of course under ideal conditions, the voltage at the negative terminal of the comparator can be expressed as:

$$V_N = -\frac{8}{16}V_{IN} + \left(\frac{8}{16}b_3 + \frac{4}{16}b_2 + \frac{2}{16}b_1 + \frac{1}{16}b_0\right) \tag{3.1}$$

Notice that the input is connected only to MSB capacitor during the sampling phase as oppose to the classical SAR implementation where the input signal should be sampled on all of the capacitors. As it is clear from 3.1, the input signal is attenuated by half during the
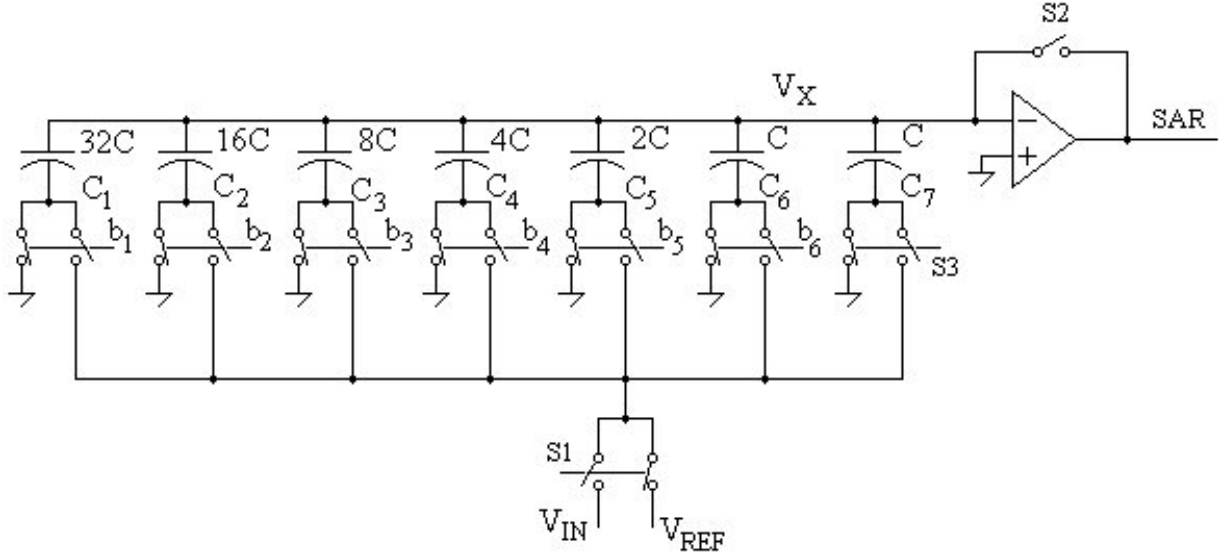
Figure 3.3. Charge-Redistribution SAR Converter core

conversion because it is sampled only on the MSB capacitor. Attenuating input signal, on the other hand, is equivalent to expand the full-scale input signal range of the converter by the same factor. Therefore, the implementation shown in Fig. 3.4 has a full-scale input range twice of the converter's reference voltage. It is also possible to extend it further easily to 4, 8 or 16 folds of the reference voltage. For this purpose the input signal should be sampled only with the sampling capacitor with the value $4C$, $2C$ and C, respectively.

Another benefit of this topology is the improved sampling accuracy. Notice that since the total capacitive load of the converter input is reduced (or more precisely halved for this case), the sampling time constraint of the converter becomes more relaxed. The sampling error percentage due to the RC time constant of the sampling circuit can be expressed as:

$$\frac{V_{SAMP\_ERR}}{V_{IN}} = 100 \times \exp\left(\frac{-t}{R_{EQ}C_{TOT}}\right) \tag{3.2}$$

where R_{EQ} is the equivalent switch-on resistance and C_{TOT} is the total capacitance that load the input during the sampling phase. It is obvious from (3.2) that in order to reduce sampling error, either sampling time should be increased or RC time constant should be decreased. Conventionally, several sampling period have to be spent before the conversion cycles start. Since proposed scheme lowers the load capacitance, it is possible to achieve higher accuracy within the same sampling time, or equivalently obtain same accuracy with reduced sampling time.

Although, this topology is very suitable, it has two disadvantages:

1. As pointed out earlier, the noise immunity is essential for the ADCs within the power management ICs. Since the converter shown in Fig. 3.4 achieves signal conditioning
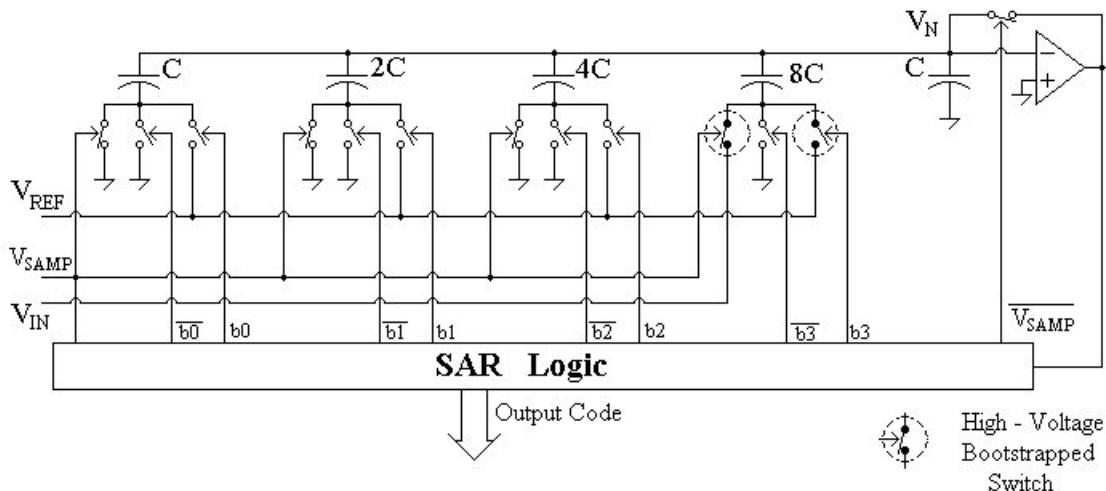
Figure 3.4. Extending the Input Signal Range of a Regular SAR ADC

by attenuating the input signal[4], this topology decreases the LSB level for a given resolution. Therefore, it becomes more difficult to obtain desired accuracy.

2. This topology becomes more and more costly with increasing number of bits because, the area of the capacitor matrix increases exponentially with the number of bits N and for a given matching specification of capacitor matrix[5], the value of the unit capacitor should be increased with increasing number of bits.

Mainly, the noise immunity requirement of the ADC dictates us to seek an alternative converter topology.

3.2.3   11-bits Sub-Ranging SAR Analog to Digital Converter:
Better Noise Immunity

The need for better noise immunity drove us to a more complex converter structure [72]. The general block diagram of the implemented PIC ADC architecture is shown in Fig. 3.5. This is an 11 bits Sub-Ranging analog to digital converter.

The MUX block preceding the first stage of the converter selects desired input channel. Since each one of the eight channel has 0 - 5.5 V signal range, the switches are all implemented using novel high-voltage sampling switch.

The main rational behind the selection of this topology is that it achieve the conversion without attenuating the input signal. Therefore, the minimum input voltage difference that

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[4]as it is clear from eq. 3.1.

[5]Or equivalently, the integral nonlinearity (INL) (or the differential nonlinearity (DNL)) specification of the ADC
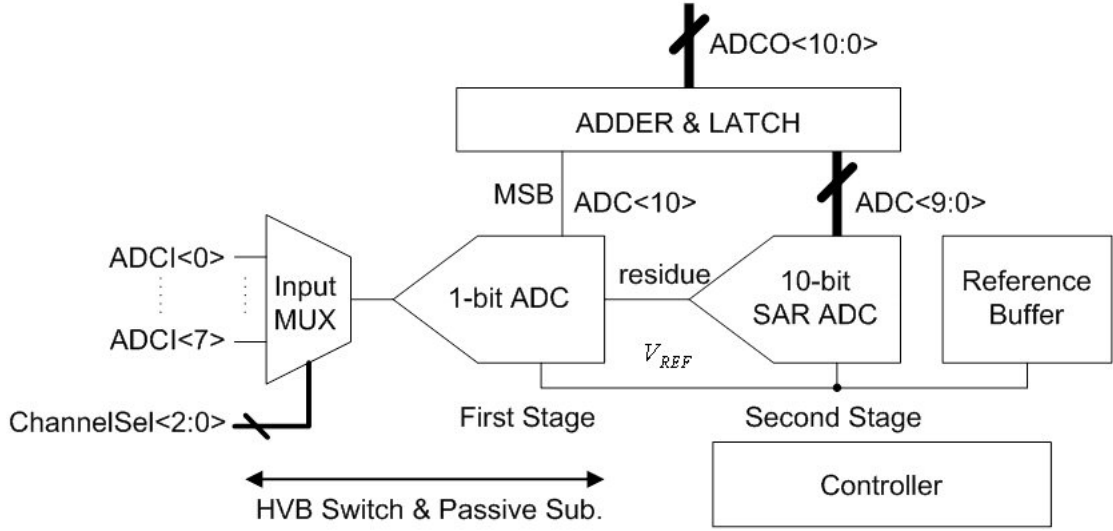
Figure 3.5. 11 bits Sub-Ranging SAR Analog to Digital Converter

this topology should resolve for a given converter resolution is bigger than the topology shown in Fig. 3.4.

The architecture shown in Fig. 3.5 achieves bigger LSB as follows: The first stage can be considered as 1-bit pipeline ADC stage. First, the block compares the input signal with the reference signal to determine the most significant bit of the conversion. The implemented comparator is classical zero-offset clocked comparator[6]. Next, with respect to the MSB, first stage generates the *residue* signal. Since the input signal can go up to twice the reference voltage[7], the residue amplifier of the first stage drive the output either directly to the input signal if the MSB is logic zero or to the difference between the input signal and the reference voltage. Notice that since the input signal is single-ended and the residue signal can change literally from rail to rail, realization of the residue amplifier is a very difficult task. This function is performed by novel high-voltage rail-to-rail passive subtractor block. In summary, the terminal definitions of the first stage are:

$$residue = \begin{cases} V_{ADCI_X} & \text{if } V_{ADCI_X} \leq V_{REF} \\ V_{ADCI_X} - V_{REF} & \text{if } V_{ADCI_X} > V_{REF} \end{cases} \tag{3.3}$$

$$MSB = \begin{cases} 0 & \text{if } V_{ADCI_X} \leq V_{REF} \\ 1 & \text{if } V_{ADCI_X} > V_{REF} \end{cases} \tag{3.4}$$

where V_{ADCI_X} is the input signal at the selected channel X. The scheme is exactly same as

---

[6]First, the input signal is applied to the bottom plate of a capacitor while the top plate is driven by a unity gain configured amplifier. Then with the next phase, reference voltage applied to the bottom plate and the amplifier amplifies the signal at the capacitor top plate to the logic level. This is a widely used standard comparator and its operation principle is very similar to charge-redistribution ADC shown in Fig. 3.3

[7]in other words, the reference voltage is mid of the full-scale input range

pipelined ADCs. Notice that the residue signal is bounded in between the rails.

Except the comparator, which performs one single comparison per conversion and shut down for the remaining of the time, all the blocks within the first stage are passive, so the power consumption of the first stage is negligible[8].

Since the output of the first stage is bounded within the supply levels, the second stage is implemented using classical low-power 10 bit SAR ADC. The SAR ADC has 0.5 LSB systematic offset. The reason of this systematic offset will be clear later on in section 3.5. Due to the aforementioned systematic offset, connecting the first and second stage directly yields to a missing code while the input signal pass through the reference voltage threshold. To solve this problem an extra adder is added to the output. Basically, this block subtract 1 LSB from the result if the MSB is 1. This problem will be further analyzed in section 3.6.

The advantages of the sub-ranging ADC architecture compared to the traditional 11 bit SAR ADC implementations are:

1. Signal conditioning with subtraction allows to keep the least significant bit (LSB) of the overall system twice of the division based signal conditioning alternative, for the same input resolution[9].

2. Passive Subtractor circuit has inherent low pass filtering effect to improve further the noise performance.

3. Resultant capacitor matrix of the 10 bit SAR ADC is smaller yielding better matching and area saving.

4. Extra circuitry to implement the first stage is simple and burns negligible amount of power.

5. There is one single capacitor undergoing to the over voltage stress. Therefore, this topology has better capacitor reliability and it is easier for OVST test.

The reference voltage of the ADC is generated by a low-drop-out voltage regulator (LDO). The output voltage of the LDO is 2.75V. The digital and analog supplies also fed through this LDO. In order to improve the noise performance, the digital and analog supply signals,i.e. DVDD, DVSS, AVDD and AVSS, are all kelvin connected at the IC pad level. The reference signal and the ADC supply pad are further connected at the package level.

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[8]Mainly switching shoot-through current

[9]In other words, we simply did not want to attenuate the input signal in a noisy environment.

3.3 High-Voltage Bootstrapped Sampling Switch (HVB)

Within chapter 2, the effects of the classical solution to the high-voltage input signal, i.e. signal conditioning, are analyzed in details. From the signal sampling point of view, the best signal fidelity is obtained, of course, when the input signal is sampled and processed there after as it is without any signal conditioning. Here, I will show that this is possible. In this work, a novel high-voltage bootstrapped sampling switch

1. capable of sampling input signals well above the supply voltage level

2. without any device reliability issue

3. without forward biasing any parasitic body diode

4. suitable for high-speed applications such as pipelined ADCs

is proposed to solve the problem cited previously by sampling the input signal, *as it is* [73, 74, 75]. The input signal range of the switch is bounded by the drain-bulk breakdown voltage of the MOS devices used, which can be made very large using drain extended MOSFETs or relaxed using proper circuit techniques. Furthermore, drain extended MOS transistors can be fabricated in regular digital CMOS technology without any extra process step (hence without any additional cost).

3.3.1 Bootstrapped Sampling Switch:
Prior Art

I will first review the operation of the well known classical bootstrapped switch that has been extensively used in pipelined ADCs to be able to appreciate the functionality of the proposed switch. Furthermore, since some of the ideas used within the proposed switch is present in classical bootstrapped switch, analyzing conventional one will be beneficiary to the reader to understand the proposed one. The analysis of the novel sampling switch will follow next.

The schematic of the classical bootstrapped switch is shown in Fig. 3.6. First, consider the charge pump formed by transistors M_1, M_2, capacitors C_1, C_2 and the inverter. The charge pump works as follows: assume that initially the voltage across the capacitors C_1 and C_2 are zero, when the clock signal $\overline{\Phi}$ goes high, the top plate of C_1 is pushed to V_{dd} and since the bottom plates of C_2 and C_3 is grounded for this state, those capacitors are charged till their top plate reach to $V_{dd} - V_{TN(M_2,M_3)}$ through M_2 and M_3.

When the clock signal $\overline{\Phi}$ goes low, the top plate of C_2 is pushed well above V_{dd} (or $2V_{dd} - V_{TN(M_2,M_3)}$ to be exact) yielding complete charging of C_1 to V_{dd} through M_1. With the
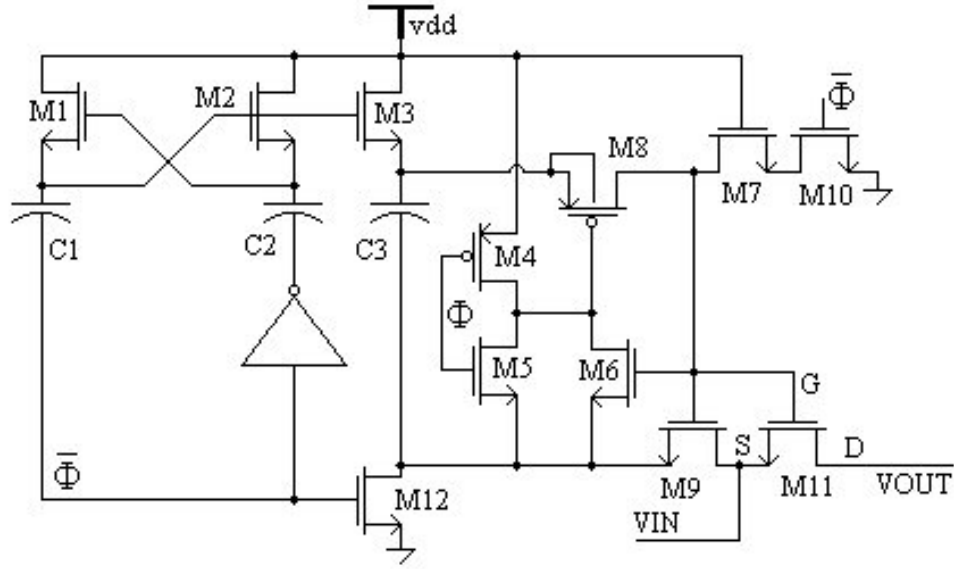
Figure 3.6. Classical Bootstrapped Switch

next phase, when $\overline{\Phi}$ goes high again, since C_1 is charged to V_{dd}, the top plate of C_1 will be pushed to $2V_{dd}$ and the capacitors C_2 and C_3 will be completely charged to V_{dd}.

Therefore, in steady state, C_1, C_2 and C_3 will be charged to V_{dd} and the voltage at the top plates of C_1 and C_2 will change between V_{dd} and $2V_{dd}$ at alternate phases. Classical bootstrapped switch reaches its steady state after at least one clock period.

Under the assumption that all three capacitors are charged to V_{dd}, the bootstrapped switch operates as follows: when $\overline{\Phi}$ goes high, bottom plate of C_3 is grounded and switch M_3 is on, hence C_3 is charged to V_{dd}; M_4 is also on, driving the gate of M_8 to V_{dd}, hence M_8 is off and finally M_{10} is on and grounds the gate terminal of the main switch, i.e. M_{11}. Since their gate terminal is grounded, M_6, M_9 and M_{11} are all off. During this phase, the switch disconnects the input node from the output and charges C_3 to V_{dd}.

When $\overline{\Phi}$ goes low, since M_{10} is off, the gate terminal of M_{11} becomes high impedance. Initially, the bottom plate of C_3 is floating, but because of the fact that M_5 connects C_3 between the gate and source terminal of M_8, this transistor turns on immediately and the charge stored on C_3 starts flowing to the gate terminal of M_{11}. While $V_{G(M_{11})}$ rises, the transistor M_9 turns on and forces the bottom plate of C_3 towards the input voltage, which pushes further the top plate of C_3 to $V_{dd} + V_{IN}$. Eventually this voltage appears at the gate of M_{11} and as a result M_{11} turns on completely to connect the input terminal to the output terminal; M_9 turns on completely to connect input terminal to the bottom terminal of C_3 and M_6 turns on completely to drive the gate of M_8 to the input voltage level. The gate to source voltages of all these four switches, i.e. M_{11}, M_9, M_6 and M_8, are all equal to V_{dd} when

the switch turned on.

3.3.2   Techniques to improve reliability

Although, the transistor M_7 is not functionally needed, it is added to the circuit to reduce V_{DS} and V_{GD} experienced by M_{10}. Notice than the voltage swing of the gate terminal of M_{11} is 0 to $2V_{dd}$. This technique is successfully used also within switching RF power amplifier circuits to protect switch transistors that can undergo excessive drain voltage excursion during initial turn on transient. Alternative to the cascoding technique used in this design, it is also possible to implement M_{10} as a drain-extended MOS transistor if available within the technology. The down side of this scheme is that due to the higher equivalent on-resistance of the switch transistor M_{10} turning off the bootstrapped switch took longer.

An important detail about device reliability is the following: although the boot-strapped switch can be turned on by pulling the gate terminal of M_8 to ground, if the input signal is equal to V_{dd} then the voltage difference between M_8 gate to source terminals would be $2V_{dd}$. For this reason, when the bootstrapped switch is turned on, the $V_{G(M_8)}$ is forced to the input signal through the switch M_6 so that the gate to source voltage of M_8 is bounded within V_{dd} and the reliability of this device is enhanced. The main challenge of this switch is the design of the scheme that protects M_8 by restricting maximum voltage appearing across its terminals.

3.3.3   Limitations of the Traditional switch

Even though, conventional switch performs well for the input signal levels that are within the supply range, it is useless when the input signal exceeds the supply voltage. The reason is the following: When the switch turned on, the input voltage appears at the gate terminal of M_8. As mentioned previously, this is necessary in order to restrict the gate to source voltage of this device to V_{dd}. Since M_4 is a PMOS transistor, if its drain voltage exceed the supply voltage (when the input signal is greater than V_{dd}), its parasitic drain-substrate diode will be forward biased, which will yield a huge current flow through the path formed by M_9, M_6 and parasitic body diode of M_4. The current path through the body diode of M_4 is shown in Fig. 3.7. Aforementioned current path renders conventional bootstrapped switch useless for the applications where input signal level exceed supply voltage.

Another downside of traditional bootstrapped switch is its turn-on and turn-off tran-sients. The slowing effect of M_7 during the turn-off transient is already mentioned previously. During the turning-on of the switch, the gate terminal of M_{11} is slowly pushed to $V_{dd} + V_{IN}$ with the gradual turn-on of the switch M_9. Of course, to improve the response time the
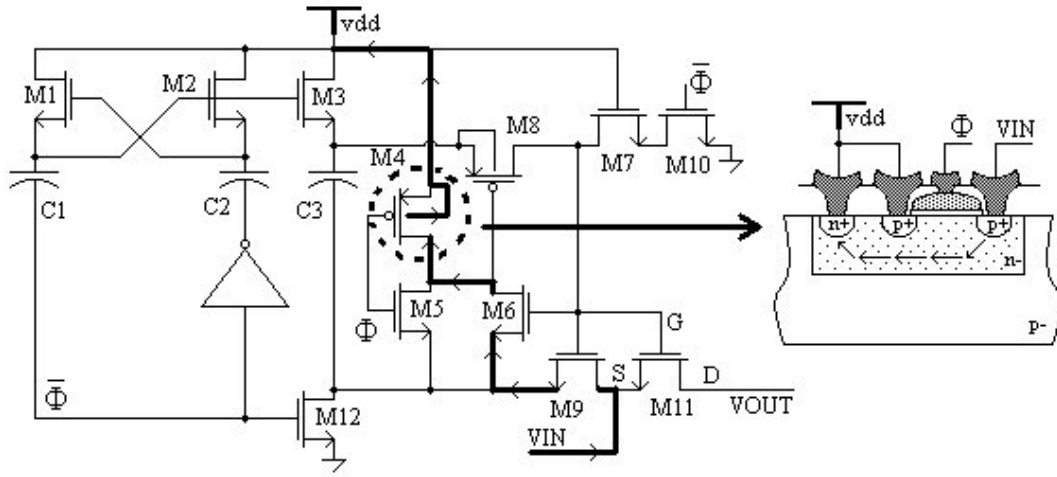
Figure 3.7. The current path due to the parasitic body diode of M_4

aspect ration of M_9 should be chosen as large as possible, which will increase the capacitive load at the control node yielding bigger C_3 to be able to charge it to the desired switch on gate overdrive voltage. Therefore, it is possible to conclude that there is a trade-off between turn-on transient time and the required silicon area.

3.3.4 Towards supply-voltage independent sampling switch: Novel High-Voltage Bootstrapped Sampling Switch

Novel sampling switch improves the traditional bootstrapped switch by

1. allowing the sampling of the input signal exceeding supply voltage level and

2. improving the turn-on transient time

with the same device reliability conditions. The schematic of the new switch is shown in Fig. 3.8.

The switch operates as follows: The operation of the charge-pump formed by M_1, M_2 and C_1, C_2, is explained previously while analyzing conventional switch. Same conclusions are also valid for this circuit. Hence, capacitors C_1, C_2 are charged to V_{dd} after one clock period once the clock is applied; and the nodes N_1 and N_2 change between V_{dd} and $2V_{dd}$, at alternate phases. It is obvious from the schematic that when N_1 goes to $2V_{dd}$ (when $\overline{\Phi}$ goes high) to turn on M_7, N_3 is grounded (because M_6 is on), hence C_3 is also charged to V_{dd}.

The sub-circuit formed by M_3-M_6, M_9 and M_{10} is a simple level shifter. It is widely used in digital designs when it is necessary to convey a logic signal between digital blocks having different power supply level. When the differential clock signals, i.e. Φ and $\overline{\Phi}$, are applied to M_5 and M_6, the positive feedback created by PMOS transistors M_3 and M_4 forces
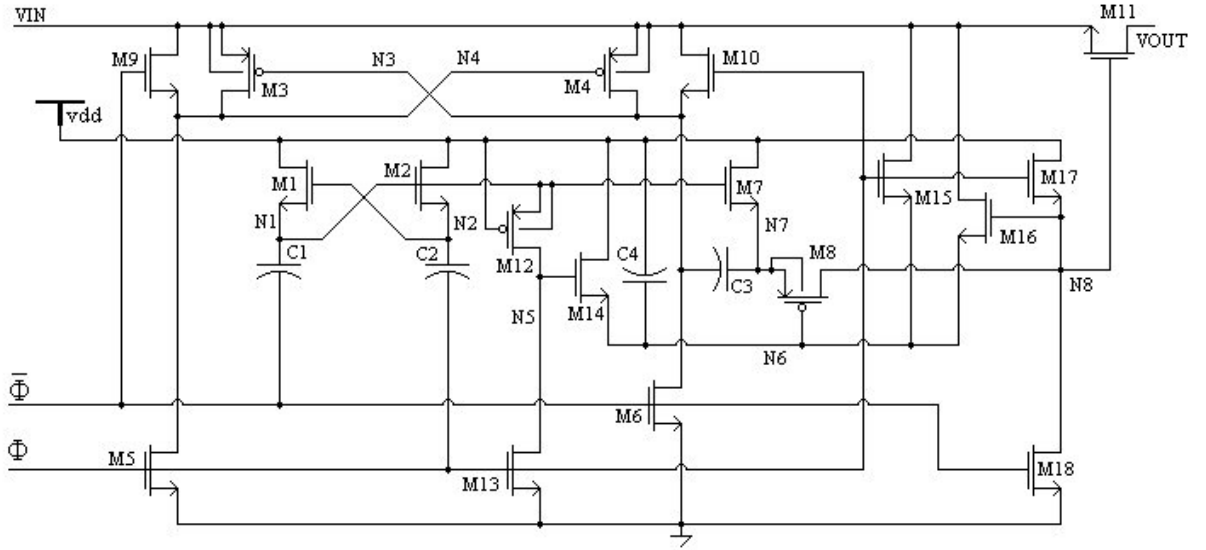
Figure 3.8. Proposed High-Voltage Bootstrapped Sampling Switch

one of the output nodes, i.e. N_3 or N_4, to go to ground and the other to go to input voltage level. The transistors M_9 and M_{10} are used to guarantee this behavior when the input signal level is very low, i.e. close or equal to the threshold voltage of M_3 and M_4. If the input signal is low, there is not enough gate-over drive for M_3 and M_4 to switch the state of the level shifter, but for this case M_9 or M_{10}, driven by the clock signals, will act as a switch and will drive the appropriate output node to the input voltage. To avoid meta stable condition, M_5 and M_6 should be designed much stronger than M_3 and M_4. In short, level shifter operates such that nodes N_3 and N_4 change between 0 and V_{IN}, at alternate phases.

Before analyzing the operation of the bootstrapped switch, we have to analyze the circuit formed by M_{12}-M_{14}. Notice that the source terminal of M_{12}, together with its bulk terminal, is connected to N_1, hence it changes between V_{dd} and $2V_{dd}$. Since the gate terminal of M_{12} is connected to V_{dd}, when N_1 goes to $2V_{dd}$ ($\overline{\Phi}$ goes high), M_{12} turns on and charges N_5 to $2V_{dd}$ to turn on M_{14}. At the alternate phase, the gate to source voltage of M_{12} is zero, hence it is off. Since M_{13} is on during this phase, N_5 is drained to ground and consequently M_{14} is off. In short, node N_5 changes between $2V_{dd}$ and 0.

Notice that even though the gate to source voltage of M_{13} is less than or equal to V_{dd}, the drain to gate voltage of this device can go twice as high. Therefore it is necessary to protect this device from over voltage stress. This can be achieved with either using a cascode device to divide the stress among two devices, exactly like M_7 in Fig. 3.6 or M_{13} has to be chosen as drain extended device.

Let us now analyze the main bootstrapped switch: during off phase ($\overline{\Phi}$ is high), M_{18} is on, therefore N_8 is at ground and the switch is off. N_1 is at $2V_{dd}$, hence M_{12} is on and

therefore M_{14} is on driving N_6 to V_{dd}. M_6 is on, hence the bottom plate of C_3 is at ground and M_7 is on charging the top plate of C_3, i.e. N_7, to V_{dd}. Since N_6 and N_7 are both at V_{dd}, M_8 is off. And finally M_{15}, M_{16} and M_{17} are all off.

At the beginning of the switch turn-on phase, the transistor M_{17} begins charging node N_8 till it reaches to $V_{dd} - V_{T(M_{17})}$. From this point on, M_{17} is off, since it does not have enough gate overdrive to conduct. Furthermore, when the charge stored on C_3 takes over and drive node N_8 to $V_{dd} + V_{IN}$, M_{17} is completely turned off. Although, this device is not required for proper operation of the switch, it is added to improve its turn-on transient.

With the rising edge of the clock signal Φ, node N_3 is pushed to V_{IN}; since C_3 is already charged to V_{dd}, the top plate of C_3, i.e. node N_7, goes to $V_{dd} + V_{IN}$ immediately and the charge on C_3 passes through M_8 to charge node N_8. There are two distinct mechanisms that turn M_8 on by forcing node N_6 to V_{IN} in three different input signal regions:

1. When input signal is within the range $V_{dd} - V_{T(M_{15})} < V_{IN}$, transistor M_{15} is always off[10]. For this case, M_8 is turned on as follows: initially since M_{14} is turned off, node N_6 is floating and it is at V_{dd}. When N_7 pushed to $V_{dd} + V_{IN}$, the voltage on node N_6 increases because of the capacitive coupling from N_7 to N_6 through the parasitic C_{GS} of M_8. The voltage on N_6 at the end of this transition can be expressed as:

$$V_{N6} = V_{dd} + \frac{C_{GS(M_8)}}{C_{GS(M_8)} + C_4} V_{IN} \tag{3.5}$$

Hence, the gate to source voltage of M_8 can be expressed as

$$V_{GS(M_8)} = -\left(1 - \frac{C_{GS(M_8)}}{C_{GS(M_8)} + C_4}\right) V_{IN} \tag{3.6}$$

Since input signal is large enough, it is possible to make the $V_{GS(M_8)}$ greater than the threshold voltage of M_8 and turn it on by properly choosing the value of C_4. Once, M_8 is turned on, C_3 charges N_8 to $V_{dd} + V_{IN}$, which will turn on M_{11} to connect input signal to output and at the same time M_{16} will further drive N_6 to V_{IN}. Notice that M_8 is protected from over voltage stress.

2. When the input signal is within the range $0 < V_{IN} < V_{T(M_8)}$. Under this condition, regardless of the value of C_4, it is not possible to make gate to source voltage of M_8 greater than $V_{T(M_8)}$ using the transient on N_7, as it is clear from (3.6). But for this case, since the input signal is low enough, transistor M_{15} driven by the clock signal will turn on and drain N_6 from V_{dd} towards input voltage. Furthermore, once M_8 turns on and N_8 is charged to $V_{dd} + V_{IN}$, M_{16} turns on also to force N_6 further towards input signal level.

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[10] M_{15}'s drain voltage is equal to V_{IN}, its gate voltage is at V_{dd} and its source voltage is initially at V_{dd} and then at V_{IN}

3. When the input signal is within the range $V_{T(M_8)} < V_{IN} < V_{dd} - V_{T(M_{15})}$, both of the mechanisms described above are active and drives the node N_6 towards input signal level.

Compared to the traditional bootstrapped switch, novel HVB sampling switch has better turn-on transient behavior. Proposed circuit, Fig. 3.8. pushes the bottom plate of C_3 immediately to the input voltage. Furthermore, M_{17} helps at the beginning of the turn on transition for faster response. This extra speed can be very useful for pipelined ADC system where the speed of the switch turn-on is as important as its accuracy. The trade-off for this extra-speed is small shoot-through current flowing from the input node to ground through the level shifter circuit.

3.3.5 Reliability issues of the Novel Switch

As mentioned previously, the main challenge of the bootstrapped switch is the design of a scheme that protects the PMOS pass transistor M_8 by restricting maximum voltage appearing across its terminals. There exist other, three different bootstrapped switch designs that basically implement different protection scheme to restrict over voltage stress of M_8, while achieving same switching functionality. Proposed high voltage bootstrapped switch has evolved from those early versions. The earlier version of HVB switch will briefly be presented within appendix E.

The voltage variations on the nodes of the HVB switch for both phases are given in Table 3.2. Terminal voltages and the worst case over voltage stress of the devices during $\Phi = V_{dd}$ and during $\Phi = 0$ are summarized in Table 3.3 and in Table 3.4, respectively. Listed worst case device over stress voltages show the maximum device terminal voltage difference that might appear during the regular operation. Notice that since it is assumed that input signal can exceed supply voltage, some of the worst case over stress voltage is equal to input signal. It is necessary to take appropriate precaution to improve reliability of the sampling switch. Proposed HVB switch is designed for TI LBC7 technology that supports 3V, 5V, 7V CMOS devices as well as 7V, 12V, 20V, 24V, 28V and 30V drain-extended MOS devices. Although it is not necessary, for the current implementation reliable operation of the switch is guaranteed by suitable device selection to avoid redundant extra circuitry.

Except the transistors M_3 and M_4 in Fig. 3.8. the operation range of the switch is bounded by the drain-bulk breakdown voltage of the MOS transistor used. Therefore, it is possible to use cascoding technique to reduce over voltage stress for all these devices in case high-voltage drain-extended MOS transistors are not available. With a small change within level shifter circuit, it is possible to expand the operation range of the level shifter

Table 3.2. Node voltages during two phases of operation and maximum voltage swing

Node	$\Phi = V_{dd}$	$\Phi = 0$	Voltage Swing
N_1	V_{dd}	$2V_{DD}$	V_{dd} -$2V_{dd}$
N_2	$2V_{dd}$	V_{DD}	V_{dd} -$2V_{dd}$
N_3	V_{IN}	0	0 - V_{IN}
N_4	0	V_{IN}	0 - V_{IN}
N_5	0	$2V_{DD}$	0 - $2V_{dd}$
N_6	V_{IN}	V_{DD}	0 - V_{IN}
N_7	$V_{dd} + V_{IN}$	V_{DD}	V_{dd} - $(V_{dd} + V_{IN})$
N_8	$V_{dd} + V_{IN}$	0	0 - $(V_{dd} + V_{IN})$

again to the drain-bulk breakdown voltage. The schematic of this minor modification is also given within the appendix E. Since appropriate devices were available within the technology, simple circuit solution is preferred for the implementation.

HVB switch is intended to sample input signal changing within 0 - 5.5V. Even though the power supply voltage for the current implementation is chosen as 2.75, it can be chosen much smaller. The measurement results confirm the proper operation of the HVB switch with only 1.2V supply voltage and up to 6V input signal. The charge-pump circuit needs a supply voltage level twice the NMOS threshold voltage. Obviously, minimum supply voltage level is ultimately bounded by the threshold voltage of the switch transistor and expected minimum switch transistor gate over-drive.

3.3.6   Simulation and Measurement Results

Fig. 3.9 shows the simulated gate drive voltage as a function of the input voltage. V_{dd} is equal to 2.75 V and the input range is from 0 to 5.5 V ($2V_{dd}$). Observe that the driving voltage is slightly less than V_{dd} for low input signals and drops by just about 200 mV when the input is almost twice the supply voltage. The result makes the switch suitable for high-frequency sampling: the high-driving voltage and its limited drop will determine a small harmonic distortion. The main reason for the decrease of effective gate-overdrive at higher input signal level is the parasitic capacitance loading node N_8. The loss of gate overdrive can be compensated by increasing the value of C_3.

Fig. 3.10 shows the simulated waveforms for an input sine wave with a swing of 0-5.5 V. The supply voltage is 2.75 V. The gate voltage during the on phase tracks the input signal and is shifted up by approximately 2.75 V.
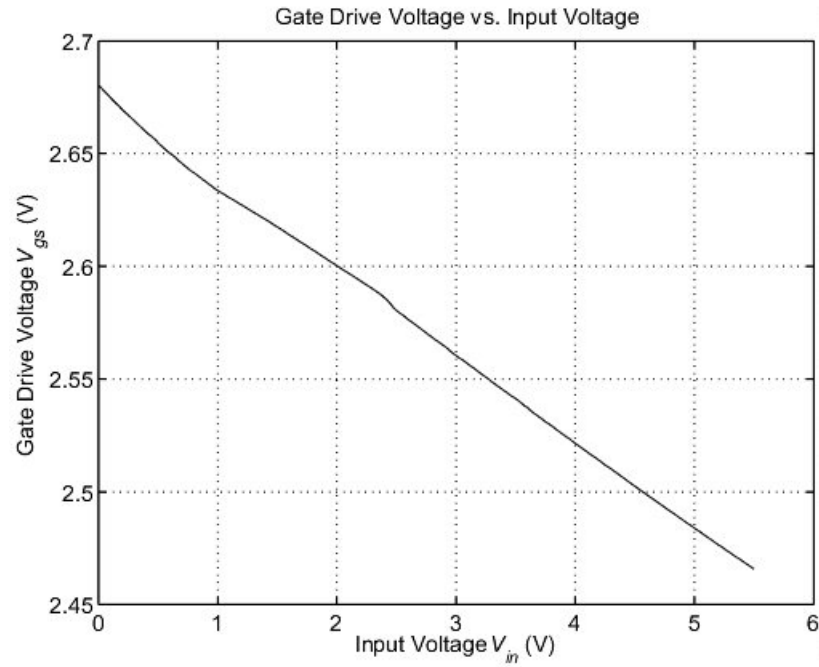
Figure 3.9. Gate Drive Voltage V_{GS} vs. Input Voltage V_{IN}
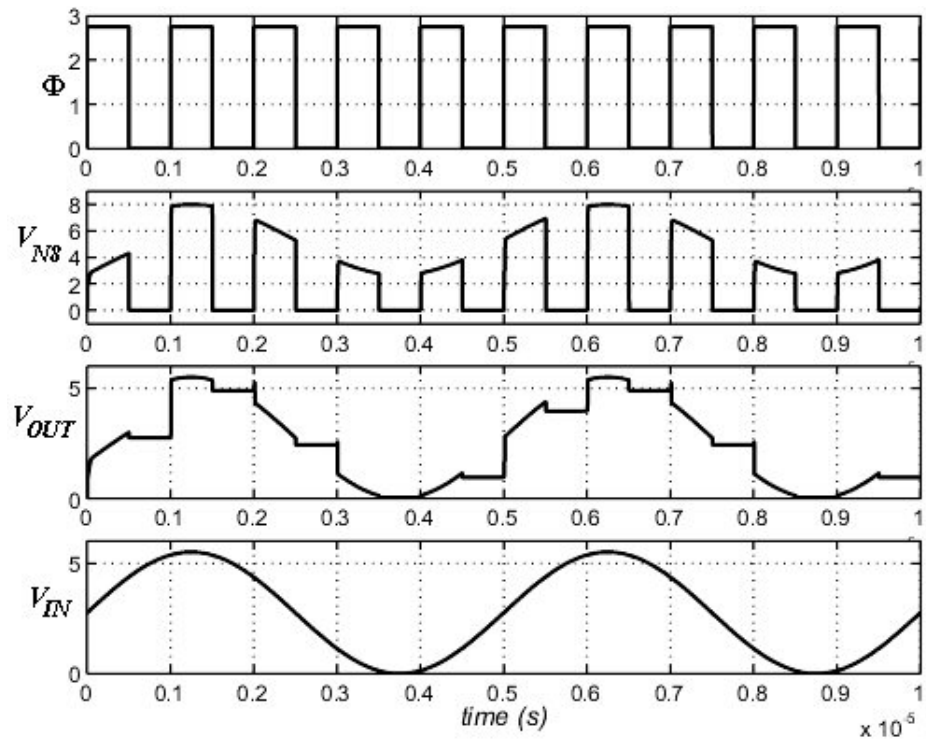
Figure 3.10. Simulated Switch Behavior with a Dynamically Changing Input Signal

Table 3.3. Terminal Voltages of the Transistors and the worst case over voltage stress during $\Phi = V_{dd}$

| Transistor | $\Phi = V_{dd}$ | | | | |
	V_D	V_G	V_S	V_B	Worst Case Stress
M_1	V_{dd}	$2V_{dd}$	V_{dd}	0	$V_{dd}\,(1)$
M_2	V_{dd}	V_{dd}	$2V_{dd}$	0	$2V_{dd}\,(V_{SB})$
M_3	0	V_{IN}	V_{IN}	V_{IN}	$V_{IN}\,(V_{GD})$
M_4	V_{IN}	0	V_{IN}	V_{IN}	$V_{IN}\,(V_{GS})$
M_5	0	V_{dd}	0	0	V_{dd}
M_6	V_{IN}	0	0	0	$V_{IN}\,(V_{GD})$
M_7	V_{dd}	V_{dd}	$V_{dd}+V_{IN}$	0	$V_{dd}+V_{IN}\,(V_{SB})$
M_8	$V_{dd}+V_{IN}$	V_{IN}	$V_{dd}+V_{IN}$	$V_{dd}+V_{IN}$	V_{dd}
M_9	V_{IN}	0	0	0	$V_{IN}\,(V_{GD})$
M_{10}	V_{IN}	V_{dd}	V_{IN}	0	$V_{IN}\,(V_{SB})$
M_{11}	V_{IN}	$V_{dd}+V_{IN}$	V_{IN}	0	$V_{dd}\,(1)$
M_{12}	0	V_{dd}	V_{dd}	V_{dd}	V_{dd}
M_{13}	0	V_{dd}	0	0	V_{dd}
M_{14}	V_{dd}	0	V_{IN}	0	$V_{IN}\,(V_{SB})$
M_{15}	V_{IN}	V_{dd}	V_{IN}	0	$V_{IN}\,(V_{SB})$
M_{16}	V_{IN}	$V_{dd}+V_{IN}$	V_{IN}	0	$V_{dd}\,(1)$
M_{17}	V_{dd}	V_{dd}	$V_{dd}+V_{IN}$	0	$V_{dd}+V_{IN}\,(V_{SB})$
M_{18}	$V_{dd}+V_{IN}$	0	0	0	$V_{dd}+V_{IN}\,(V_{GD})$

Fig. 3.11 shows the corresponding measured sampled signal. The switch is used in a simple track and hold configuration. The clock signal, input signal and the supply voltage level is apparent in the figure and the output behaves as expected. Even if the input goes up to twice the supply voltage, the obtained output signal tracks the input signal very well. The current flowing from the input node was negligible (less than 1 μA) during the measurement proving that none of the parasitic body diode is forward biased.

The nominal supply voltage is 2.75 V. However the circuit can operate with a lower supply voltage. Measurement results show that the circuit operates properly for a supply voltage as low as 1.2 V. With this supply voltage the switch can work with input signals up to 6 V. Therefore, the obtained maximum ratio of V_{in}/V_{dd} is 5.

Table 3.4. Terminal Voltages of the Transistors and the worst case over voltage stress during $\Phi = 0$

Transistor	$\Phi = 0$				
	V_D	V_G	V_S	V_B	Worst Case Stress
M_1	V_{dd}	V_{dd}	$2V_{dd}$	0	$2V_{dd}\,(V_{SB})$
M_2	V_{dd}	$2V_{dd}$	V_{dd}	0	$V_{dd}\,(1)$
M_3	V_{IN}	0	V_{IN}	V_{IN}	$V_{IN}\,(V_{GS})$
M_4	0	V_{IN}	V_{IN}	V_{IN}	$V_{IN}\,(V_{GD})$
M_5	V_{IN}	0	0	0	$V_{IN}\,(V_{GD})$
M_6	0	V_{dd}	0	0	V_{dd}
M_7	V_{dd}	$2V_{dd}$	V_{dd}	0	$V_{dd}\,(1)$
M_8	0	V_{dd}	V_{dd}	V_{dd}	V_{dd}
M_9	V_{IN}	V_{dd}	V_{IN}	0	$V_{IN}\,(V_{SB})$
M_{10}	V_{IN}	0	0	0	$V_{IN}\,(V_{GD})$
M_{11}	V_{OUT}	0	V_{IN}	0	$V_{IN}\,(V_{GS})$
M_{12}	$2V_{dd}$	V_{dd}	$2V_{dd}$	$2V_{dd}$	V_{dd}
M_{13}	$2V_{dd}$	0	0	0	$2V_{dd}\,(V_{GD})$
M_{14}	V_{dd}	$2V_{dd}$	V_{dd}	0	$V_{dd}\,(1)$
M_{15}	V_{IN}	0	V_{dd}	0	$V_{IN}\,(V_{GD})$
M_{16}	V_{IN}	0	V_{dd}	0	$V_{IN}\,(V_{GD})$
M_{17}	V_{dd}	0	0	0	V_{dd}
M_{18}	0	V_{dd}	0	0	V_{dd}

3.4   High-Voltage Passive Subtractor (HPS)

3.4.1   Ideal Transfer Function

The high-voltage passive subtractor circuit designed to realize residue amplifier of the 11-bit ADC's input stage. The block works as follows: If the input signal is smaller than the reference voltage, the output of the block is equal to the input signal. If the input signal is bigger than the reference voltage, the block subtracts a constant voltage, i.e. reference voltage V_R, from the input signal and drives the output. The ideal output transfer function of HPS is as shown in Fig. 3.12.

HPS contains a comparator to implement conditional branching described above, a by-pass transistor to implement lower part of the transfer function, a passive subtractor
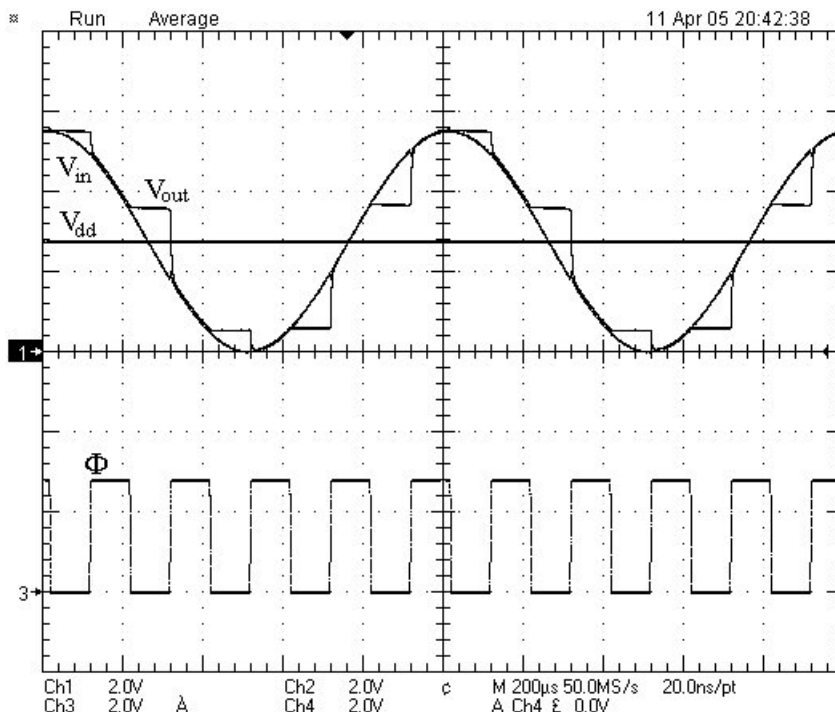
Figure 3.11. Measured Switch Behavior with a dynamically Changing Input Signal

circuit to implement higher part of the transfer function and finally some digital logic to control process flow. The implementation of the comparator is pretty strait forward: During the first phase, the reference voltage V_R is stored on an input capacitor. The offset of the comparator is stored at the same time. Then, with the next phase, the input signal is applied to the capacitor so that the voltage difference between the input and the reference voltage appears at the input of the comparator. The comparator amplifies this difference to logic level. If the output is logic zero meaning that the input signal is smaller than the reference voltage then the MSB bit is set to zero and the by-pass transistor is activated to connect the input signal to the output. The by-pass transistor is a high-voltage bootstrapped sampling switch. If the output of the comparator is logic one, then MSB bit set to one and the passive subtractor block is activated to subtract the reference voltage from the input. The power consumption of the comparator is negligible; it is activated once during the conversion to make the decision and turned off for the remaining of the time.

The most challenging part of the block, in terms of implementation, is the subtractor circuit. This sub-block cannot be implemented using classical feedback amplifier topologies because of the following facts: the input signal is single-ended and the reference voltage of the system is equal to the power supply voltage. Therefore, the output signal of the block
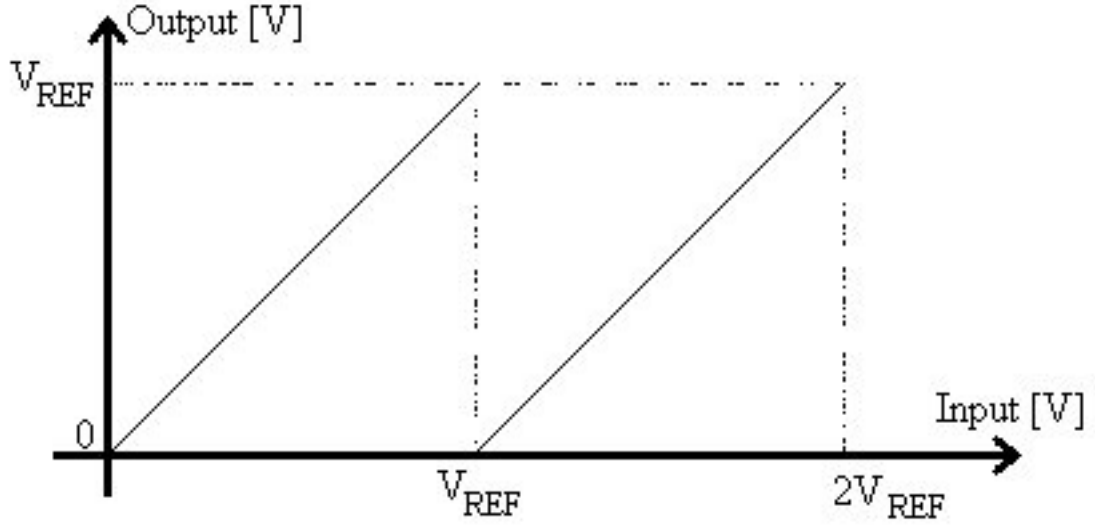
Figure 3.12. Simplified Schematic of HPS

changes literally rail-to-rail[11] while input signal is changing from V_R to $2V_R$. It is not possible to design an output stage that can operate in such condition. A novel passive circuit that can operate truly rail-to-rail is developed to perform the subtraction operation. The circuit has no static power consumption. As it is obvious, the HPS block is named after passive subtractor circuit.

In summary, the ideal transfer function of the whole passive subtractor block is

$$V_O = \begin{cases} V_I & \text{if } V_I \leq V_R \\ V_I - V_R & \text{if } V_I > V_R \end{cases} \tag{3.7}$$

3.4.2 Passive Subtractor Transfer Function

The schematic in Fig. 3.13 shows only the passive subtractor sub-block [72]. For the rest of the section, I will refer this circuit as HPS since it is the core of the whole block and assume the functionality of the remaining sub-blocks as described above. The circuit requires three clock phases, i.e. Φ_1, Φ_2 and Φ_3. The clocking scheme is given in Fig. 3.14. Switches S_1 and S_2 are high-voltage bootstrapped switches. A simple digital inverter drives clock Φ_3 between 0 and V_R. A careful observer should already notice that HPS is actually a so called parasitic sensitive switched capacitor filter. Capacitor denoted C_P represents parasitic capacitor associated to node N_1. Since the capacitor C_2 is grounded the parasitic capacitance on N_2 can be combined with it.

The circuit operates as follows: While the circuit is idle, the bottom plate of C_1 is held at V_R. Since the input signal of the block can exceed the supply voltage, this way, the

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[11]Notice that the ADC's LSB is 2.688mV
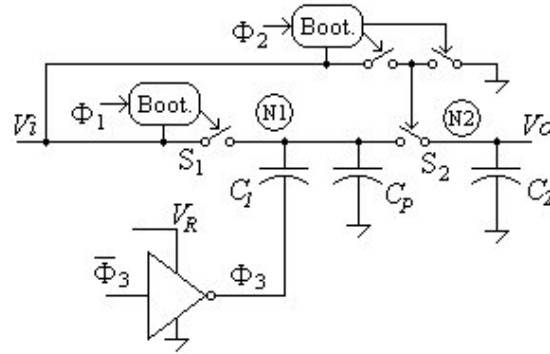
Figure 3.13. Simplified Schematic of HPS
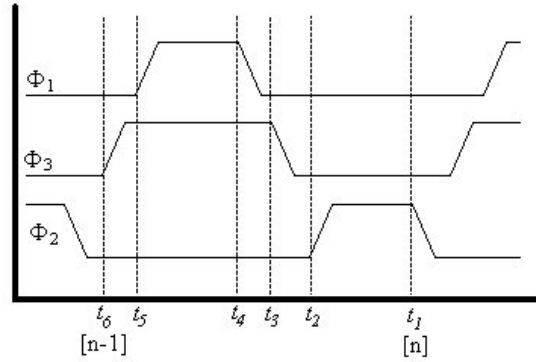
Figure 3.14. Switching timing diagram of HPS

oxide stress of the capacitor C_1 is reduced to improve device reliability. When the block is activated, the top plate of C_1 is connected to the input node through S_1 to store a charge equal to $C_1(V_{IN} - V_R)$. Then, the input node is disconnected from N_1 by turning off S_1. Next, the bottom plate of C_1 is pulled to ground. Ideally, the voltage on the node N_1 should be equal to $V_{IN} - V_R$ because of the charge conservation principle at the end of this phase. Node N_1 is connected to the output through S_2 to transfer the charge of C_1 to C_2. After the charge transfer, the switch S_2 is turned off to disconnect the output node from N_1 and then the bottom plate of C_1 is pushed back to V_R. This charge transfer scheme is repeated multiple times so that both capacitors, i.e. C_1 and C_2, are charged to $V_{IN} - V_R$. This sequence of events can easily be verified with the help of Fig. 3.13 and Fig. 3.14.

The error at the output of HPS goes to zero, ideally, after infinite number of period. Therefore, this structure is suitable only for systems having low input frequencies. The analysis showing required number of clock period to settle within a given error margin will be given later in this section. Notice that subtraction is obtained without any amplifier. HPS has two distinct advantages: 1. as oppose to the classical feedback amplifier implementation, HPS output signal can change rail-to-rail; 2. there is no static supply current so it is

inherently very low power.

Z-domain transfer function of HPS can be calculated using charge conservation equations on nodes N_1 and N_2:

$$V_O[n] = \frac{1}{C_1 + C_2 + C_P}[C_2 V_O[n-1] + C_1(V_I - V_R) + C_P V_I] \tag{3.8}$$

For the sake of simplicity, let define

$$a \equiv \frac{C_2}{C_1 + C_2 + C_P}, \quad b \equiv \frac{C_1}{C_1 + C_2 + C_P}, \quad c \equiv \frac{C_P}{C_1 + C_2 + C_P} \tag{3.9}$$

Using (3.9), (3.8) can be simplified to

$$V_O[n] = a V_O[n-1] + b(V_I - V_R) + c V_I \tag{3.10}$$

Therefore, the z-domain transfer function of the output signal including the error associated with C_P can be expressed as

$$V_O(z) = \frac{b}{1 - az^{-1}}(V_I - V_R) + \frac{c}{1 - az^{-1}}V_I \tag{3.11}$$

3.4.3 DC response and output error due to parasitic capacitance C_P

The final value theorem gives the DC response of HPS:

$$V_{O(DC)} = \lim_{z \to 1} V_O(z) = \frac{b}{1-a}(V_I - V_R) + \frac{c}{1-a}V_I \tag{3.12}$$

Notice that non ideal transfer function (3.12) reduces to ideal transfer function (3.7) while parasitic capacitance C_P goes to 0. The output error due to the parasitic C_P at the output can be expressed by subtracting the ideal HPS transfer function (3.7) from (3.12). Hence, DC output error is (using (3.9)) :

$$V_{OE(DC)} = \frac{C_P}{C_1 + C_P}V_R \tag{3.13}$$

Equation (3.13) suggests that the error is independent of the input signal. Although the result suggests that the error is constant (because V_R is constant), because of the fact that most of the parasitic capacitance on node N_1 is junction capacitance, C_P and therefore the output error changes with the input signal. Variation of the unit area junction capacitance with respect to the voltage across its terminals for typical CMOS process is shown in Fig. 3.15. Hence, in general case, error signal can be expressed as

$$V_{OE(DC)} \cong \frac{C_P(V_I)}{C_1 + C_P(V_I - V_R)}V_R \tag{3.14}$$

In order to obtain a design equation to bound the output error to a given value for a given C_P, let define that

$$C_P \equiv \max_{V_I}(C_P(V_I), C_P(V_I - V_R)) \tag{3.15}$$
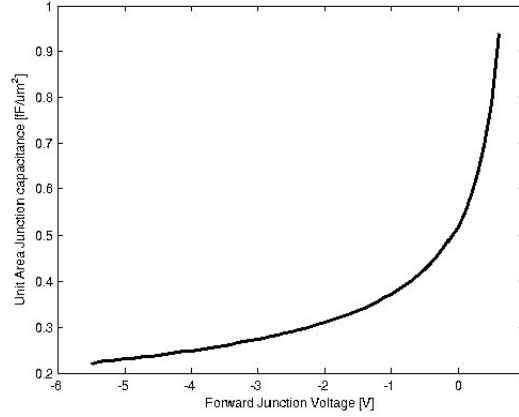
Figure 3.15. Unit Area capacitance variation of a junction capacitance for typical CMOS process

Since the reference voltage V_R is a given system level parameter, the only possible way of reducing the output error is by increasing C_1. For an N-bit ADC the reference voltage V_R is equal to 2^{N-1} LSB, therefore for bounding the error within the fraction α of an LSB ($0 < \alpha < 1$), C_1 should be chosen as

$$\frac{C_P}{C_1 + C_P} 2^{N-1} LSB < \alpha LSB \tag{3.16}$$

$$C_1 > \left(\frac{2^{N-1}}{\alpha} - 1\right) C_P \tag{3.17}$$

The design equation (3.17) is a very restrictive one because of its exponential nature. Sampling capacitor C_1 becomes quite large for high resolution system. For example, bounding the HPS output error in an 11-bit ADC to 0.2LSB requires a sampling capacitance higher than 51pF for just 10fF parasitic capacitance. As a design guideline, we can conclude that the switch transistors connected to node N_1 should be chosen as small as possible.

3.4.4 Settling Time

Let consider now the ideal case, assume that C_1 and $C_2 >> C_P$ and define $V_{IN} \equiv V_I - V_R$, we can simplify (3.11) using (3.9) as

$$\frac{V_O(z)}{V_{IN}(z)} = \frac{1 - a}{1 - az^{-1}} \tag{3.18}$$

DC response of the transfer function (3.18) is equal to 1 (or equivalently there is no DC error) but this response is obtained after infinite number of clock period. For practical implementations, it is necessary to assume that circuit reaches steady state after n (finite number) clock period for a given error margin, i.e. a fraction α of an LSB ($0 < \alpha < 1$). To

analyze required number of period to reach steady-state, assume that step input signal is applied to the input:

$$V_{IN}(t) = V_{IN}u(t) \Leftrightarrow V_{IN}(z) = \frac{1}{1 - z^{-1}}V_{IN} \tag{3.19}$$

By substituting (3.19) into (3.18), the output signal can be rewritten as

$$V_O(z) = \frac{1 - a}{1 - az^{-1}}\frac{1}{1 - z^{-1}}V_{IN} \tag{3.20}$$

The inverse z-transform of (3.20) is

$$V_O[n] = V_{IN} - a^{n+1}V_{IN} \tag{3.21}$$

Notice that $a < 1$, therefore $V_O[n]$ is convergent. The first term in (3.21) is the DC solution; the second term is the error. The maximum value of V_{IN} is equal to $2^{N-1}LSB$ for N bit ADC and occurs when full-scale voltage is applied. The minimum number of cycle n required to reach steady state under worst case condition can be expressed as:

$$\max_{V_{IN}}(a^{n+1}V_{IN}) = a^{n+1}2^{N-1}LSB < \alpha LSB \tag{3.22}$$

Using (3.9) and ignoring C_P, (3.22) can be rewritten as

$$n > \frac{\log\frac{\alpha}{2^{N-1}}}{\log a} - 1 = \log_{\left(1 + \frac{C_1}{C_2}\right)}\frac{2^{N-1}}{\alpha} - 1 \tag{3.23}$$

Due to the fact that the settling behavior of the HPS is exponential, the design equation (3.23) is much easier to satisfy compared to (3.17).

3.4.5   Filtering

As it is clear from (3.18), HPS is actually a switched capacitor low pass filter. -3dB cut-off frequency of the filter can be calculated as follows:

$$|H(jw)|_{-3dB} = \frac{1 - a}{\sqrt{(1 - a\cos(w))^2 + a^2\sin^2(w)}} = \frac{1}{\sqrt{2}} \tag{3.24}$$

Substituting (3.9) in (3.24), ignoring C_P and solving the equation for ω yields:

$$\frac{f_{-3dB}}{F_S} = \frac{1}{2\pi}\cos^{-1}(\frac{3}{2} - \frac{1}{2}(\frac{C_1 + C_2}{C_2} - \frac{C_1}{C_1 + C_2})) \tag{3.25}$$

The variation of -3dB frequency of the HPS as percentage of the sampling frequency F_S for different C_1/C_2 ratio is shown in Fig. 3.16. As it is clear from the figure, better filtering requires smaller C_1 which contradicts the requirement of the precision and fast settling obtained previously. The Bode plots of the HPS for three different C_1/C_2 capacitive ratios are shown in Fig. 3.17. X-axis is normalized to the sampling frequency F_S.
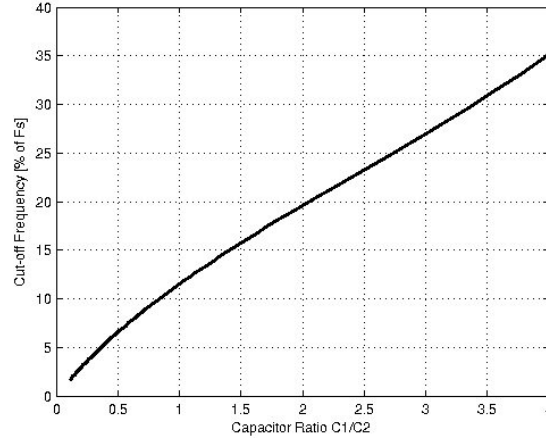
Figure 3.16. -3dB Bandwidth of the passive subtractor as a percentage of sampling frequency F_S for different C_1/C_2 ratio

The error introduced by the passive subtractor at the output while processing time varying input signals can also be analyzed using z-domain transfer function of the block. The error introduced for this case can be expressed in terms of gain variation of the transfer function and then the input signal bandwidth can be extracted for a given error margin from the transfer function.

3.4.6 The effect of switch channel charge injection

It is possible to sample the output node at two different phases: t_1 or t_6 as shown in Fig. 3.14. Detailed analyze of the HPS reveals that the error introduced by the channel charge injection of the switches S1 and S2 differs with respect to output sampling phase. Assuming that reference voltage V_R is equal to power supply voltage and neglecting body effect, the output error term created by the switch channel charges can be expressed at time t_1 and time t_6, respectively, as follows:

$$V_{OE\_CHI\_t1} = \frac{1}{2}\frac{C_{OX}WL(V_R - V_T)}{C_1} \tag{3.26}$$

$$V_{OE\_CHI\_t6} = -\frac{1}{2}\frac{C_{OX}WL(V_R - V_T)}{C_2} \tag{3.27}$$

where C_{OX}, W, L and V_T are unit area gate capacitance, channel width, channel length and the threshold voltage of the switch transistor used. Final remark, sampling the output signal after turning S2 off, i.e. at t_6, is advantageous because it is possible to partially cancel the error introduced by the parasitic capacitance C_P, expressed in (3.13).
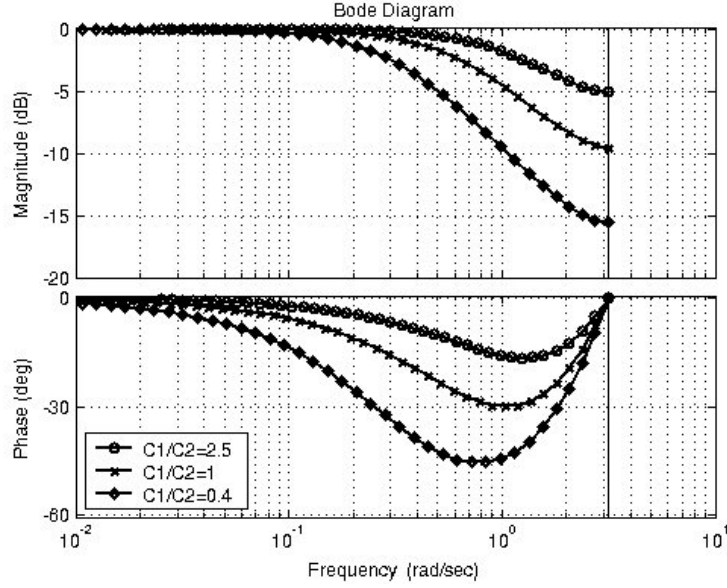
Figure 3.17. The Bode plot of the passive subtractor for different C_1/C_2 ratio

3.4.7 Power issues

As it is clear from Fig. 3.13. in principle, there is no static supply current in HPS block. There will be shoot-through current and a small switching current flowing within the high-voltage bootstrapped switches. The capacitors C_1 and C_2 are charged only once to $V_{IN} - V_R$ from their previous states. Therefore, except for abnormally large C_1 and C_2 values, the current that is used to charge these capacitors can be easily ignored.

For high-resolution systems, where C_1 should be chosen relatively large to reduce the effect of the parasitic capacitance on N_1, the power dissipated by the inverter to charge and discharge the bottom plate parasitic capacitance C_{P1} of C_1 might need to be considered. Assuming that C_{P1} is $\alpha\%$ of C_1 and the duty cycle of the HPS block is $\beta\%$, the power dissipated by the inverter can be expressed as:

$$P_{INV} = \frac{1}{2}\alpha\beta C_1 f_{clk} V_R^2 \tag{3.28}$$

3.4.8 Design guideline for performance and reliability

In light of the analyses conducted so far, we can conclude the following design guidelines in terms of performance and reliability for proper design of the HPS:

1. Since the top plate of C_1 will be exposed to high voltage levels, it is necessary to configure the clock logic so that during idle cases the bottom plate of C_1 is kept at V_R. This will reduce oxide stress of C_1 and improve device lifetime.
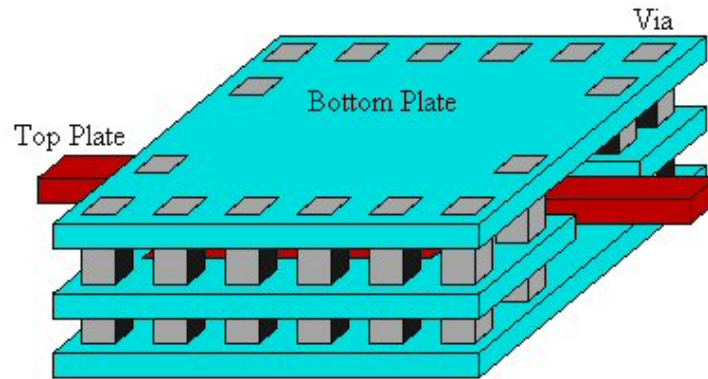
Figure 3.18. Suggested Layout for the Capacitor C_1

2. Determine minimum switch size that provides required on resistance that will allow total charge transfer at the end of each phase for a given system clock frequency, reference voltage and supply voltage (if different than the reference voltage) levels.

3. Great care should be given to the layout of C_1. To minimize parasitic capacitance associated to top plate, the bottom plate should be laid out like a rectangular prism covering the top plate. Suggested layout for C_1 is shown in Fig. 3.18.

4. Check using simple layout, process limits for minimum parasitic capacitance on node N_1 and determine the value of C_1 for targeted resolution. Iterate with 2 if necessary.

5. Trade settling time with the filter bandwidth. For better noise immunity, choose small C_1/C_2 ratio if long settling time is acceptable.

6. Make sure inverter driving the bottom plate is strong enough for C_1.

7. Output node N_2 is high impedance. Shielding is necessary to prevent any noise coupling.

8. Choose the proper output sampling phase to reduce the total output error.

3.4.9 Simulation results

In this sub-section a collection of simulation results showing the behavior of the HPS will be presented. The reference voltage V_R is chosen at 2.75V for all these simulations. System clock frequency is set to 2MHz.

Fig. 3.19 shows the transient behavior of HPS. During this simulation input signal is kept initially at 5.5V and changed to 2.751V at 32 μs. Markers M_1 and M_2 show the ideal output levels. Exponential convergence as predicted by 3.21 is apparent. The negative glitch at the beginning of the simulation is due to the following fact: Initially bottom plate of C_1 is held at V_R and top plate is at 0V. Pulling down bottom plate to ground drives top plate
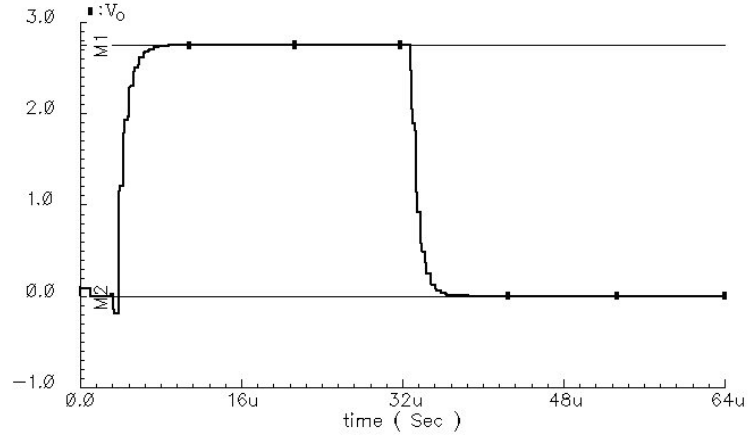
Figure 3.19. Transient Simulation of HPS (Input signal changes from 5.5V to 2.751V at 32μs)

N_1 to negative voltage levels. Pushing N_1 to negative voltage level turns on the parasitic body diodes of the switch transistors S_1 and S_2 to drain the negative charge stored on C_1. With subsequent cycles, through the charging of C_1 with the input signal, HPS recovers and settles to its final value.

This behavior is more apparent in the simulation result shown in Fig. 3.20. In this second simulation figure, ideal transfer function and HPS output is plotted together for different input signal levels. The error signal defined as the difference between the ideal transfer function and the output signal is given in Fig. 3.21. The effect of sampling at different phases, i.e. t_1 or t_6, is apparent in this figure. While sampling the output at t_1 results around 1.3mV absolute error, sampling the output at t_6 results less than 600 μV absolute error. For the remaining of the simulation results, output error refers to the error of the output signal sampled at t_6.

The variation of the error signal with respect to input voltage is shown in Fig. 3.22. This error signal is extracted from the output of the ADC's input stage output. Extra circuitry within the input stage that compares the input signal with the reference voltage and connects the input signal directly to the output or enables the HPS blocks according to the comparison is not shown in Fig. 3.13. Because of the aforementioned circuitry, the error voltage is zero for the input signal levels below the reference voltage, i.e. 2.75V. The variation of the error can be attributed to the variation of C_P, as described in (3.14). The largest capacitance variation (or equivalently largest error) occurs for the input signal levels equal to V_R for which the voltage across C_P changes between V_R and 0V. The smallest capacitance variation (or equivalently smallest error) occurs for full-scale input levels for which the voltage across C_P changes between $2V_R$ and V_R. Fig. 3.23 and Fig. 3.24 show the variation of the error signal with respect to input signal at different process corner within
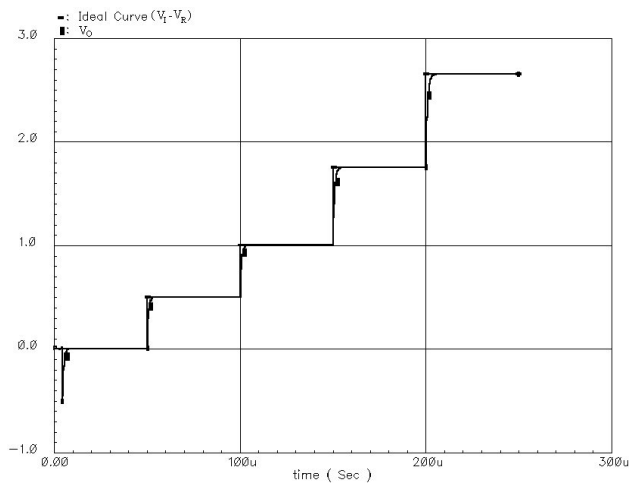
Figure 3.20. Transient Simulation Result Showing Ideal Output together with HPS Output For Different Input Voltages
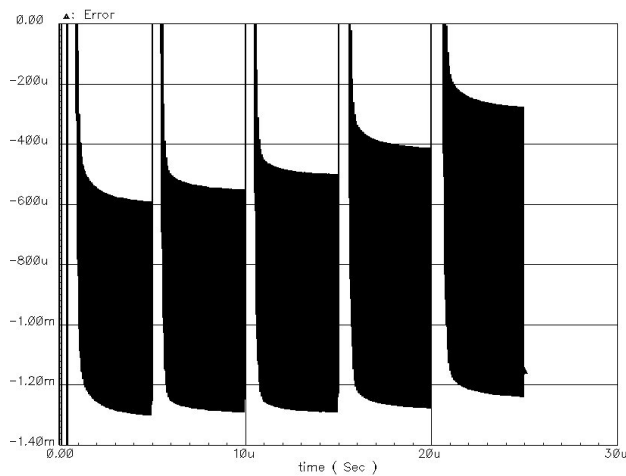
Figure 3.21. Error signal at the output

temperature range -50 to 150 degree C.

The ACS[12] simulation result suggests that designed HPS adds around 600 μV systematic error.

3.5   10-bit Successive-Approximation Register Analog to Digital Converter

Since the output of the first stage is bounded in between the supply rails, the second stage of the sub-ranging ADC is implemented using traditional SAR ADC architecture. Implemented 10 bit SAR converter schematic is given in Fig. 3.25. Charge redistribution converter is realized with 5 by 5 segmented capacitor matrix [76]. The advantages of the coupled capacitor

[12]TI proprietary statistical process corner simulation tool.
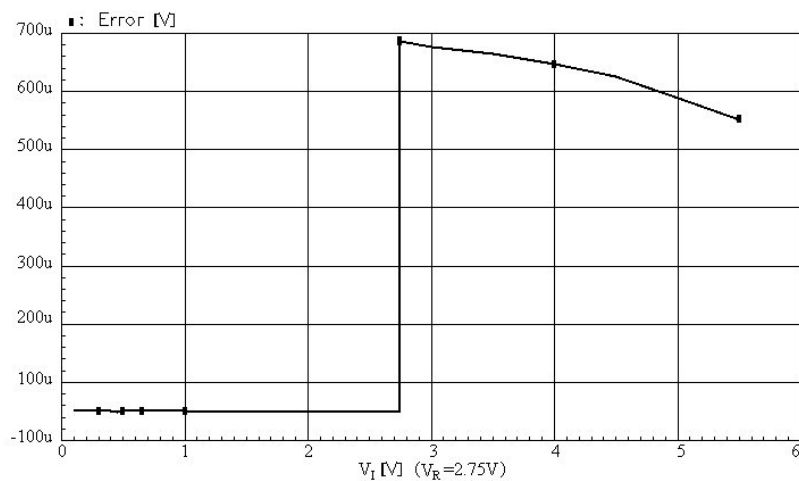
Figure 3.22. Variation of the Error Signal with respect to Input Signal

array realization over the traditional fully parallel realization[13] are :

1. smaller capacitor matrix area,

2. smaller number of unit capacitor within the matrix, $(2\sqrt{2^N} + 1)$ unit capacitor instead of 2^N,

3. better unit capacitor matching, therefore smaller unit capacitor size,

4. smaller capacitive input load.

The down side of the segmented realization is that:

1. high impedance node V_{HZ}

2. complex capacitor matrix layout

The layout of the capacitor array is the most critical design step of the SAR ADC converter. It ultimately determines the linearity performance of the converter. During the layout special care should be given to minimize the parasitic capacitance between the high impedance node V_{HZ} and the ground because this parasitic capacitance creates non-linearity. The parasitic capacitance loading the node V_{IM} yields to a small gain error, therefore its minimization is not very critical. The capacitor array is build from a unit capacitor of 158.5 fF.

The switches shorting the input terminals of the comparator during the sampling phase are both realized with NMOS transistors. The rational behind this selection is that during the transition from the sampling phase to evaluation phase, large spikes might occur

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[13]shown in Fig. 3.3
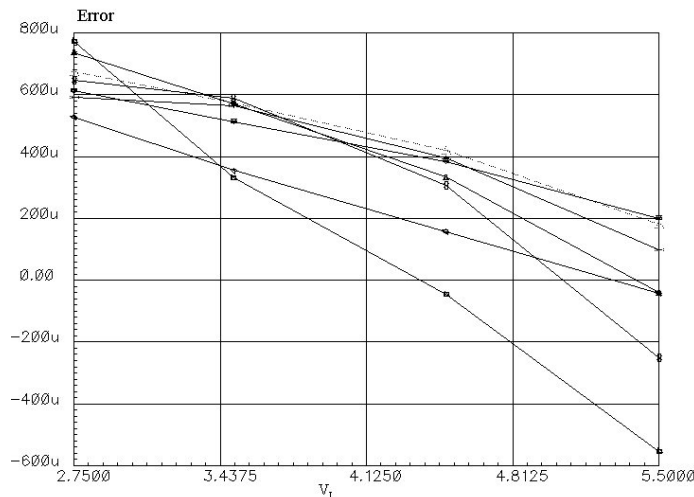
Figure 3.23. Error Signal with respect to Input Signal at Different Process Corner within temperature range -50 to 150 degree C.

on node V_{IM} due to the initialization of the SAR register bits. If a PMOS transistor is connected to that node[14], the charge stored on the capacitor matrix would leak to the power supply through its parasitic body diode that is forward biased during the spikes. Obviously, this would degrade the accuracy of the converter. In summary, those switches should be realized with NMOS transistors and of course, it is also important to chose proper bias voltage level such that not only the next block, i.e. the comparator, is properly biased but also the NMOS switches can adequately connect the bias voltage to the nodes V_{IM} and V_{IP} during the sampling phase.

At the end of the sampling phase, when the NMOS switches turned off, the channel charges of these two switches are injected to the high-impedance input terminals of the comparator, i.e. nodes V_{IM} and V_{IP}. To match the voltage shift due to the charge injection on both input terminals the capacitive load on the negative terminal is replicated at the positive terminal. This approach, although it is very inefficient in terms of silicon area, improves greatly the accuracy of the comparator, hence the accuracy of the conversion.

The gate level schematic of the SAR logic will not be presented here for the sake of simplicity. The logic implements the conversion process flow, the algorithm shown in Fig. 3.2. together with some test modes. Implemented SAR converter has two distinct differences compared to traditional segmented SAR ADC implementations:

1. The coupling capacitor is unity (integer)[76, 77],

2. Most significant 4 bit of the converter is realized with thermometric decoding[15].

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[14]As it would be if the switches are realized using transmission gates.

[15]It is not shown in Fig. 3.25
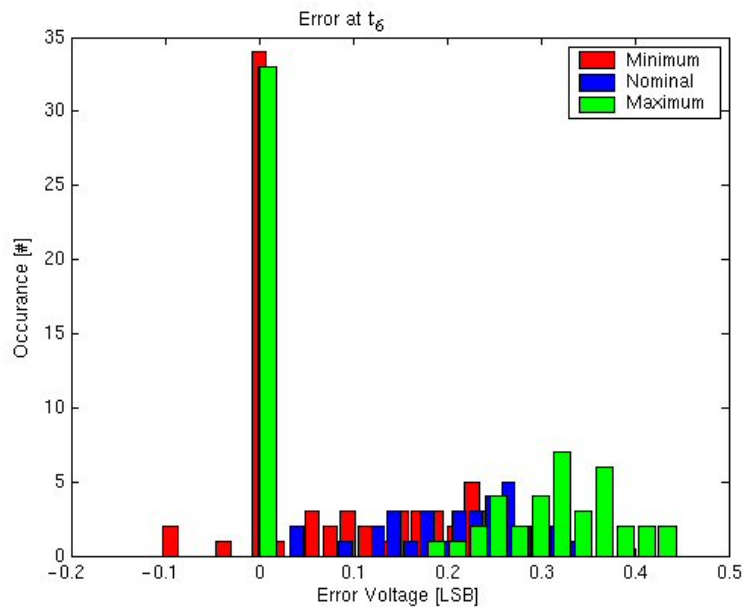
Figure 3.24. ACS simulation showing the error distribution at different Process Corner within temperature range -50 to 150 degree C.

3.5.1 Coupling Capacitor and the Transfer function

In order to obtain ideal ADC transfer function, traditional segmented SAR converter topology contains an extra capacitor within the LSB bit segment to adjust the offset. Furthermore, the ideal ADC transfer function requires that the value of the coupling capacitor should be chosen equal to $N/(N-1)C_U$ where N is the number of unit capacitor within the LSB segment. Therefore, the coupling capacitor is not integer multiple of the unit capacitor. For example, the value of the coupling capacitor for the current implementation would be equal to $32/31C_U$. The layout of the coupling capacitor[16] is a very serious design burden . It mars the regularity of the capacity matrix, which eventually yields to poor capacitor matching and therefore linearity error.

The topology shown in Fig. 3.25 does not contain an offset compensation capacitor and the coupling capacitor is chosen equal to the unit capacitor. This modification inserts a systematic 0.5 LSB offset to the ADC transfer function, as shown in Fig. 3.26. This is a very small price to pay for resulting linearity improvement.

Fig. 3.27 shows the equivalent capacitor circuit of the 5 by 5 segmented capacitor matrix. The total charge on node V_{IM} is equal to the charge stored on the C_{MSB} consisting 31 unit capacitor summed with the charge stored on the serial equivalent of the coupling capacitor and C_{LSB}, which consist of 1 and 31 unit capacitors, respectively. This way, each step at the LSB capacitor array is equivalent to $1/32^{nd}$ of a step in the MSB capacitor array.

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[16]or rather placing it within the matrix
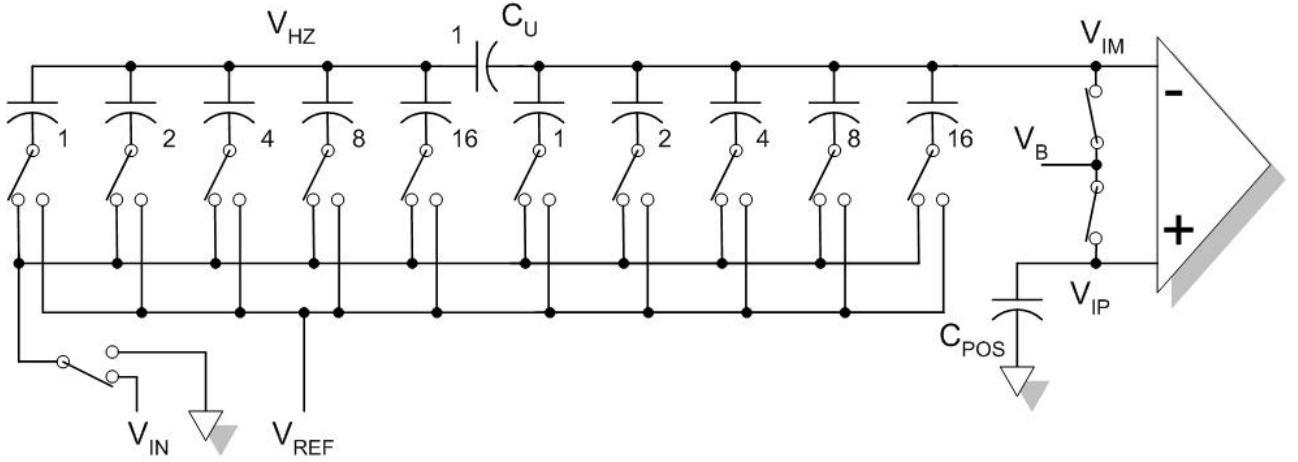
Figure 3.25. 10 bit 5 by 5 segmented Charge Redistribution SAR ADC
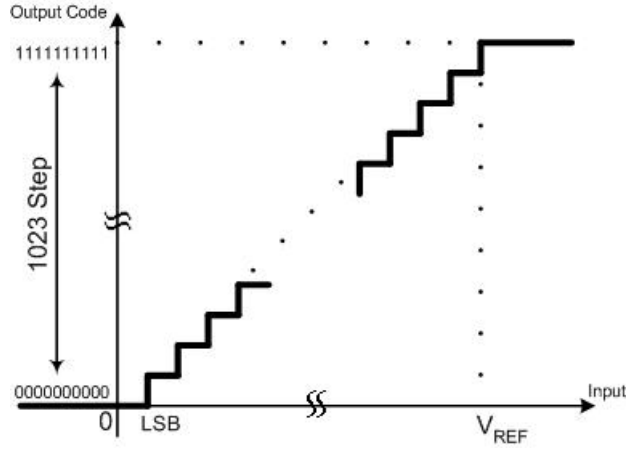
Figure 3.26. Transfer Function of the 10 bit SAR ADC

It is possible to express the resolution of the converter by reflecting the MSB bits back to the LSB array.

$$resolution = \underbrace{32 \times 31 \ C_U}_{MSB \ Array} + \underbrace{31 \ C_U}_{LSB \ Array} = 1023 \ C_U \tag{3.29}$$

Therefore, accordingly, the LSB level of the presented 10 bit SAR ADC can be expressed as

$$LSB = \frac{V_{REF}}{2^N - 1} = \frac{V_{REF}}{1023} \tag{3.30}$$

Finally, the transfer function of the implemented 10 bit SAR ADC can be expressed as

$$OUT = \text{int} \left(\frac{V_{IN}}{LSB} \right) \tag{3.31}$$
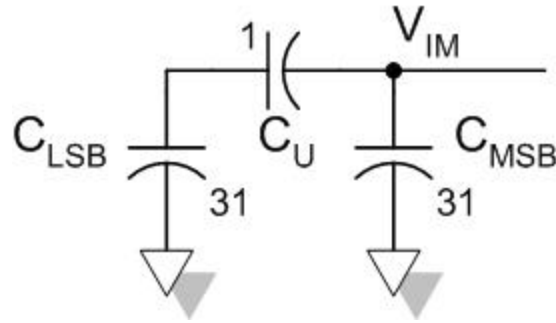
Figure 3.27. Equivalent circuit of the 5 by 5 Segmented Capacitor Matrix
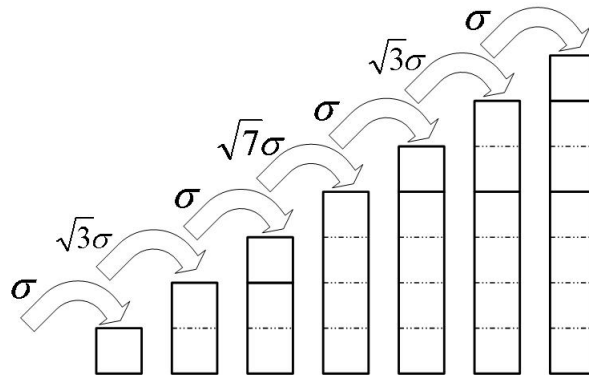
Figure 3.28. Random Variation Binary Capacitor Array

3.5.2 Thermometric Decoding

Another important design detail adopted within the developed 10 bit SAR ADC is that the most significant 4 bits of the converter is implemented with thermometric decoding. Fig. 3.28 and Fig. 3.29 compare the DNL standard variations of binary capacitor array and thermometric capacitor array. The binary capacitor array consists of binary weighted capacitors whereas thermometric capacitor array consists of unit capacitors. As it is clear from Fig. 3.28 worst case DNL variation of the binary array occurs for MSB code. This is due to fact that none of the MSB capacitors are present within the previous code. The thermometric capacitor array solves this problem and consequently reduces the DNL variation by adding one by one the unit capacitors, as illustrated in Fig. 3.29. Therefore, each code uses all the capacitors that the preceding one uses. Both architectures contain 7 unit capacitors. Binary capacitor array has 3 elements whereas thermometric capacitor array has 7 elements. Consequently thermometric array requires decoding and routing but the benefit is that all codes have the same DNL and it is much smaller than binary capacitor array's counterpart.
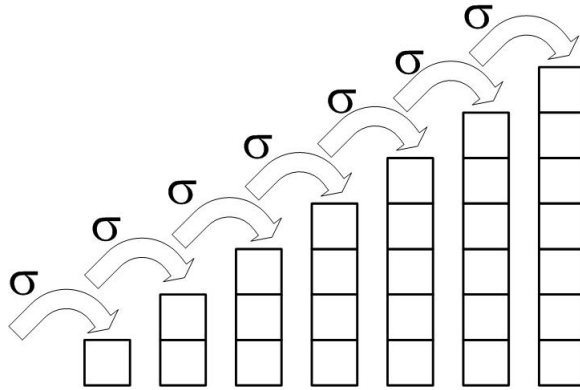
Figure 3.29. Random Variation Thermometric Capacitor Array
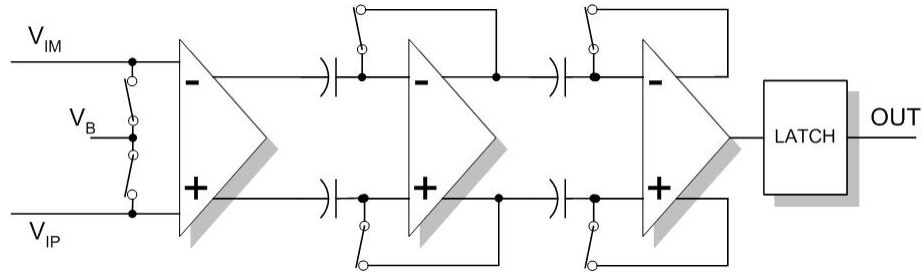
Figure 3.30. Block Diagram of the Comparator

3.5.3 Comparator

The comparator used within the SAR ADC is standard zero offset clocked comparator. It consists of capacitively coupled three amplifier stage. The offset of the amplifiers are stored on the capacitors during the sampling phase so that its effect can be canceled during the comparison phase. As a result, the input offset is limited by the switch charge injection mismatch. Adopted fully differential comparator structure improves the resilience of the comparator to the common mode noise injected from the supply terminals and the bulk of the chip. The block diagram of the whole comparator is shown in Fig. 3.30 [78, 79]. The simplified schematic of the amplifiers is given in Fig. 3.31.

Finally, the comparator within the first stage of the 11 bit Sub-Ranging ADC is also implemented with exactly same structure.
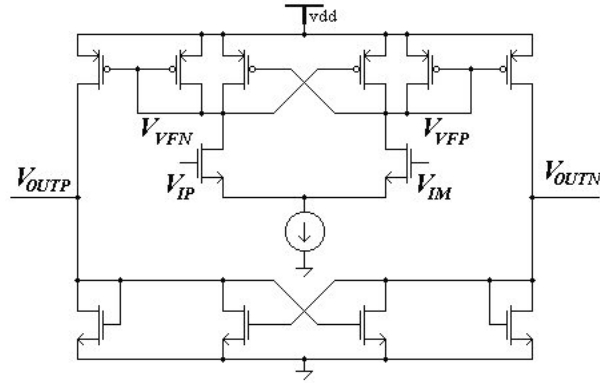
Figure 3.31. Schematic of the Comparator Amplifiers

3.6   11-bit Sub-Ranging Analog to Digital Converter

3.6.1   Connecting the stages

The first and the second stage schematics of the 11-bit sub-ranging ADC are shown in Fig. 3.32 together with the input stage clock signals for an input signal greater than the reference voltage. Although it is not explicitly shown in the figure, to improve linearity performance of the overall converter, 4 MSB bits of 10 bit SAR ADC's charge redistribution DAC are driven by thermometric decoder as explained in section 3.5.2. Since, the transfer function of each one of the two stages is already known, it is possible to expressed the overall transfer function of the converter obtained by cascading them. Therefore, the transfer function of the 11 bit Sub-Ranging ADC is

$$Out = \begin{cases} \text{int}\left(\frac{V_{IN}}{LSB}\right) & \text{if } V_{IN} \leq V_{REF} \\ 2^{N-1} + \text{int}\left(\frac{V_{IN} - V_{REF}}{LSB}\right) & \text{if } V_{IN} > V_{REF} \end{cases} \qquad (3.32)$$

where LSB is defined in (3.30) and N is the number of bits of the converter, i.e. 11. If this transfer function is plotted with respect to the input signal, a serious problem reveals itself. The converter has a missing code for input signal level equal to the reference voltage V_{REF}.

The reason of this error is the following: The 10 bit SAR ADC reaches its maximum code, i.e. 1111111111, when the input signal reaches the reference voltage. This is simply due to the systematic 0·5 LSB offset error. The first stage, on the other hand, tries to detect whether the input signal has reached to the reference voltage to set the MSB bit, i.e. 11th bit, to logic 1 and to subtract the reference voltage from the input signal. Therefore, the output code's transition from 1111111110 to the next code is not 1111111111 but to 1000000000.

To show this behavior, equation (3.32) is plotted with respect to the input signal and
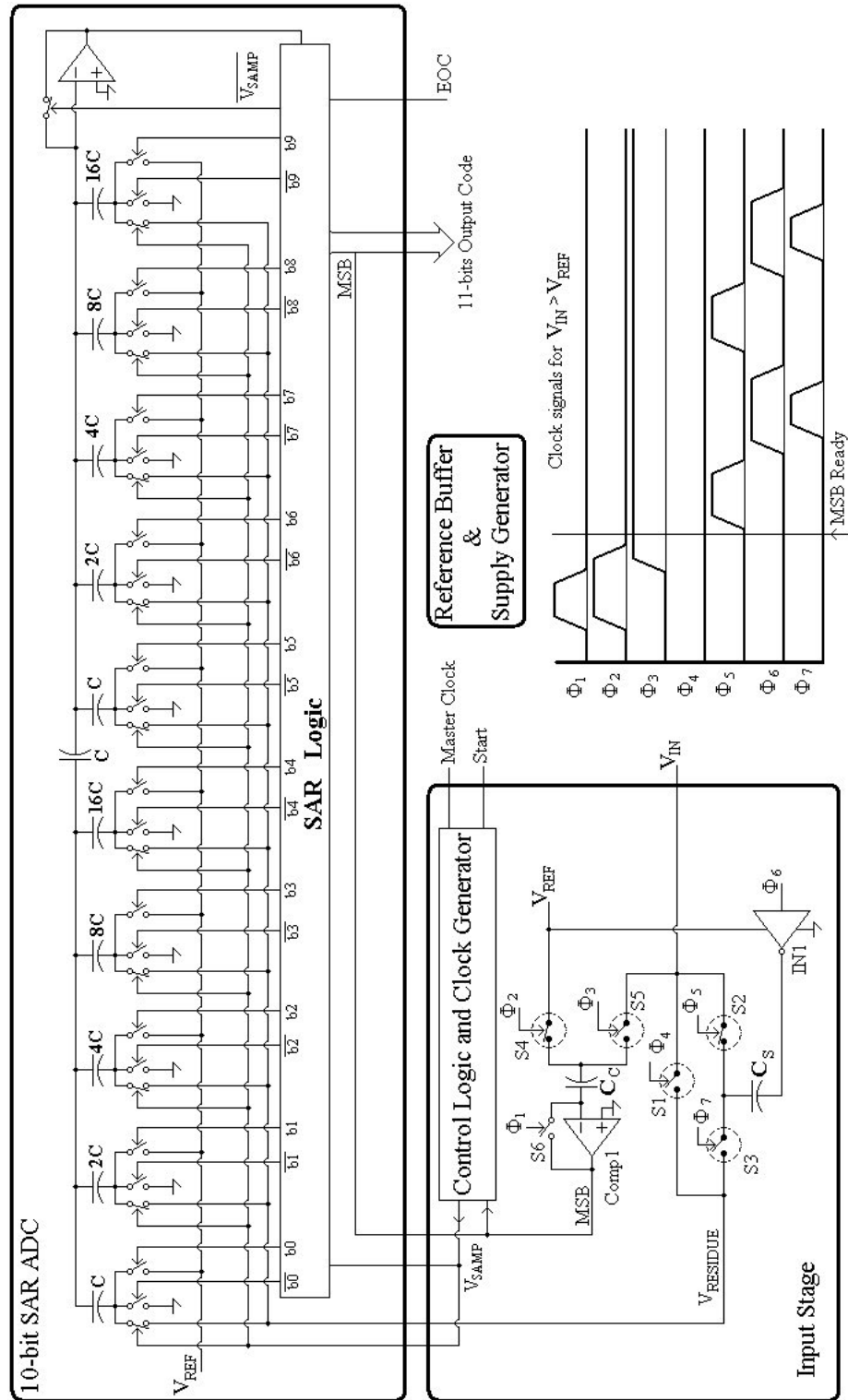
Figure 3.32. 11 bit Sub-Ranging ADC First and Second Stage Schematic with clock signals for $V_{IN} > V_{REF}$
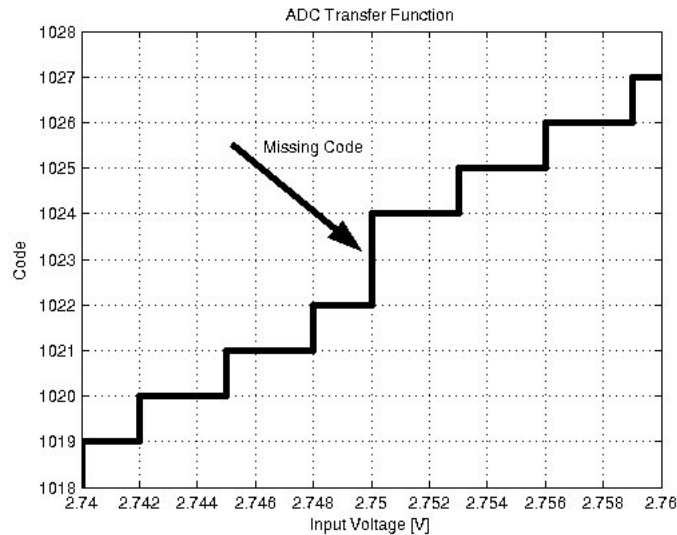
Figure 3.33. Missing Code due to the Systematic 0.5 LSB offset of the 10 bit SAR

zoomed to the transition region in Fig. 3.33 and resulting DNL of the converter is plotted in Fig. 3.34.

3.6.2 Removing the Missing Code

It is apparent from the description above that this problem is due to the fact that the first stage override the last code of the SAR ADC because of its comparison threshold level, i.e. reference voltage V_{REF}. Since, this error is equivalent to shift to upper half of the transfer function 1 LSB up, an easy and cheap solution to fix this problem is to subtract 1 LSB from the output code when the most significant bit is logic 1. This is exactly what is implemented, as it is clear from Fig. 3.5. Therefore, the transfer function of the overall converter system at the output of the adder can be expressed as:

$$Out = \begin{cases} \text{int}\left(\frac{V_{IN}}{LSB}\right) & \text{if } V_{IN} \leq V_{REF} \\ 2^{N-1} - 1 + \text{int}\left(\frac{V_{IN} - V_{REF}}{LSB}\right) & \text{if } V_{IN} > V_{REF} \end{cases} \tag{3.33}$$

As a consequence of the subtraction operation at the output of the converter, obtainable number of code of the converter is 2047 instead of 2048. In other word, the last code of an ideal 11 bit ADC, i.e. 11111111111, is not obtainable. This is a very small price to pay to solve the missing code problem.

3.6.3 11 bits ADC Layout

The layout of the ADC system is shown in Fig. 3.35. The total silicon area is 560 by 560 μm^2. The converter system, in addition to the described sub-blocks, contains high-voltage
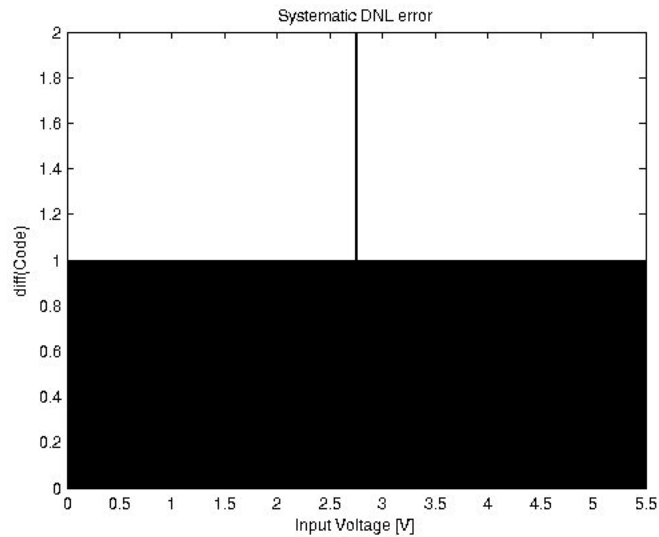
Figure 3.34. Systematic DNL error due to the Missing Code

digital interface circuit to communicate with other sections of the power management IC having different supply voltage level, OVST test[17] mode circuitry, digital control blocks controlling conversion process flow and test modes, clock signal generator and buffers. The implementation of these blocks are pretty strait-forward, therefore the details of these blocks will not be presented for the sake of simplicity.

The most critical signals within the system are the reference signals, i.e. V_{REF} and reference ground. These signals are properly shielded in order to prevent noise injection. Since the output of the passive subtractor circuit is high-impedance for input signal levels exceeding the supply voltage, this node is also properly shielded.

The digital and analog supply signals are kelvin connected at the bonding pad in order to reduce required power supply pad and to provide some isolation in between digital and analog circuit domains. Since the comparators of the ADC are fully differential, they are resilient to the common mode noise signals infiltrating through the supply line.

In order to characterize high-voltage bootstrapped switch circuit, a separate group of HVB switch is also included to the layout. Those switches are accessible from within embedded test modes.

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[17]Over Voltage Stress Test for oxide reliability
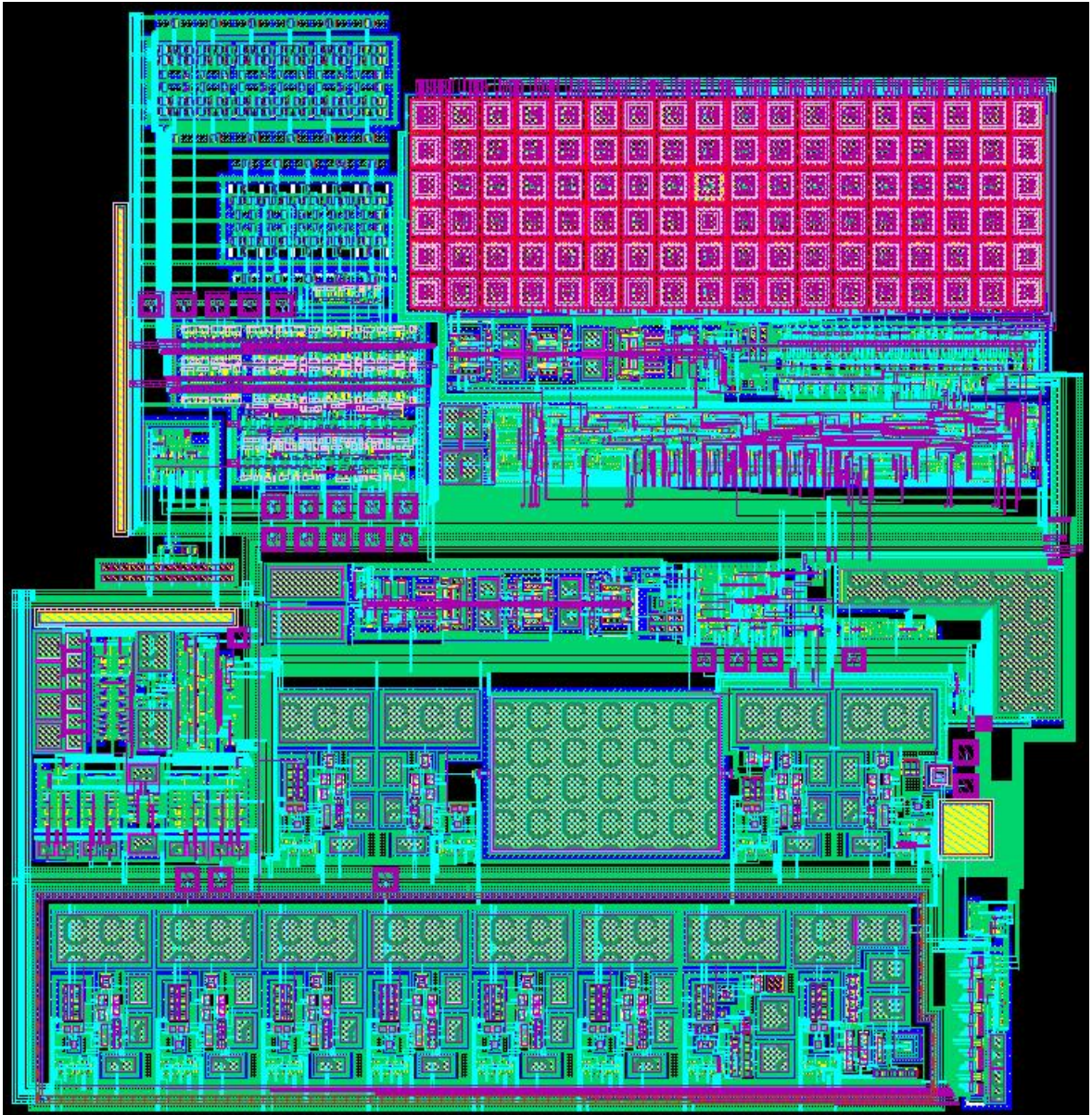
Figure 3.35. Layout of the 11 bit Sub-Ranging ADC

CHAPTER 4

SYMBOLIC SMALL SIGNAL ANALYZER
SSA Tool

4.1 Introduction

In this chapter, SSA Tool, a general purpose circuit analyzer that calculates small signal transfer function of any given circuit and/or system symbolically, will be presented. Basically, SSA Tool extracts symbolic node equations from a given circuit description and solves the symbolic linear node equation system. The chapter is organized to present different modules of the tool and to provides examples to prove its efficiency.

The tool is built upon preexisting symbolic solver, i.e. Matlab symbolic toolbox, and graphical circuit capture tools, i.e. Cadence DFII Virtuoso and Matlab Simulink. Therefore, the aim of the tool is not the development of a generic symbolic equation system solver or the development of generic symbolic simplification algorithms, but rather to create a designer friendly circuit/system design and analysis environment using existing tools and integrate the environment to the regular IC design flow. This chapter should be treated as the operation manual and general description of the tool. The chapter is organized as follows:

The tool's process flow and the interaction in between its modules will be analyzed in section 4.2. Special effort spends on integrating the SSA tool with standard IC design softwares, i.e. Cadence DFII design environment and Matlab. The tool is developed using Matlab symbolic toolbox and the interface software developed within Cadence DFII to export the data to Matlab. The tool uses Cadence Virtuoso Schematic capture tool as main interface to enter circuit description. Alternatively, it is also possible to use Matlab Simulink interface or custom circuit netlist text file to describe the circuit to the tool. The basics of the custom SSA tool netlist file, together with the design flow starting from Cadence Virtuoso Schematic or Matlab Simulink Schematic, will be explained in section 4.3.

Matlab symbolic toolbox solves the symbolic linear equation system and simplify the results. The result simplification algorithms of the tool are based on a priori knowledge of the analyzed circuit/system and they are implemented in extension modules, such as $\Sigma\Delta$ modulator analysis module. The efficiency of such approach will be exemplified.

The tool can be used for any problem involving solving linear equation system. Therefore, it is possible to obtain small signal transfer function gain and phase expressions, gain

bandwidth product, phase margin, gain margin, DC gain, common mode rejection ratio, power supply rejection ration, node impedance, noise analysis, signal-flow-graph analysis or for $\Sigma\Delta$ modulators, signal transfer function, noise transfer function, internal node dynamic range, in band noise power, stability analysis, sensitivity analysis, analyzing SNR degradation due to circuit non-idealities (DC Gain, GBW, Mismatch, etc) using SSA Tool.

The SSA tool can also calculate distortion and intermodulation distortion transfer functions of arbitrary circuit and systems provided that the circuit netlist contains appropriate nonlinearity parameter set. The basics of the nonlinear analysis together with analysis examples will be provided in sections 4.9 and chapter 6, respectively. The tool can also be used to calculate complex nonlinear performance parameters, such as IP2, IP3, mixer conversion gain, etc...

The tool also provides specialized extension modules for circuit/system design and analyze. Especially, $\Sigma\Delta$ Modulator analysis module proves to be an indispensable design tool during the development, analysis and optimization of $\Sigma\Delta$ modulator architectures. These modules also will be presented later in the chapter.

Known problems of the tool can be found in appendix F.

4.2   Process Flow, Control And the Outputs

The process flow of the SSA Tool is shown in Fig. 4.1. The whole tool can be partitioned to three separate modules, i.e. input stage, circuit solver and post processing blocks.

The input stage is responsible for the netlist translations. The output of this module is the circuit description in custom SSA tool netlist format.

The circuit solver module extracts the symbolic node equations from the netlist and solves the linear equation system. This module also modify the original circuit netlist and solves the new equation system to calculate harmonic and intermodulation distortion transfer functions.

Finally, the post processing modules manipulate and simplify the symbolic circuit responses. There are several different post-processing blocks. We will review them in detail later in the chapter

This whole processing flow is orchestrated by the matlab function **ssatool()** and its nomenclature is

[ssacirsol,ssacomp,ssasade,ssaimp,ssaup]=ssatool(simdirname,cellname,ssaoption)

The definitions of the input and output arguments are:

simdirname: This is a string variable containing the name of the directory where the circuit description file is saved. For circuits described using SSATool netlist file or simulink .mdl
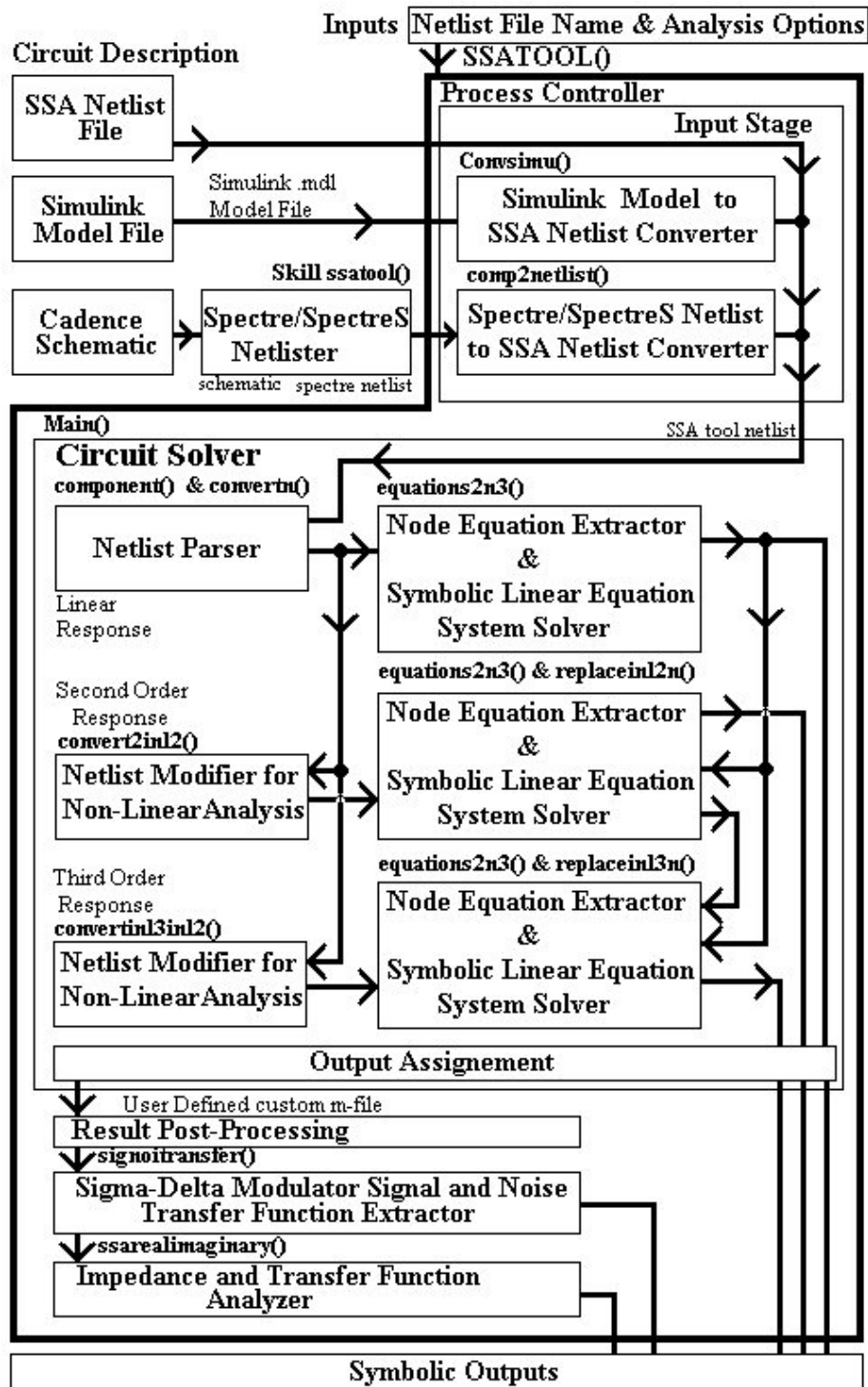
Figure 4.1. Process flow Diagram of SSA Tool

file, this is the name of the directory where the circuit description file is actually saved; for cadence spectre(S) netlist interface, this is the name of the directory where spectre(S) simulation run directory of the design is saved.

cellname: This is a string variable containing the name of the design. For custom SSA Tool netlist file, it is a Matlab .m file; for simulink model, it is an .mdl file; for cadence spectre(S) interface, it is the name of the simulation run directory.

ssaoption: This is a string variable that sets, changes the options of the tool that in turn modify the analysis process flow. Ssaoption string should be in the form of

$$',option\_name=option\_value,...,'$$

Each option variable should be separated from each other with a comma sign. The string should start and end with comma sign. If ssaoption input is not provided, default option values are assumed.

Executing the command **ssatool** from the Matlab command window displays the tool main help. Executing the command **ssatool(helpnum)** displays the appropriate help of the SSA Tool sub-modules. The names of the possible option variables, their default values and descriptions are given in Table 4.1. Please refer to ssahelpnum in the option list to find out the correspondence between the numbers and sub-functions.

The option variables related to post-processing module settings can also be changed or set through SSA Tool netlist file or Cadence DFII Virtuoso schematic.

The descriptions of the output variables are

ssacirsol: This structure variable contains the circuit solution. Basically, this variable is the output of the circuit solver, i.e. ssamain(). It has the following fields:

1. ssacirsol.eq$_{XY}$: These fields contains the symbolic circuit responses at corresponding frequencies[1]. This is a two column matrix. First column of the variable contains the circuit node names and voltage source currents. Second column of the variable contains small signal analysis results. Since, the linear analysis is always performed by the tool, the linear analysis result variable, i.e. ssacirsol.eq11, is always present in the matlab work space. The remaining fields assigned if the circuit response at corresponding frequency is calculated.

2. ssacirsol.TFN : This is the generic form of how every single one of the calculated transfer functions appear in the Matlab work space at the end of the analysis. The acronym TFN stands for transfer function name and it is replaced by the transfer function name declared within the Signal Transfer Function definition xtf . This is a symbolic variable

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[1]The suffix XY represents operation frequency. The possible values of the operation frequency are summarized in Table 4.2.

Table 4.1. SSA Tool Option variable names, their default values and descriptions.

Option Name	Default Value	Description
ssainputfiletype	spectres	In case, there is more than one file that can be loaded for a given simdirectory and cellname input pair, this option can be used as selection switch. Possible switch values are 'spectres', 'spectre', 'matlab' and 'textbased'.
ssaoutfilename	SSAToolnetlist	This option can be used to set the intermediate text based SSA Tool netlist name for Cadence and Simulink design flow. By default, tool creates intermediate netlist file with the name SSAToolnetlist.m
ssamatlabstability	off	This is a switch to enable Matlab Simulink model netlister for Sigma-Delta modulator stability analysis. Possible values are 'on' and 'off'.
ssasigmadeltasimp	off	This is a switch to enable the tool to extract the signal and noise transfer functions of sigma-delta modulator output. Possible values are 'on' and 'off'.
ssasdoutvarname	none	This option is used to declare the name of the symbolic sigma-delta output variable for transfer function extraction. It is only necessary when ssasigmadeltasimp switch turned on.
ssasdnonana	off	This switch is used to configure the tool for nonlinear signal extraction from the output signal of the sigma-delta modulator. If the switch is turned on, the tool assumes that the modulator output is obtained through non-linearity analysis. Possible values are 'on' and 'off'.
ssapostprocesssw	off	This switch is used to run post processing matlab function. Post processing code is run after the circuit solution is calculated. Possible values are 'on' and 'off'.
ssapostprocessmfilename	none	This option contains the name of the Matlab file that will be used to post process the circuit results. It should be a command line executable matlab file. This file can contain any matlab function or any post processing code.
ssaimpon	off	This option enables the impedance/ admittance/ transfer function extraction function. Possible values are 'on' and 'off'.
ssaimpvar	none	This option used to change the variable name that will be processed by the impedance or transfer function analyzer function.
ssaimpadmit	impedance	Because of the fact that the circuit solution is in the form of node voltages, it is only possible to extract the symbolic impedance function from the symbolic circuit solver. This option allows converting impedance function to admittance function, i.e. Y=1/Z. Possible values are 'impedance' and 'admittance'.
ssahelp	off	This switch is used to show the help texts. Possible values are 'on' and 'off'.
ssahelpnum	1	This switch is used to view the help text of the different matlab function within the SSA tool. Possible values and attached help texts are: 1 ssatool(), 2 main(), 3 comp2netlist(), 4 convsimu(), 5 signoitransfer(), 6 ssarealimaginary
ssadefaultoptionlist	off	This switch is used to see default options as stored in the file ssatooldefaultoptionfile. Possible values are 'on' and 'off'.
ssadefaultoptionsave	off	This switch is used to save current options to the file ssatoolcustomoptionfile. Possible values are 'on' and 'off'.
ssadefaultoptionload	off	This switch is used to load options from the file ssatoolcustomoptionfile.mat. Possible values are 'on' and 'off'.

and it contains calculated signal transfer function. Please refer to section 4.3.2 for rules regarding proper selection of transfer function variable name.

3. ssacirsol.TC : This field contains device terminal current expressions. It exist in the work space only if the terminal current calculation module is enabled.

4. ssacirsol.ssahelp : This field contains the information regarding to the content of ssacirsol structure fields.

5. ssacirsol.update : This field contains the last update date of the function ssamain().

ssacomp : This structure variable contains the input signal source, quantizer and impedance analysis related component parameters.

ssasade : This structure variable contains the analysis results obtained from $\Sigma\Delta$ Modulator analysis module. The list of possible fields within the variable will be given in section 4.6.

ssaimp : This structure variable contains the analysis results obtained from transfer function analysis module. The list of possible fields within the variable will be given in section 4.7.

ssaup : This field contains the last update dates of various functions within the tool.

4.3   Input Stage and Circuit Description (Input)

Input stage controls the existence of the circuit description file, execute netlist conversion codes, if it is necessary to convert Matlab simulink model file or Cadence spectre(S) netlist to custom SSA Tool netlist. In this section, we will concentrate on different possible design flows to describe the circuits to the SSA tool.

There are three different ways to describe a circuit to SSA Tool:

1. Text based circuit netlist file (similar to Spice circuit netlist input).

2. Matlab Simulink model file that contains solely the components provided by custom simulink library named *ssalibrary*.

3. Cadence DFII Virtuoso schematic that contains solely the components provided by custom Cadence design library named *SSALIB*.

The SSA Tool symbolic solver function ssamain() process only text based circuit netlist input. Therefore, interface established with Matlab Simulink model and Cadence Virtuoso schematic by simply converting the netlist obtained from these two schematic capture tool to the text based SSA Tool netlist.

4.3.1 The basics of the text based SSA Tool netlist file

SSA Tool expects that the extension of the netlist file is '.m'. A valid netlist line (description) is defined within parentheses, i.e. {}. Any line that is not enclosed within the parentheses is considered as a comment line and therefore ignored during the netlisting. The netlister of the SSA Tool is basically a text processor. Therefore for correct interpretation of the netlist, number of left parentheses '{' have to be equal to number of right parentheses, '}'. To remove a line from the netlist, it is enough to delete parentheses enclosing the component definition.

A netlist line has the following general format:

{definition, parameters}

Definition section of the netlist line contains an acronym related to the content nature[2] of the line and **parameter** section contains the values of the required parameters related to that specific definition. In case of multiple parameters, every parameter is separated from each other using comma sign ','. For the definitions requiring more than one parameter, it is required to put an extra comma at the end of the line, before the right parenthesis, to comply with the text processor requirements.

With respect to their functionality, there are three different definition class:

1. Ground node and Analysis mode definitions

2. Signal Transfer Function definitions and Schematic option definitions

3. Component definitions

Each one of these classes has their own acronym, parameters and specific syntax. As pointed out above, since the netlister is just a text processor, the consistency of the netlist syntax with the netlister expectation is very important. Valid SSA Tool netlist definitions, their functionality and their syntaxes are given below[3]:

First class contains the definitions that affect the way the circuit solution is calculated. Ground nodes are considered as AC ground and replaced with zero during the small signal analysis. The syntax for ground node definition is:

{g,gr_n_name}

where g is ground node definition acronym and gr_n_name is the ground node name (vdd, gnd, etc..). To find the signal transfer function from the ground nodes to any another node, for power supply rejection ratio calculations for example, the ground node should be

---

[2]resistor, transistor, analysis type etc

[3]SSA Tool netlist definition syntaxes can also be found in the SSA Library data sheet, in appendix H, containing the information of the available Cadence and Simulink components.

separated from the circuit and a signal source should be connected in between. It is possible to declare multiple ground definition.

Example :{g,vdd}

Analysis mode definition is used to force the symbolic solver to calculate harmonic and intermodulation transfer functions of the circuit. Because of the fact that calculating higher order responses of a circuit is complex and computational intensive, harmonic and intermodulation response calculations are performed only if analysis mode command forces the solver to do so. If analysis mode definition is not present within the netlist, SSA Tool performs only linear small signal analysis. The syntaxes for analysis mode definition are:

{ana,analysis_type}

The parameter analysis_type can only have the following values:

1. second : For the calculation of the second order harmonic response

2. secondsimp : For the calculation of the second order simplified harmonic response.

3. third : For the calculation of the third order harmonic response

4. thirdsimp : For the calculation of the third order simplified harmonic response.

Example :{ana,thirdsimp}

Because of the fact that the symbolic expression simplification process creates heavy load resulting longer computation time, two extra switches are added to the definition to be able to skip the simplification phase. The acronym **ana** is included to the definition list for harmonic response calculation only. A more general definition is given below:

{anaim,analysis_enable}

The parameter analysis_enable is a sixteen bit number. Each one of these bit can be set to 0, 1 or 2. If a bit is set to 0, corresponding analysis mode is disabled. If it is set to 1, related analysis mode is enabled and finally, if the bit is set to 2, the analysis results are simplified. Table 4.2 summarizes bit allocation of the analysis_enable parameter. As it is obvious from the table, the intermodulation calculations are enabled through this definition. The linear analysis bit, i.e. 1st bit, is set default to 1; the default setting of all other analyses modes is 0.

Example :{anaim,1000200000000000}

Second class contains definition related to circuit solution manipulation. Signal Transfer Function definition is used to calculate custom transfer function expression. The syntax of the definition is:

{xtf,tf_name,denominator,numerator,option,}

Denominator and numerator expressions can be any complex mathematical expression containing independent symbolic variables, constants, functions and of course, node names

Table 4.2. Definition anaim bit allocation

Bit #	Analysis Mode & Frequency	Structure Suffixes	Discrete Time Variable and its Definition
1	w_1	eq11	z11, $\exp(jw_1T)$
2	w_2	eq12	z12, $\exp(jw_2T)$
3	$-w_1$	eq13	z13, $\exp(-jw_1T)$
4	$-w_2$	eq14	z14, $\exp(-jw_2T)$
5	$2w_1$	eq21	z21, $\exp(j2w_1T)$
6	$2w_2$	eq22	z22, $\exp(j2w_2T)$
7	$w_1 + w_2$	eq23	z23, $\exp(j(w_1 + w_2)T)$
8	$w_1 - w_2$	eq24	z24, $\exp(j(w_1 - w_2)T)$
9	$w_2 - w_1$	eq25	z25, $\exp(j(w_2 - w_1)T)$
10	$3w_1$	eq31	z31, $\exp(j3w_1T)$
11	$3w_2$	eq32	z32, $\exp(j3w_2T)$
12	$2w_1 + w_2$	eq33	z33, $\exp(j(2w_1 + w_2)T)$
13	$2w_1 - w_2$	eq34	z34, $\exp(j(2w_1 - w_2)T)$
14	$2w_2 + w_1$	eq35	z35, $\exp(j(2w_2 + w_1)T)$
15	$2w_2 - w_1$	eq36	z36, $\exp(j(2w_2 - w_1)T)$
16	Component terminal Current calculations (TC)		

and voltage source currents. Naming convention for hierarchical designs and voltage source currents will be explained in sections 4.3.4 and 4.3.2, respectively.

While evaluating the expressions, tool replaces the node names and voltage source currents within the expressions with their calculated values. The ratio of numerator to denominator is then assigned to the variable named tf_name. The parameter option is used to enable/disable simplification process at the end of transfer function evaluation phase. If the option parameter is chosen as **'simp'**, simplification phase is enabled.

Xtf definition allows also accessing circuit's higher order responses. Harmonic order of a variable is declared by adding corresponding suffix to the variable name. The valid suffixes are given in the third column of the Table 4.2. If there is no suffix or a different suffix is used, linear response is assumed. If there is a reference to uncalculated variable, tools lefts that variable as it is. Of course, to be able to access to a given harmonic response, the circuit solver should be configured to calculate that particular response.

The circuit netlist may have multiple **xtf** definitions.

Example :

Assume that the output terminal names of a fully differential amplifier are outp and outn. Then second order harmonic distortion can be calculated with the command

{xtf,HD2,outp_eq11-outn_eq11,outp_eq21-outn_eq21,simp,}

and third order harmonic distortion can be calculated with the command

{xtf,HD3,outp_eq11-outn_eq11,outp_eq31-outn_eq31,nosimp,}

Schematic option definition is used to redefine SSA Tool options within the circuit netlist to manipulate tool extension module variables. The syntax of the definition is:

{opt,option_name=option_value;}

SSA Tool options and corresponding valid option values are given in Table 4.1. Circuit netlist may have multiple **opt** definitions. The expression defined within the schematic option line is executed as a Matlab command. Therefore, this command can be used to execute any Matlab command to manipulate work space after the circuit response calculations[4]. The command execution order is exactly same as the order of appearance within the circuit netlist file.

Example:

{opt,ssasdsimp='on';}

Last definition class contains definitions related to the circuit components such as resistor, capacitor, etc... Component definition line has the following general format:

{definition,instance_name,terminal_list,parameter_list,}

Definition section contains the component acronyms, for example the acronym **cap** is used to declare capacitor. Instance name is the unique name of the declared component within the netlist. The Tool is not controlling whether the instance name is unique or not. Having multiple components sharing same instance name in a circuit netlist may yield to wrong circuit solution.

Terminal_list contains the list of the terminal node names. Node names within the list should be separated using comma sign, i.e. ','. The location of a specific node name within the terminal list, declares the connection of this node to the corresponding component terminal, exactly same as spice netlist. For example, the netlist line

{mos,I1,node1,node2,node3,node4,...,}

declares a MOSFET transistor with instance name I1 whose drain terminal is connected to node1, gate terminal is connected to node2, source terminal connected to node3 and finally bulk terminal is connected to node4. The node names within the terminal list are used to extract node equations. It is obvious that one and only one node can be connected to any given terminal of any component.

Parameter_list contains component specific parameters. Each parameter should be separated with a comma sign, i.e. ','. To comply with the requirement of the netlister text processor another comma sign should be added at the end of the parameter list before the right parenthesis. It is possible to define parameter with complex expression containing arithmetic operations, several different variables or functions. For example, the following netlist line

---

[4]A better way of doing this is using post-processing module. This module will be defined in section 4.5

{nondirenc,Inres1,bnode,enode,gm/beta,K2gm/beta,K3gm/beta,}
declares a non-linear resistor (more specifically, base-emitter resistance of a bipolar transistor) whose name is Inres1, its positive terminal is connected to the node named bnode, its negative terminal is connected to the node named enode, its linear conductance is the ratio of the parameters gm and beta, its second order nonlinearity coefficient[5] is K2gm/beta and finally its third order nonlinearity coefficient is K3gm/beta.

SSA Tool process node names, voltage source currents and parameter variables exactly the same way. Therefore using a node name within the parameters of a component renders this component voltage controlled[6]. Even though, this approach facilitates the declaration of voltage controlled components (for example, a transconductance amplifier can be declared as simple as {cur,Ivccs1,outp,outn,transcond*(inp-inn),}), great care should be taken while using this feature because it can result non-linear equation system which is unsolvable.

A complete list of the available components, their definition acronyms, terminal name list, parameter name list and their description can be found in appendix H. This data-sheet is prepared to describe the cells of Simulink and Cadence design libraries, but related SSA Tool netlist line definition is also included to the description of the library cells. Some of the component within the data sheet uses hierarchical design. Therefore, they do not have a SSA Tool netlist definition. Those models are only available with Cadence design flow.

SSA Tool allows the creation of custom component models. There are two ways to define custom model. First method involves creation of custom device specific m-file. The rules related to how to create specific custom component model m-file will be explained in detail later in section 4.8. The second method is to use hierarchical design in Cadence Virtuoso schematic capture tool together with spectreS netlister. This method will be reviewed again in section 4.8.

Sample SSA Tool netlists are included in sections 4.3.3 and 4.3.4.

4.3.2 Symbolic Variable Definitions and Restrictions

The symbolic expression used within parameter definitions can be any complex expression, containing multiple variable, node names, voltage source currents, arithmetic operation or even functions.

By default, all the variables are assumed to be positive real valued. If a given variable has different property, such as negative real, real, complex, corresponding suffix should be added to the variable name. Table 4.3 summarizes possible cases and corresponding suffixes.

There are three special variables that are introduced mainly for simplification purpose.

---

[5]The term non-linearity coefficient will be defined in section 4.9
[6]Difference from Spice netlisting procedure where node names and parameter variables are treated separately

Table 4.3. Variable Definition

Variable Property	Nomenclature
Positive Real Number	$variable$
Negative Real Number	$variable\_$neg
Real Number	$variable\_$real
Complex Number	$variable\_$comp

These variables are **ssasonsuz**, **ssasifir** and **ssabir**. The final expressions obtained from symbolic solver are simplified by taking their limits for the cases ssasonsuz goes to infinite, ssasifir goes to zero and ssabir goes to one. This technique proves to be extremely useful for post simplification of the responses of the circuits/systems containing ideal components, such as ideal OPAMPs.

The rules regarding to variable name[7] selection are:

1. A variable name cannot start with '_' sign and cannot contains any of the following signs: \, %, #, &, $, !, |, ˜, <, > and aritmetic operation signs.

2. A variable name cannot start with prefixes 'inl' and 'ssa'.

3. eq11, eq12, eq13, eq14, eq21, eq22, eq23, eq24, eq25, eq31, eq32, eq33, eq34, eq35, eq36, components, update are reserved words.

4. Matlab and maple reserved words are also reserved words of SSA Tool.

5. Variables **s** and **z** are used for s-domain and z-domain calculations. Furthermore, the discrete and continuous time domain variables defined in Table 4.2 are reserved words, i.e. w1, w2, z11, z12, etc...

6. If a variable name and a net name coincide, symbolic solver treats them as identical. Therefore, this kind of parameter assignments results as voltage control behavior.

7. function names, i.e. cos, exp, etc..., are treated as function.

The naming convention of the node name within schematics deep under design hierarchy will be given in section 4.3.4 with the details of the Cadence DFII design flow. Cadence DFII design flow is the only flow supporting hierarchical design. The remaining two flows, i.e. SSA tool custom netlist or Matlab Simulink schematic, do not support hierarchical design.

The naming convention of the voltage source current variables is as follows: The variable starts with the prefix **'Iv_'** and ends with the component name. Therefore, it is crucial to assign a unique name to each component.

---

[7]A variable can be a net, a voltage source current, transfer function name, a variable within a parameter or a parameter itself.

4.3.3   Design Flow using Matlab Simulink schematic capture tool

To ease the analysis of $\Sigma\Delta$ modulators designed using MATLAB Simulink Toolbox, an SSA Tool Simulink library named (conveniently) **ssalibrary** and related interface codes to generate custom SSA Tool netlist from a Simulink mdl-file are developed.

The library contains all necessary components to design $\Sigma\Delta$ modulators. Current version of the ssalibrary has the following blocks: Zero Order Hold, Unit Delay, Discrete Time Integrator, Discrete Transfer Function, Discrete Time Filter, Integrator, Transfer Function, Derivative, Sum, Gain, Product, Polynomial, Quantizer, Constant, Sine Wave, Step, Ground and Scope blocks. The scope block is used to declare signal transfer function definition.

Because of the Simulink schematic editor limitation necessitating that any node should have one and only one driving cell, components requiring bidirectional port connections, such as resistor, capacitor, etc... are not included to the current version of Simulink library.

Each node name is assigned as the instance name of its driving block. For example, the name of a node that is driven by a quantizer having the instance name quantizer1 is quantizer1.

The value of the block parameters can be any complex expression containing multiple variables, arithmetic operations or functions. The component parameters can also be a function of the circuit nodes to create signal controlled component but greate care should be taken to not to introduce nonlinearity to the equation system. In general, this practice is not recommended.

Of course, since SSA Tool is performing small signal analysis, some of the parameters that are meaningful for Simulink environment is meaningless for SSA Tool[8]. Only necessary parameters are netlisted during the process. For the description of the complete ssalibrary blocks and related list of meaningful parameters refer to appendix H.

The interface between the Simulink schematic and the SSA Tool is established with a conversion MATLAB function that converts Simulink models to text based SSA Tool netlist. After building and saving the system schematic using Matlab Simulink schematic editor, ssatool() function call apropriate conversion function to generate SSA Tool netlist, i.e. **convsimu()**.

This function is basically a text processor. It reads the simulink model file and extracts the block and connection information from it. Then it creates a netlist file describing the original circuit to SSA Tool. Block and connection information is extracted from the model file using Matlab function **findsec()** and the netlist conversion is performed by the Matlab function **blockconv()**. To add new component to ssalibrary, it is enough to modify the function blockconv() to recognize the new block and create appropriate SSA Tool netlist

---

[8]For example, the parameter Sample Time
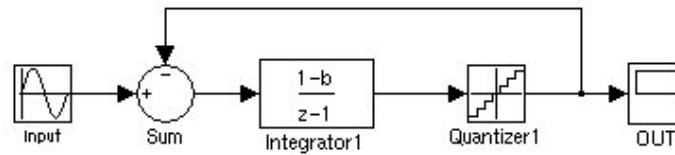
Figure 4.2. First Order $\Sigma\Delta$ Modulator schematic captured from Matlab Simulink Schematic Editor

line. Since blockconv() function contains only text manipulation commands, it is easy to expand it.

Current version of the simulink schematic entry module has the following properties and limitations:

1. Hierarchical design is not supported. Therefore subsystems should not be used.

2. Only the simulink components given within the **ssalibrary** library are supported.

3. The blocks polynomial and product should be used with care because they create non-linearity within the system node equations and therefore they might yield to unsolvable equation system.

4. For every node, there is one and only one driving port (requirement of the simulink schematic editor).

5. Bus connections are not supported. Only Sum and Product blocks can have multiple inputs.

6. For z-domain systems, blocks can have only one single sample time. Multiple sample time within the same system, down sampling or up sampling are not supported. In other word, the variable z is the same for every block within the system.

7. The amplitude of the input source is considered as the input signal magnitude.

8. Quantizer block name assumed to be in the form of Quantizer_qnumber (Quantizer1, Quantizer2, etc...).

9. Quantization noise variable for a given quantizer is named as epsi_qnumber (epsi_1, epsi_2, etc...).

10. During the regular analysis quantizer gain assumed to be equal to 1.

11. During the stability analysis quantizer gain variable is k_qnumber, (k_1,k2_2, etc)

Figure 4.3. SSA_Tool Menu in the banner of Virtuoso Schematic window

Figure 4.4. SSA Tool Pop-Up Form

Example:

The schematic of a simple first order $\Sigma\Delta$ modulator captured using Matlab Simulink schematic editor is shown in Fig. 4.2. The gain mismatch error is also modeled with the error variable b. During the analysis, the model is converted to the custom SSA Tool netlist, which is given below.

```
% Simulink to SSA Conversion Tool Output
% Written By Devrim AKSIN
% Version 1.
% Commercial use is stricly forbidden
% Please contact devrimaksin@ieee.org for info.
% Grounds
{g,gnd}
% Description
{vol,Integrator1,Integrator1,gnd,Sum*((1-b))/(z+(-1)),}
{xtf,OUT,1,Quantizer1,simp,}
{vol,Quantizer1,Quantizer1,gnd,Integrator1+epsi_1,}
{vol,SineWave,SineWave,gnd,Input,}
{vol,Sum,Sum,gnd,SineWave-Quantizer1,}
```

4.3.4 Design Flow using Cadence DFII Virtuoso schematic capture tool

Cadence DFII flow is the main and recommended design flow of the tool. The hierarchical design is supported within Cadence DFII environment.

To use effectively the Virtuoso schematic editor of Cadence DFII a design library named SSALIB is designed. Spectre(s) netlist conversion module supports only the netlist created from the components of the design library SSALIB. The library contains total of 103 device and 44 system, including all the Matlab Simulink blocks, ideal macro blocks, linear and non-linear passive components, nonlinear active components, independent sources, dependent sources, global sources, as well as, custom models of on-chip inductance, crystal

resonator, etc... The library also contains special cells to extract the voltage or current data from the solution variable, to control the analysis mode of the symbolic solver and to set the options of the extension modules. CDF parameters of the components are edited so that they can be correctly netlisted by the Spectre/SpectreS netlister. The complete list of available components and their parameters and descriptions are given in appendix H.

The value of the components' parameters can be any complex expression containing multiple variables, arithmetic operations or functions. It may also contain node names or voltage source currents as a variable to implement dependent components. But since this approach might result non-linear equation system that are unsolvable, great care should be taken while using node names within the parameter expressions.

The interface between the Cadence Virtuoso schematic and the SSA Tool is established in two steps. First step involves the creation of the netlist within the Cadence DFII design environment. For this purpose Cadence SKILL files, executing necessary Cadence procedures are developed. Provided codes add a menu item named 'SSA_Tool' to the banner of the schematic window, as shown in Fig. 4.3. containing SSA Tool Netlister. Choosing SSA Tool Netlister displays a Pop-Up Form window, shown in Fig. 4.4. allowing user to select between two netlisters, i.e. Spectre and SpectreS, and netlisting directory. The default netlister is SpectreS. The reason for this choice is that SpectreS netlister allows flat netlisting which in turn make it possible to use multiple hierarchies within the schematic design. This property allows designer to build custom small signal models with arbitrary accuracy and complexity using SSALIB basic components. Spectre netlister does not support hierarchical design. The netlisting directory is the directory where the final netlist will be created and saved. After clicking OK button on the form window, the circuit netlist is created[9].

After generating spectre(s) netlist within Cadence DFII environment, the conversion module of SSA Tool translates it to custom SSA Tool netlist. To add new component to SSALIB library, the matlab function **comp2netlist()** function should be modified so that it recognizes new component and creates appropriate SSA Tool netlist line.

For SpectreS netlister, the node names that are within a lower hierarchy level have the following naming convention: Node name at lower hierarchy level got a prefix that is the name of the instance under which the node is following with the word **'UndeR'**. For example, assume that the original name of a node that is within the instance named Ibir that is in turn within the instance Iiki with respect to the top level hierarchy, is net1 then the final netlist name of this node is IikiUndeRIbirUndeRnet1. The instance name of the design has the same naming convention.

Example:

---

[9]Towards the end of the netlisting process, the user is asked whether he/she wants to save the analog artist state.
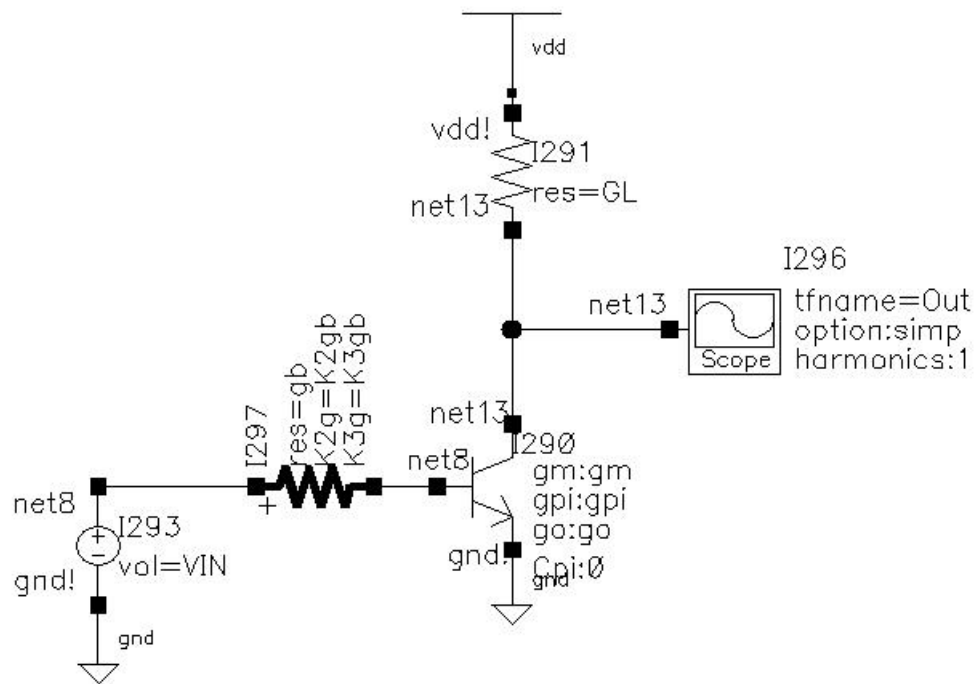
Figure 4.5. Simple bipolar amplifier schematic captured from Cadence DFII Virtuoso Schematic Editor

The schematic of a simple bipolar amplifier captured from Cadence DFII Virtuoso schematic editor is shown in Fig. 4.5. Non-linear base resistance is explicitly included to the schematic. The SpectreS netlist created using provided Cadence SKILL codes is given below.

```
* # File name: ~/SSASIMDIR/test_sch/spectreS/schematic/netlist/
# test_sch.c.raw
# Netlist output for spectreS.
simulator lang=\spectre
ahdl0 (5 4) nondirenc res=gb K2g=K2gb K3g=K3gb
ahdl1 (3) Scope tfname=Out option=simp harmonics=1.0
ahdl2 (5 0) voltaj vol=VIN
ahdl3 (1 3) direnc res=GL
ahdl4 (3 4 0) npn gm=gm gpi=gpi go=go Cpi=0.0 K2gm=K2gm K2gpi=K2gpi &
K2go=0.0 Kgmgo=Kgmgo K2cpi=0.0 K3gm=K3gm K3gpi=K3gpi K3go=0.0 &
K32gmgo=K32gmgo K3gm2go=0.0 K3cpi=0.0
# Include file for AHDL
# HDL text files to be included for this design.
ahdl_include "~/TEMP/SSALIB/npn/ahdl/ahdl.def"
ahdl_include "~/TEMP/SSALIB/direnc/ahdl/ahdl.def"
ahdl_include "~/TEMP/SSALIB/voltaj/ahdl/ahdl.def"
ahdl_include "~/TEMP/SSALIB/Scope/ahdl/ahdl.def"
ahdl_include "~/TEMP/SSALIB/nondirenc/ahdl/ahdl.def"
simulator lang=\spice
simulator lang=\spectre
```

```
simulator lang=\spice
# Include files
simulator lang=\spectre
# End of Netlist
```

Next, SSA Tool netlist conversion module translates the spectres netlist to SSA Tool netlist, as shown below.

```
% Spectre to SSA Conversion Tool Output
% Written By Devrim AKSIN
% Version 1.
% Commercial use is stricly forbidden
% Please contact devrimaksin@ieee.org for info.
% Grounds
{g,glb_ground}
% Description
% Circuit Netlist
{nonres,ahdl0,net8,net06,gb,K2gb,K3gb,}
{xtf,Out_bir,1,net13_bir,simp,}
{vol,ahdl2,net8,glb_ground,VIN,}
{res,ahdl3,glb_ground,net13,GL,}
{bjt,ahdl4,net13,net06,glb_ground,gm,gpi,go,K2gm,K2gpi,Kgmgo,K3gm,K3gpi,K32gmgo,
0.0,0.0,0.0,0.0,0.0,0.0,}
```

Even though, the component models within the netlist contain related non-linearity coefficients, this netlist is not enough to run non-linear analysis. The input source type should be changed to non-linear input source type and the analysis definition component, i.e. ana or anaim, should be included. The nonlinear analysis flow will be detailed in section 4.9.

4.4   Circuit Solver

After the creation of the custom SSA Tool netlist, the tool invokes the symbolic circuit solver. The Matlab function that supervises the solving processes named **ssamain()**. The supervisor calls during the solving process several sub-functions that reads the SSA Tool netlist file, calculates individual branch currents, generates the symbolic node equations, solves the linear equation system and assigns the output variables.

Nonlinear analysis of the circuit is also performed by this module. The circuit solver does the necessary netlist modifications, solves the modified netlists to calculate the circuit higher order responses and finally assigns the results to the proper output variables. The current version of SSA Tool is able to calculate circuit responses up to third order.

It is also possible to access the circuit solver separately. The nomenclature to call the symbolic circuit solver is

ssacirsol=ssamain(netlist_file_name)

the input argument netlist_file_name is a string variable containing the name of the custom SSA tool netlist file. The module assumes that the extension of the file is **'.m'**. The

outputs of the modules are already defined in section 4.2.

Example 1:

The first order $\Sigma\Delta$ modulator shown in Fig. 4.2 is analyzed using SSA Tool. The output structure variable of the symbolic circuit solver has two fields. The field ssacirsol.eq11 contains the linear circuit solution. The symbolic expression of each node within the system is given in this field. The variables $Input$, $epsi\_1$ and b are the input signal magnitude, quantization error introduced by the quantizer block and gain mismatch error of the discrete time integrator, respectively.

$$ssacirsol{\cdot}eq11 = \begin{bmatrix} Integrator1 & -(epsi\_1 - Input) \times (-1 + b)/(b - z) \\ Quantizer1 & (-Input + b \times Input - z \times epsi\_1 + epsi\_1)/(b - z) \\ SineWave & Input \\ Sum & (epsi\_1 - Input) \times (z - 1)/(b - z) \\ gnd & gnd \end{bmatrix} \qquad (4.1)$$

The second field is named ssacirsol.OUT and its content is the output signal of the modulator, i.e. Quantizer1. After the simplification of this field using $\Sigma\Delta$ modulator analysis module, we obtain the signal and noise transfer functions of the modulator.

$$ssacirsol{\cdot}OUT = \frac{1 - b}{z - b}Input + \frac{z - 1}{z - b}epsi\_1 \qquad (4.2)$$

Example 2:

The bipolar amplifier shown in Fig. 4.5 is analyzed with SSA Tool. Since the circuit does not have any analysis mode definition cell, i.e. ana or anaim, the tools performs only linear analysis. The output structure variable of the circuit solver has two fileds, i.e. ssacirsol.eq11 and ssacirsol.OUT_eq11. The first field contains the linear circuit response.

$$ssacirsol{\cdot}eq11 = \begin{bmatrix} net8 & VIN \\ net06 & gb \times VIN/(gb + gpi) \\ net13 & -gm \times gb \times VIN/(GL + go)/(gb + gpi) \\ glb\_ground & glb\_ground \end{bmatrix} \qquad (4.3)$$

The second field contains the amplifier output signal, which is minus the transconductance of the npn transistor divided by the output conductance (first term of the equation) multiplied by the voltage at the base terminal of the transistor which is the output of the resistive divider formed by the transistor input conductance (gpi), and the conductance gb (second term of the equation).

$$ssacirsol{\cdot}OUT\_eq11 = -\frac{gm}{GL + go}\frac{gb}{gb + gpi}VIN \qquad (4.4)$$

4.5   Result Post-Processing

SSA tool allows post-processing of the circuit solutions. It is possible to use two different ways for this purpose.

1. Schematic option definition

2. Post-processing module

The schematic option definition can be used to create Matlab work space executable lines. The details of the schematic option definition has been given in section 4.3. A better way to use for complex solution manipulations, is the post processing module.

The post-processing module is very helpful for applying transformations to the solution space. An example of such transformation is up or down sampling in multi-rate systems. Since, the definition of discrete time frequency variable z is the same for all blocks within the circuit during the analysis, the transformations for up and down sampling should be performed separately after executing circuit solver module. The post-processing module basically execute a .m file that contains any command line executable Matlab function or processing code. The extension modules, i.e. $\Sigma\Delta$ Analysis module or Transfer Function analysis module, or any other custom function of the SSA Tool can be accessed and executed from within the post processing module, multiple times.

For this purpose the schematic option ssapostprocesssw should be set 'on' and a post processing file name should be provided through the schematic option ssapostprocessmfilename. These two options can be declared either within the ssatool() function or within the Cadence schematic using **optpp** cell.

The variables that can be processed are the output of the circuit solver. The outputs are stored in the structure variable ssacirsol[10]. Hence available fields are ssacirsol.eq$_{XY}$ and ssacirsol.TFN. Notice that the variables ssacircol.eq$_{XY}$ are two columns matrixes. First column contains the circuit node and voltage source current variables. The second column contains the circuit solutions. Using ssacirsol.TFN format with transfer function extraction method is a more convenient way to access the solution space.

Since the post-processing file is executed within the flow of the tool, it is not possible to access directly any variable created within the post-processing file. If it is necessary to access a post-processing variable, it can be done using the structure variable output of the circuit solver[11]. For example, to be able to access the variable $Yout$ created within the post processing file from the Matlab workspace at the end of the SSA tool execution, the command $'ssacirsol\cdot Yout = Yout;'$ should be included to the post-processing file. As a result

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[10]This is the exact name. Hence, it should be used as it is within the post-processing file.

[11]By using the format ssacirsol.TFN

an extra field named $Yout$ will appear within the structure variable ssacirsol. An example post processing Matlab file is also provided within the tool.

4.6 $\Sigma\Delta$ Modulator Analysis Module

4.6.1 Towards the Automation of $\Sigma\Delta$ Modulator Design and Optimization

The SSA Tool contains $\Sigma\Delta$ modulator analysis module that eases the analysis, design and optimization of complex modulator architectures. As it will be clear with the examples in chapter 6, this extension module proves to be indispensable for modulator topology optimization and analysis. Using the module, it is possible to analyze and optimize

- signal transfer function (STF),
- noise transfer function (NTF),
- sensitivity of these transfer functions to circuit coefficients,
- modulator stability (linear root locus method) and critical quantizer gain,
- optimize STF and NTF together to determine the best modulator coefficients,
- signal swing at any node within the system,
- in band noise power, SNR, SFDR of the modulator,
- the effect of the finite DC gain and its nonlinearity, gain bandwidth product (or linear settling error), slew-rate of the integrator amplifiers,
- the effect of the mismatch (channel mismatch or gain error),
- the effect of switch on resistance and its nonlinearity,
- noise,
- the effect of DACs non-linearity in multi-bits sigma-delta modulators

of arbitrary $\Sigma\Delta$ modulator architecture. The module is capable of expressing symbolically SNR degradation and the spurious-free-dynamic range of the modulator for all these cases in terms of modulator parameters.

The module is designed with optimization automation goal in mind. The next step towards the optimization automation is the design of an engine that will determine the critical blocks and parameters of the modulator, and will use the analysis module to quantify the effects of their non-idealities to the performance.

Large signal non-idealities of the integrator amplifiers essentially creates harmonic distortion. Therefore, it is also possible to model and analyze the effect of the amplifiers large signal non-idealities symbolically using SSA tool.

4.6.2 Executing the $\Sigma\Delta$ Analysis Module

There are three ways to enable and call (use) the analysis module. It is possible to use

1. matlab function ssatool() together with proper option settings. For this purpose, the option ssasigmadeltasimp should be set 'on' and the output of the modulator should be declared using the option ssasdoutvarname. The symbolic expression name should match with the variable name containing symbolic expression within the Matlab workspace. This variable might be created while executing a post-processing file or it might be the output of the circuit solver.

2. It is possible to use the cell **optsd** within the Cadence schematic, which basically does set the options described above.

3. It is possible to use post processing module to call the module functions, i.e. **ssasdmodule()**.

It is also possible to analyze more than one variable. The output variable name string should consist of signal name list string. The names should be separated with a comma sign within the string.

4.6.3 Simplification of the Symbolic Expressions

The $\Sigma\Delta$ modulator analysis module uses a priori system knowledge to simplify the linear analysis expressions. $\Sigma\Delta$ modulators can be modeled as two input linear system. Those inputs are actual modulator input signal, X, and the quantization noise signal, ϵ. Like every linear system, $\Sigma\Delta$ modulators obey the superposition principle. Therefore, the output of the modulator can be expressed in the following form

$$OUT = SNF \times X + NTF \times \epsilon \tag{4.5}$$

where SNF and NTF are signal and noise transfer functions of the modulator, respectively. The module uses this information to simplify the expressions. To extract the noise transfer function, the input signal is substituted with zero and the resulting expression is simplified.

If there are more than one quantizer block within the system, such as MASH structure or time interleaved modulator structure, each one of these quantizer blocks will introduce an extra white quantization noise signal to the system. Thanks to the linearity and the superposition principle, these noise signals will appear as additive terms in equation 4.5 at the output of the modulator with their associated noise transfer functions. The $\Sigma\Delta$ analysis module extracts the noise transfer function of each quantization noise signal separately. For such case, after substituting the input signals by zero within the expression, all quantization
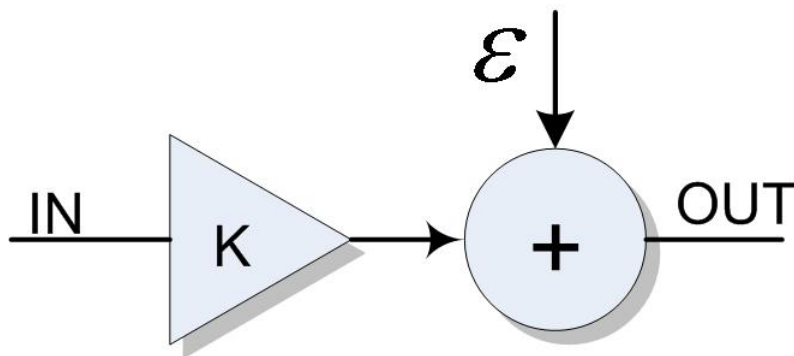
Figure 4.6. Linear Quantizer Model

noise signal, except the one that is in the consideration, will also be substituted with zero in order to obtain corresponding noise transfer function. Of course, this procedure is repeated until all NTFs are obtained. To extract signal transfer function, all of the quantization noise variable is substituted with zero and the resulting expression is simplified.

After extracting STF and NTF from the output signal, the module process these transfer functions further to determine the system stability, in band noise power, etc...

4.6.4 Stability Analysis

The criterion to determine the stability of $\Sigma\Delta$ modulators or in general a non-linear system is still an ongoing research area. In the literature, there are several stability criterion extracted using linear analysis of the $\Sigma\Delta$ modulator structure. The module performs the following stability analyses:

1. Modified Lee criterion

   A single bit modulator with a noise transfer function $H(z)$ is stable if

   $$\max_{w} |H(e^{jw})| < 1{\cdot}5 \tag{4.6}$$

   is satisfied. This criterion should be treated as a helpful rule of thumb, since it has no solid theoretical background. Generally speaking, the peak of the noise transfer function generally occurs[12] for $w = \pi$ or $z = -1$.

2. Linear Root Locus Analysis

   Since the transfer function of the quantizer is a step function, the gain of the quantizer block cannot be defined. Fig. 4.6 shows a linear quantizer model. Ideally, the quantizer gain, i.e. K, is assumed to be equal to 1. In reality, the quantizer gain is defined with

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[12]An exception is the modulator structures having high-Q poles.

respect to the input signal magnitude.

$$K = \frac{< OUT, IN >}{< IN, IN >} = \frac{E\left[|IN|\right]}{E\left[IN^2\right]} \tag{4.7}$$

where the output signal is equal to $OUT = \text{sign}[IN]$. The module replaces the unity gain of the quantizer with the quantizer gain variable and extracts the noise transfer function of the modulator as a function of it. The stability of the modulator is predicted by drawing the locus of the NTF roots while sweeping the quantizer gain within $0 < K < 1$. To obtain unconditional stability, all the roots of the NTF should be within the unit circle for all value of K. For higher order modulators, the root locus method shows the stability of the modulator decreases with decreasing quantizer gain. There is a one critical value of the quantizer gain at which the noise transfer function roots are on the unit cycle. Since the output of the quantizer has constant amplitude, the gain drops with increasing input amplitude. Therefore, the problem of making the modulator stable is equivalent to finding maximum allowable input signal magnitude that will make the quantizer gain higher than its critical value. Examples of root-locus plot can be found in chapter 6.

4.6.5 $\Sigma\Delta$ Analysis Module function: ssasdmodule() and the Outputs of the module

The supervisor Matlab function that controls the $\Sigma\Delta$ analysis module is **ssasdmodule()**. The input arguments of the function with their description are listed below. While calling the module function, the argument order given here should be preserved.

1. SymbolicExpression

   This is the symbolic expression containing the output signal of the $\Sigma\Delta$ modulator.

2. Input_Signal_Amplitudes

   Vector of input signals amplitude variables. The function expect the variable InputSignalAmplitude to be generated by SSA Tool. For stand-alone use, this variable should be a structure variable having the field 'ampl' that contains the input signal amplitude variable(s). Modulator may have multiple input signal. The signal transfer function of each one of the input signals are calculated separately.

3. Quantization_Error

   Vector of Quantization Error amplitude variables. The function expect this variable to be generated by SSA Tool. For stand-alone use, this variable should be a structure variable having the field 'nameq' that contains the quantization error signal amplitude

variable(s). The modulator structure may have multiple quantizer, as in the case of MASH structure. The module calculate the noise transfer function of each one the corresponding quantization noise signal separately.

4. Quantizer_Gain

Vector of Quantizer Gain variables. The quantizer block within the modulator is modeled as an adder that adds its input signal with white quantization noise. The function expect this variable to be generated by SSATool. For stand-alone use, this variable should be a structure variable having the field 'qgain' that contains the quantizer gain symbolic variables. During the stability analysis, the SSA Tool uses the naming convention, $K\_quantizername$[13], to assign a variable to a quantizer but this is not mandatory. Simply, these are the variables that are swept from 0 to 1 to extract pole-zero plot of the modulator and critical gain of the quantizer.

5. Sigma_Delta_Stability_Enable

This argument is used to enable stability analysis. It should be set equal to 1 to enable the stability analysis.

6. Option

This option variable is used for non-linearity analysis of the modulator. Possible values are 'off' for linear analysis and 'on' for nonlinear analysis. During the linear analysis, modulator output assumed to be linear and STF(s) and NTF(s) are extracted as defined above. During the nonlinear analysis, the quantization noise variable(s) within the output signal is substituted with zero to obtain non-linear response.

The output of the module is a structure variable. It has the following fields:

xtfname field contains the name of the modulator output signal or the signal analyzed.

result field contains simplified modulator transfer function in the form defined in equation 4.5.

stf field contains signal transfer function related analysis results. Its subfields are

- **tf** contains extracted signal transfer function(s).

- **poles** contains the poles of the STF. The field exists if STF poles can be calculated.

- **zeros** contains the zeros of the STF. The field exists if STF zeros can be calculated.

ntf field contains noise transfer function related analysis results. Its subfields changes with respect to whether the stability analysis is enabled or not. If the stability analysis is not enabled, the subfields are

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[13]Example: K_1, K_2, etc...

- **help** is an help string containing information related to the definition of the subfields.

- **ntfl** contains extracted noise transfer function expressions for each quantization noise variable.

- **order** contains the noise shaping order of each extracted NTFs.

- **stab** contains stability related information, such as Lee criterion.

- **powint** contains the expression of integrated in band quantization noise power.

- **powsimp** contains the expression of integrated in band quantization noise power simplified with the assumption that over sampling ratio is much bigger than one.

- **powintbode** contains the integrated noise power extracted from the bode plot of the associated noise transfer function. This is a two column matrix. First column contains the over sampling ratio and the second column contains associated in band quantization noise power. The field exists if an LTI system definition can be extracted from the expression.

- **ntfpoles** contains the poles of the NTF. The field exists if NTF poles can be calculated.

- **ntfzeros** contains the zeros of the NTF. The field exists if NTF zeros can be calculated.

The module gives also SNF and NTFs bode plot, if the expression does not have any symbolic variable except the discrete time frequency variable z. If the stability analysis is enabled, the subfields of ntf are

- **help** is an help string containing information related to the definition of the subfields.

- **ntfl** contains extracted noise transfer function expressions for each quantization noise variable.

- **powint** contains the expression of integrated in band quantization noise power.

- **qgain** contains the poles, zeros and critical values at different sweep value. It has the following subfields

  1. polezero contains the pole locus for of corresponding noise transfer function quantizer gain 0.

  2. poleone contains the pole locus for of corresponding noise transfer function quantizer gain 1.

  3. zerozero contains the zero locus of corresponding noise transfer function for quantizer gain 0.

4. zeroone contains the zero locus of corresponding noise transfer function for quantizer gain 1.

5. criticalK contains the critical quantizer gain value.

6. critpole contains the pole locus for critical quantizer gain.

7. critzero contains the zero locus for critical quantizer gain.

The module also gives the root-locus plot during stability analysis. It is also possible to run the same analysis for any arbitrary variable defined within the system to check the stability sensitivity of the noise transfer function to that particular variable.

4.7 Transfer Function Analysis Module

Transfer function analysis module designed to analyze extracted transfer functions. It proves to be useful to draw quickly the bode plots of continuous or discrete time systems or to analyze complex impedance/admittance functions. Using the module, it is possible to extract

- real part of the transfer function

- imaginary part of the transfer function

- magnitude of the transfer function

- resonance frequency

- peak frequency

- low and high frequency asymptotes

of the analyzed transfer function. It is also possible to analyze discrete time domain expression. Before processing the expression, the module substitutes discrete time frequency variable(s) with its(theirs) corresponding continous time expression as given in Table 4.2.

There are three ways to enable and use the transfer function analysis module[14]. It is possible to use

1. matlab function ssatool() together with proper option settings. For this purpose, the option **ssaimpon** should be set 'on', the transfer function name that will be analyzed should be declared using the option **ssaimpvar** and finally the option **ssaimpadmit** should be set to convert the impedance function to admittance function if necessary.

2. or it is possible to use the cell **opttf** within the Cadence schematic, which basically does set the options described above

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[14]Exactly the same as the $\Sigma\Delta$ analysis module

3. or finally, using post processing module.

It is also possible to analyze more than one variable. The output variable name string should consist of signal name list string. The names should be separated with a comma sign within the string.

A special cell named **impcurs** is added to Cadence SSALIB library to ease the impedance analysis flow. To obtain the impedance of any given node, it is necessary to first nullify all the input signal sources present within the circuit and then connect the cell impcurs[15] in between that particular node and ground. As a result of the linear analysis of this circuit, the node voltage that the cell impcurs connected is equal to the node impedance.

The conversion from impedance function to admittance function is achieved by taking the inverse of the expression. This conversion is required simply because the circuit solution obtained from the tool is in the form of node voltages; hence it is only possible to extract symbolic impedance function from the circuit solver.

The module process flow is supervised by the function ssarealimaginary(). The input arguments of the function are

1. **expression** contains the symbolic expression that will be analyzed.

2. **name** is the name of the expression as it appears in Matlab work space.

   The output of the module is a structure variable. It has the following fields

- **name** is the name of the transfer function as it appears within the Matlab work space

- **jw** contains the original expression.

- **real** contains the real part of the expression.

- **imag** contains the imaginary part of the expression.

- **realimag** contains the expression in the form of a+i*b

- **magnitude** contains the magnitude expression of the expression

- **resonance** contains the resonance frequency of the transfer function, if there is one.

- **extremumf** contains the peak frequency of the expression, if there is on.

- **dc** contains low frequency asymptote.

- **highfreq** contains high frequency asymptote.

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[15]This is actually a simple current source with magnitude -1

- **bodemag** is two column matrix. The first column is the frequency and the second column is the corresponding magnitude of the expression.

- **bodepha** is two column matrix. The first column is the frequency and the second column is the corresponding phase of the expression.

4.8 Custom Model Definition

SSA Tool offers two alternative ways to add new device model to the tool.

The first option is to create a Cadence Virtuoso schematic using SSALIB primitive cells, i.e. resistors, capacitors, inductors, voltage controlled current sources, voltage controlled voltage sources, etc... and to use it as the new device model. This design flow is only valid, if the design environment is Cadence DFII and SpectreS netlister is used to netlist the circuit. As explained previously, it is not possible to use this flow neither with Spectre netlister nor with Matlab Simulink schematic editor.

The second option is to write a custom device model function in Matlab. When SSA netlister find a definition acronym that is not hard coded within the tool, it tries to execute the Matlab function starting with the prefix **'model'** and ending with the acronym of the definition[16].

These model functions contain linear and non-linear model information of the custom device. For convenience, they are located within the *custommodel* directory underneath the SSA Tool installation director. In order to facilitate the development of new model, the Matlab function modelmos.m contains comment lines explaining in detail how to modify the function and what to include or to remove from it to obtain a new customized model file.

The main limitation of writing a custom model function is that it is not possible to include internal node to the model. Hence the nodes of the model should be the terminals of the device. The only way of building complex device model containing internal nodes is to use Cadence Virtuoso schematic editor together with SpectreS netlister.

Custom model files have 9 sections each of which is used at the different stage of the circuit response calculations.

Section 1 contains the linear response analysis related component descriptions. If the modeled device will never be part of a netlist that runs second or third harmonic response analysis, customizing first section is enough. But, even though, modeled component is linear, if it will ever be in a netlist that runs non-linear analysis, sections 2 through 9 have also be modified properly.

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[16]For example, the Matlab function name searched to process the netlist line {bjtHighF,..,} is modelbjtHighF.m

Section 2 adds the non-linear current sources that should be included during the second order response analysis of the circuit. The answers to the questions 'Which non-linear current sources should be added?', 'How many non-linear current sources should be added?', 'What is the value of these non-linear current sources?' or 'Between which nodes, these non-linear current sources should be connected?' will be given later in section 4.9. Section 3 and 8 replace the second order harmonic and intermodulation distortion current sources with their equivalent values in terms of component non-linearity coefficient values and circuit's linear response. Again, the calculation of the non-linear current source equivalent value will be explained in more detail in section 4.9.

Section 4 adds the non-linear current sources that should be included during the third order response analysis of the circuit and section 5 and 9 replaces the third order harmonic and intermodulation distortion current sources with their equivalent values in terms of component non-linearity coefficient values and circuit's smaller order responses.

Section 6 adds a comment line to custom SSA tool netlist showing the nomenclature of the model. Section 7 is used during the terminal current calculations.

4.9 Basics of Non-Linear Analysis

SSA Tool calculates circuit second and third order harmonic and intermodulation distortion transfer functions using the technique described in 'Non-Linearity analysis of Analog Integrated Circuit' of Piet Wamback and Willy Sansen [60]. The method is based on modified small signal analysis technique and is capable of computing the harmonic responses of weakly non-linear circuits (or low-distortion circuits). The term weakly non-linear circuits refer to the following conditions:

1. The non-linear circuit should be exited by an input signal magnitude small enough so that n^{th} order harmonic response of the circuit can be determined by only its nth order nonlinear behavior,

2. The energy of the output signal is concentrated towards the lowest harmonics. In other words, the array of amplitudes of the even and odd order harmonics is decreasing,

3. the devices should not change operation region.

Weakly non-linear behavior is typically due to the curvature of the device characteristics in a given operation condition whereas the strong non-linear behavior is due to the operation region changes of the device such as turn on and off of a transistor. Weakly-nonlinear behavior is need to be able to assume that the magnitude of nth harmonic at the

output of a circuit is a function of only the circuit's n^{th} and lower order responses so that each harmonic response can be sequentially calculated from the circuit's lower order responses.

Due to weakly-nonlinear behavior assumption, the effects of the higher order harmonics to the lower order harmonics are ignored. Therefore, some performance parameters such as compression points cannot be calculated using this method.

To not to repeat what has already been done, the axioms of the method will be recited here and the procedure to calculate the harmonic responses of a circuit using this method will be explained without any formal proof. Interested reader should refer to book for more detail.

Although, there is no theoretical limitation, SSA Tool is build to calculate at most third order harmonic response. The reasons for this decision are:

1. the weakly nonlinear circuit assumption necessitates that second and third harmonics have to be the largest even and odd order harmonics, respectively and

2. in general, the dominant harmonic component at the output of a single-ended and differential circuit are its second order and third order harmonics, respectively.

Now, let us proceed with the description of the nonlinear analysis technique. Every device within the analog integrated circuits can be modeled at an operating point with an equivalent circuit containing the following basic non-linear components:

1. Non-linear conductance,

2. Non-linear resistance,

3. Non-linear capacitance,

4. Non-linear transconductance,

5. Non-linear transresistance.

The first step towards the solution, is the determination of the equivalent circuit and corresponding nonlinear terminal equations. SSA Tool solves the circuit response using node equations. Therefore, it is necessary to model non-linear resistance and non-linear transresistance components in the form of $I = f(V)$. The detail of this transformation can be found in [60].

The analysis technique uses power expansion coefficients of nonlinear device model which are calculated around device's operation point during the evaluation of the final expression. The assumption of weakly non-linear circuit allows ignoring the terms of the power series that have higher order than the harmonics response that will be calculated, i.e. the terms having order greater than three. The term expansion coefficients will be used to refer

to the power series expansion coefficients. The term nonlinearity coefficients will be used to refer expansion coefficients of order greater than one. The power series expansion of three variable function $f(x_1, x_2, x_3)$ is given in equation (4.8).

$$y = f(x_1, x_2, x_3) = \underbrace{y_0 + \frac{\delta f}{\delta x_1}x_1 + \frac{\delta f}{\delta x_2}x_2 + \frac{\delta f}{\delta x_3}x_3}_{Linear\ Terms} \tag{4.8}$$

$$\underbrace{+ \frac{1}{2}\frac{\delta^2 f}{\delta x_1^2}x_1^2 + \frac{1}{2}\frac{\delta^2 f}{\delta x_2^2}x_2^2 + \frac{1}{2}\frac{\delta^2 f}{\delta x_3^2}x_3^2 + \frac{\delta^2 f}{\delta x_1 \delta x_2}x_1 x_2 + \frac{\delta^2 f}{\delta x_1 \delta x_3}x_1 x_3 + \frac{\delta^2 f}{\delta x_2 \delta x_3}x_2 x_3}_{Second\ Order\ Terms}$$

$$+ \frac{1}{6}\frac{\delta^3 f}{\delta x_1^3}x_1^3 + \frac{1}{6}\frac{\delta^3 f}{\delta x_2^3}x_2^3 + \frac{1}{6}\frac{\delta^3 f}{\delta x_3^3}x_3^3 + \frac{1}{2}\frac{\delta^3 f}{\delta x_1^2 \delta x_2}x_1^2 x_2 + \frac{1}{2}\frac{\delta^3 f}{\delta x_1 \delta x_2^2}x_1 x_2^2$$

$$\underbrace{+ \frac{1}{2}\frac{\delta^3 f}{\delta x_1^2 \delta x_3}x_1^2 x_3 + \frac{1}{2}\frac{\delta^3 f}{\delta x_1 \delta x_3^2}x_1 x_3^2 + \frac{1}{2}\frac{\delta^3 f}{\delta x_2^2 \delta x_3}x_2^2 x_3 + \frac{1}{2}\frac{\delta^3 f}{\delta x_2 \delta x_3^2}x_2 x_3^2 + \frac{\delta^3 f}{\delta x_1 \delta x_2 \delta x_3}x_1 x_2 x_3}_{Third\ Order\ Terms}$$

For example, the MOS transistor drain current can be expressed with power series expansion using more familiar coefficient symbols as follows[17] :

$$I_D = \underbrace{I_{D0} + gmV_{GS} + goV_{DS} - gmbV_{SB}}_{Linear\ Terms} \tag{4.9}$$

$$\underbrace{+ K_{2gm}V_{GS}^2 + K_{2go}V_{DS}^2 - K_{2gmb}V_{SB}^2 + K_{gmgo}V_{GS}V_{DS} + K_{gmgmb}V_{GS}V_{SB} + K_{gogmb}V_{DS}V_{SB}}_{Second\ Order\ Terms}$$

$$+ K_{3gm}V_{GS}^3 + K_{3go}V_{DS}^3 - K_{3gmb}V_{SB}^3 + K_{32gmgo}V_{GS}^2 V_{DS} + K_{3gm2go}V_{GS}V_{DS}^2$$

$$\underbrace{+ K_{32gmgmb}V_{GS}^2 V_{SB} + K_{3gm2gmb}V_{GS}V_{SB}^2 + K_{32gogmb}V_{DS}^2 V_{SB} + K_{3go2gmb}V_{DS}V_{SB}^2 + K_{gmgogmb}V_{GS}V_{DS}V_{SB}}_{Third\ Order\ Terms}$$

First order expansion coefficients are used daily basis by the engineers to calculate regular small signal linear response[18]. The output expressions of the SSA Tool describing linear or non-linear responses are function of the input signal, expansion coefficients of the non-linear devices and the frequency variables s or z[19].

Before discussing how the method obtains the nonlinear transfer functions, it is important to develop a strategy for improving the accuracy and manageability of the final results. As it is true for most of the engineering problem, the term accuracy is relative to the expectations and the aim of the analysis.

It is possible to identify two kinds of accuracy for the evaluation of the nonlinear transfer function. First one is the accuracy of the expression itself. In other word, how many of the nonlinear devices within the circuit should be modeled as detailed as shown in equation 4.9 or how many terms of the equation (4.9) is enough?

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[17]This notation will be used to refer expansion coefficients.

[18]The distinction between small signal linear response and small signal non-linear response is necessary because the non-linear analysis technique uses small signal analysis techniques to obtain circuit's non-linear responses.

[19]Of course the definition of the frequency variables changes with respect to the harmonic response that is calculated.

The non-linear analysis method is capable of calculating the non-linear response with arbitrary expression accuracy. Hence, it is possible to model all of the devices perfectly. But improving expression accuracy trades with the calculation process time and interpretability of the expression. For example, a very accurate device model of a MOS transistor should contain gate-source, gate-drain, gate-bulk, source-bulk and drain-bulk capacitances (and for PMOS transistor in NWELL processes, bulk-substrate capacitance as well); gate, drain, source, bulk serial resistances; drain current source that is function of gate-source, drain-source and source-bulk voltages. To model all these basic nonlinear devices together with their non-linearity, it is required to define 38 parameters. Hence for a circuit having just 10 transistors, the final expressions will have, in worst case, 380 parameters. Obviously, trying to solve this equation system will take somewhat longer than a system having just, say, 10 parameters. And, obtained final expressions will be (in general) impossible to interpret[20].

From engineering point of view, extreme accuracy is rarely needed. Therefore, it is important to chose a correct device model (or parameter set) for targeted accuracy. The dominant distortion term can also change with the operation point and frequency of the circuit. For example, the distortion at the output of a capacitively loaded emitter follower is dominated by the transconductance related nonlinearity coefficients (such as K_{2gm}, K_{3gm}) at high operating frequencies, whereas it is dominated by the output conductance related nonlinearity coefficients at low operating frequencies. Hence, at low operating frequencies including transconductance related nonlinearity coefficients[21] will not improve the accuracy (in numerical sense) but will just make the final expression more complex, difficult to calculate and/or interpret. Therefore, it is important to carefully simplify and/or ignore some of the parameters that will not dominate the value of the final expression to obtain relatively fast, an interpretable expression with acceptable numerical accuracy. In reality, it is enough to model nonlinearly only few devices within the circuit to obtain acceptable level of expression accuracy.

The second kind of accuracy is related to the accuracy of the expansion coefficients' values, which is important, of course, for numerical evaluation of the final expressions. The accuracy of the expansion coefficient's numerical value is determined by the accuracy of the nonlinear device model equation. Using very accurate device model equation yields good accuracy but difficult to handle expansion coefficient expressions.

The selection of the device model should be consistent with expected dominant distortion term. For example, if the output resistance of the MOS transistor is expected to be the dominant source of the distortion, the simple MOS model, which is $I_D = 0.5\beta(V_{GS} -$

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[20]Having an expression that is not interpretable might not be an important issue. The symbolic expression can still be used to evaluate (numerically) the sensitivity of the expression to a given parameter to identify critical devices (and/or parameters).

[21]Or equivalently including output conductance related nonlinearity coefficients at high operating frequencies
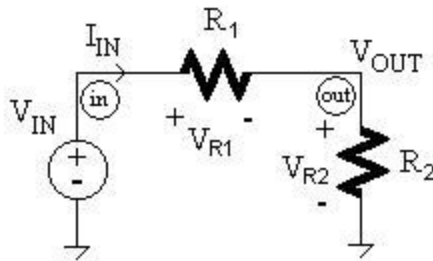
Figure 4.7. Non-Linear Resistive Divider

$V_T)^2(1 - \lambda V_{DS})$, should not be used[22]. Therefore, it is important to predict accurately dominant distortion terms with respect to circuit's topology, biasing and operating conditions and select appropriate device model. As an example, the expressions of the expansion coefficients of a bipolar transistor model that is accurately modeling the non-linearity of the device's output conductance are given in appendix G. More detailed discussion about how to calculate (measure) MOS and bipolar transistors' expansion coefficients can be found in [60].

From circuit analysis point of view, each non-linearity coefficient creates a non-linear current source within the equivalent circuit. Therefore, the answers to the questions, brought up during the custom models definition section, 'Which non-linear current sources should be added?', 'How many non-linear current sources should be added?' are related strictly to the accuracy of the final expressions as discussed above.

As a final word related to the accuracy, the accuracy of the final expression is important to extract its tendencies; whereas, the accuracy of the expansion coefficient, together with the accuracy of the expression is important to compare simulation result with analytical results and design proof.

4.9.1   Analysis of a Non-Linear Resistive Divider: Introduction

Let us now proceed with describing the procedure to obtain the circuit harmonic responses. The procedure will be explained with a simple example: non-linear resistive divider. The schematic of the resistive divider is shown in Fig. 4.7. To be able to write the node equations, it is necessary to express the terminal equation of the resistors in the form of

$$I_R = f(V_R) = gV_R + K_{2g}V_R^2 + K_{3g}V_R^3 \tag{4.10}$$

---

[22]This expression models output conductance linearly. Therefore, it does not have any distortion component due to the output conductance.
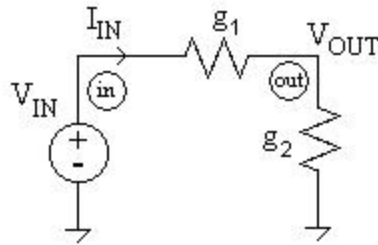
Figure 4.8. Linearized equivalent of non-linear resistive divider
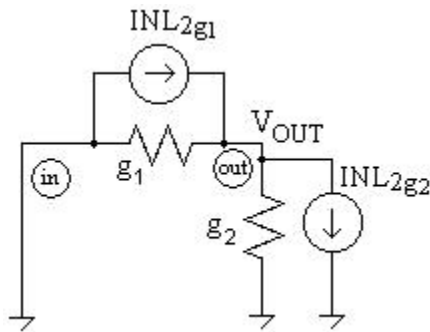
Figure 4.9. Equivalent circuit for the calculation of the second order responses

4.9.2 Linear responses

First step of the non-linear analysis is to find first order responses of the circuit. For this purpose, it is necessary to replace the nonlinear resistor with their equivalent linear conductances (Linear term in the equation 4.10, i.e. g) in Fig. 4.7.

The first order response of the circuit can be calculated easily from the equivalent circuit shown in Fig. 4.8. The notation $V_{x,y}$ will be used to denote the yth order voltage response on node x. Hence, the linear responses are

$$V_{in,1} = V_{IN} \tag{4.11}$$

$$V_{out,1} = \frac{g_1}{g_1 + g_2} V_{IN} \tag{4.12}$$

4.9.3 Second order harmonic responses

To calculate the second order responses, the external excitations should be removed from the equivalent circuit as shown in Fig. 4.9 and the nonlinear current sources of order of two have to be added to the equivalent circuit.

At this point, it is possible to explain the reason why special input sources should be used while SSA Tool runs non-linear analysis. As it is mentioned above, to calculate higher

Table 4.4. Non-Linear second order current sources for the basic non-linear components to compute second harmonics at $2w$. The controlling voltages are V_i for the nonlinear (trans)conductance and nonlinear capacitor and V_i and V_j for two dimensional conductance.

Type of Non-Linearity	Non-linear current source at $2w$
(trans)conductance	$0{\cdot}5K_{2g1}V_{i,1}^2$
Capacitor	$jwK_{2c1}V_{i,1}^2$
Two-dimensional conductance (cross terms)	$0{\cdot}5K_{g1g2}V_{i,1}V_{j,1}$

order responses, the input excitations should be removed. The way this task is done by SSA Tool is that the tool identifies the components whose instance names are **'input'** as the input excitations and nullify their values. Therefore, the instance name 'input' should be used only for voltage and/or current source and for the sole purpose of declaring an input signal for non-linearity analysis.

The cells nonvols and noncurs within Cadence design library SSALIB are designed for this purpose. Four more nonlinear input source cells are also included to SSALIB for intermodulation distortion calculations. The cells named nonvolsw1 and noncursw1 are used to declare input voltage and current signals at w_1 frequency and the cells named nonvolsw2 and noncursw2 are used to declare input voltage and current signals at w_2 frequency. They are identical to regular voltage and current sources, except during netlisting their instance name is replaced with 'input'. It is also possible to use multiple non-linear input sources. Every one of them is nullified during the calculation of the circuit's higher order responses.

The non-linear current sources should be connected in parallel to the linear components in Fig. 4.8. representing related basic non-linear component[23], i.e. conductances g_1 and g_2. The direction of the non-linear current source should be chosen same as the non-linear component control voltage polarity. Fig. 4.9 shows the modified equivalent circuit to calculate second order responses of the circuit.

Solving the equivalent circuit yields to:

$$V_{in,2} = 0 \tag{4.13}$$

$$V_{out,2} = \frac{INL_{2g1} - INL_{2g2}}{g_1 + g_2} \tag{4.14}$$

The values of the non-linear sources are given in Table 4.4.

$$INL_{2g1} = \frac{1}{2}K_{2g1}V_{R1,1}^2 \tag{4.15}$$

---

[23]The main idea behind this modification can be interpreted as follows: the linear analysis considers only the first term of device model equation 4.10 assuming that remaining terms are negligible. This assumption yields to an additive error. The parallel non-linear sources are used to compensate this error under the weakly non-linear circuit operation condition.
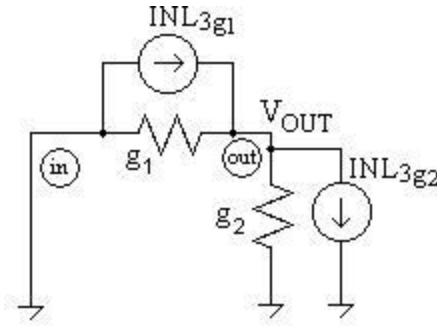
Figure 4.10. Equivalent circuit for the calculation of the third order responses

Table 4.5. Non-Linear third order current sources for the basic non-linear components to compute third harmonics at $3w$. The controlling voltages are V_i for the nonlinear (trans)conductance and nonlinear capacitor, V_i and V_j for two dimensional conductance and V_i, V_j and V_k for three dimensional conductance.

Type of Non-Linearity	Non-linear current source at $3w$
(trans)conductance	$K_{2g1}V_{i,1}V_{i,2} + 0 \cdot 25K_{3g1}V_{i,1}^3$
Capacitor	$3w(K_{2c1}V_{i,1}V_{i,2} + 0 \cdot 25K_{3c1}V_{i,1}^3)$
Two-dimensional conductance (cross terms)	$0 \cdot 5K_{g1g2}(V_{i,1}V_{j,2} + V_{i,2}V_{j,1})$ $+0 \cdot 25K_{32g1g2}V_{i,1}^2V_{j,1} + 0 \cdot 25K_{3g12g2}V_{i,1}V_{j,1}^2$
Three-dimensional conductance (cross terms)	$0 \cdot 25K_{g1g2g3}V_{i,1}V_{j,1}V_{k,1}$

$$INL_{2g2} = \frac{1}{2}K_{2g2}V_{R2,1}^2 \tag{4.16}$$

where control voltages $V_{R1,1}$ and $V_{R2,1}$ can be expressed as

$$V_{R1,1} = V_{in,1} - V_{out,1} = V_{IN} - \frac{g_1}{g_1 + g_2}V_{IN} = \frac{g_2}{g_1 + g_2}V_{IN} \tag{4.17}$$

$$V_{R2,1} = V_{out,1} - 0 = \frac{g_1}{g_1 + g_2}V_{IN} \tag{4.18}$$

Substituting equations 4.15-4.18 in 4.14 yields

$$V_{out,2} = \frac{1}{2}\frac{K_{2g1}g_2^2 - K_{2g2}g_1^2}{(g_1 + g_2)^3}V_{IN}^2 \tag{4.19}$$

4.9.4   Third order harmonic responses

To calculate the third order responses, the equivalent circuit shown in Fig. 4.9 should be modified by just replacing the nonlinear current sources of order of two with the nonlinear current sources of order of three, as shown in Fig. 4.10.

Since the two circuits, Fig. 4.9 and Fig. 4.10. are identical except the values of the non-linear current sources, the same circuit solution can be used to calculate third order response with appropriate modification on the values of the non-linear current sources[24]. Therefore,

$$V_{in,3} = 0 \tag{4.20}$$

$$V_{out,3} = \frac{INL_{3g1} - INL_{3g2}}{g_1 + g_2} \tag{4.21}$$

The values of the non-linear sources are given in Table 4.5.

$$INL_{3g1} = K_{2g1}V_{R1,1}V_{R1,2} + \frac{1}{4}K_{3g1}V_{R1,1}^3 \tag{4.22}$$

$$INL_{3g2} = K_{2g2}V_{R2,1}V_{R2,2} + \frac{1}{4}K_{3g2}V_{R2,1}^3 \tag{4.23}$$

where the control voltages $V_{R1,1}$ and $V_{R2,1}$ are given by 4.17 and 4.18 and the control voltages $V_{R1,2}$ and $V_{R2,2}$ can be expressed as

$$V_{R1,2} = V_{in,2} - V_{out,2} = 0 - \frac{1}{2}\frac{K_{2g1}g_2^2 - K_{2g2}g_1^2}{(g_1 + g_2)^3}V_{IN}^2 = -\frac{1}{2}\frac{K_{2g1}g_2^2 - K_{2g2}g_1^2}{(g_1 + g_2)^3}V_{IN}^2 \tag{4.24}$$

$$V_{R2,2} = V_{out,2} - 0 = \frac{1}{2}\frac{K_{2g1}g_2^2 - K_{2g2}g_1^2}{(g_1 + g_2)^3}V_{IN}^2 \tag{4.25}$$

Substituting equations 4.15,4.16,4.22-4.25 in 4.21 yields

$$V_{out,3} = \frac{1}{4}\frac{(g_1 + g_2)(K_{3g1}g_2^3 - K_{3g2}g_1^3) - 2(K_{2g1}g_2 - K_{2g2}g_1)(K_{2g1}g_2^2 - K_{2g2}g_1^2)}{(g_1 + g_2)^5}V_{IN}^3 \tag{4.26}$$

The linear response expressions (4.11) and (4.12), the second order harmonic response expressions (4.13) and (4.19) and finally the third order harmonic response expressions (4.20) and (4.26) conclude our quest to find the harmonic responses of the non-linear resistive divider shown in Fig. 4.7.

An alternative way of calculating the non-linear responses of the resistive divider starts by drawing the schematic of the non-linear resistive divider in Cadence DFII environment as shown in Fig. 4.11. Then, we extract the spectre(s) netlist using ssatool() skill function as explained previously.

```
* # File name: ~/SSASIMDIR/test_sch/spectreS/schematic/netlist/
# test_sch.c.raw
# Netlist output for spectreS.
# Generated on Aug 13 19:27:11 2003
simulator lang=\spectre
ahdl0 (2) xtfinp tfname=Output option=simp harmonics=3.0
ahdl1 (2 0) nondirenc res=g2 K2g=K2g2 K3g=K3g2
ahdl2 (1 2) nondirenc res=g1 K2g=K2g1 K3g=K3g1
ahdl3 (1 0) nonvols vol=VIN
```

---

[24]Same circuit solution can be used for n^{th} order response also. It is enough to substitute the values of the nth order non-linear current sources in equations 4.13 and 4.14.
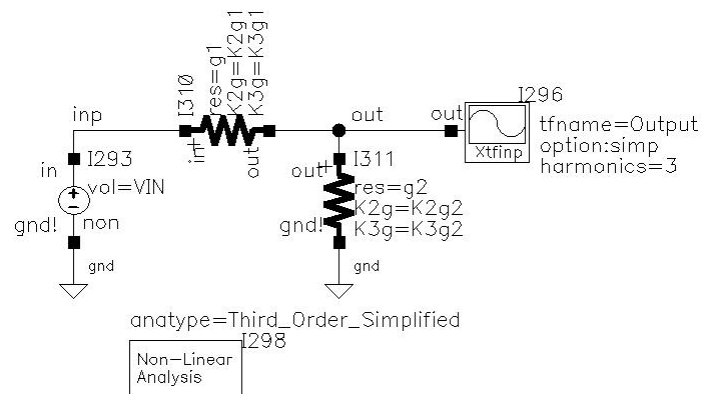
Figure 4.11. Cadence Virtuoso schematic of the non-linear resistive divider

```
ahdl4 ana anatype=Third_Order_Simplified
# Include file for AHDL
# HDL text files to be included for this design.
ahdl_include "~/TEMP/SSALIB/ana/ahdl/ahdl.def"
ahdl_include "~/TEMP/SSALIB/nonvols/ahdl/ahdl.def"
ahdl_include "~/TEMP/SSALIB/nondirenc/ahdl/ahdl.def"
ahdl_include "~/TEMP/SSALIB/xtfinp/ahdl/ahdl.def"
simulator lang=\spice
simulator lang=\spectre
simulator lang=\spice
# Include files
simulator lang=\spectre
# End of Netlist
```

we run the matlab function ssatool() to generate custom SSA Tool netlist and to solve the circuit.

```
% Spectre to SSA Conversion Tool Output
% Written By Devrim AKSIN
% Version 1.
% Last update ConvspectreS   :08-10-2003
% Commercial use is stricly forbidden
% Please contact devrimaksin@ieee.org for info.
% Grounds
{g,glb_ground}
% Description
% Circuit Netlist
{xtf,Output_eq11,1,out_eq11,simp,}
{xtf,Output_eq21,1,out_eq21,simp,}
{xtf,Output_eq31,1,out_eq31,simp,}
{nonres,ahdl1,out,glb_ground,g2,K2g2,K3g2,}
{nonres,ahdl2,inp,out,g1,K2g1,K3g1,}
{vol,input,inp,glb_ground,VIN,}
{ana,thirdsimp}
```

Finally, after couple of second waiting, we can access the following results from the Matlab work space. This path, of course, is much faster, accurate and designer friendly.

$$ssacirsol \cdot eq11 = \begin{bmatrix} out & \dfrac{g_1}{g_1 + g_2}V_{IN} \\ inp & V_{IN} \\ glb\_ground & glb\_ground \end{bmatrix} \tag{4.27}$$

$$ssacirsol \cdot eq21 = \begin{bmatrix} out & \dfrac{1}{2}\dfrac{K_{2g1}g_2^2 - K_{2g2}g_1^2}{(g_1 + g_2)^3}V_{IN}^2 \\ inp & 0 \\ glb\_ground & glb\_ground \end{bmatrix} \tag{4.28}$$

$$ssacirsol \cdot eq31 = \begin{bmatrix} out & \dfrac{1}{4}\dfrac{(g_1 + g_2)(K_{3g1}g_2^3 - K_{3g2}g_1^3) - 2(K_{2g1}g_2 - K_{2g2}g_1)(K_{2g1}g_2^2 - K_{2g2}g_1^2)}{(g_1 + g_2)^5}V_{IN}^3 \\ inp & 0 \\ glb\_ground & glb\_ground \end{bmatrix} \tag{4.29}$$

$$ssacirsol \cdot Output\_eq11 = \frac{g_1}{g_1 + g_2}V_{IN} \tag{4.30}$$

$$ssacirsol \cdot Output\_eq21 = \frac{1}{2}\frac{K_{2g1}g_2^2 - K_{2g2}g_1^2}{(g_1 + g_2)^3}V_{IN}^2 \tag{4.31}$$

$$ssacirsol \cdot Output\_eq31 = \frac{1}{4}\frac{(g_1 + g_2)(K_{3g1}g_2^3 - K_{3g2}g_1^3) - 2(K_{2g1}g_2 - K_{2g2}g_1)(K_{2g1}g_2^2 - K_{2g2}g_1^2)}{(g_1 + g_2)^5}V_{IN}^3 \tag{4.32}$$

The technique is very similar for intermodulation transfer function calculations. Interested reader can found several examples and the table for nonlinear current source values for intermodulation distortion analysis in [60]. For the sake of simplicity, these are not included here.

As a final remark, there are dedicated cells to extract nonlinear transfer functions from the solution space. The cell **xtfHD** is designed to extract second and third order harmonic distortion. The cell **xtfinpim** is the general purpose transfer function definition to extract any calculated nonlinear transfer function.

CHAPTER 5

EXPERIMENTAL RESULTS

In this chapter, the measurement setup and results of the 11 bits Sub-Ranging ADC will be reviewed. I will start with a brief LBC7 process overview and show the ADC silicon die and its partition. Next, I will continue with the test board design details. The measurement instruments, test setup and measurement procedure will follow the board design. And finally, I will finish with the measurement results.

5.1 Technology Overview and the Test Die

The 11 bits Sub-Ranging Analog to Digital converter is fabricated using Texas Instruments $0.35\mu m$ double-poly LBC7 technology. This technology is the extension of TI's 3370A07S process. It contains wide variety of devices to ease high voltage high power system design. The base self-aligned CMOS devices of the process are 3.3V $0.35\mu m$ feature size CMOS transistors. Along with the core transistors, the technology has also 5V and 7V thick gate oxide CMOS transistors. And finally, to ease high-voltage and high power designs, drain-extended MOS transistors and LDMOS transistors are present. The process also has very low sheet resistance copper metal layer option which is very important for power management ICs.

The silicon area of the 11 bit ADC is 560 by 560 μm^2. The die photo is given in Fig. 5.1. The functional blocks are encircled and numbered within the die photo. The numbered sections and their functions are listed below.

1. Input MUX, 8 input channels
2. High-Voltage Rail-to-Rail Passive Subtractor
3. First Stage Comparator
4. Comparator High-Voltage Input Switch & OVST test structures
5. First Stage process flow logic and clock generator circuitry
6. 10 bit Successive Approximation Register Analog to Digital Converter
7. Digital Adder, Test Structures, High-Voltage Digital Interface Circuitry
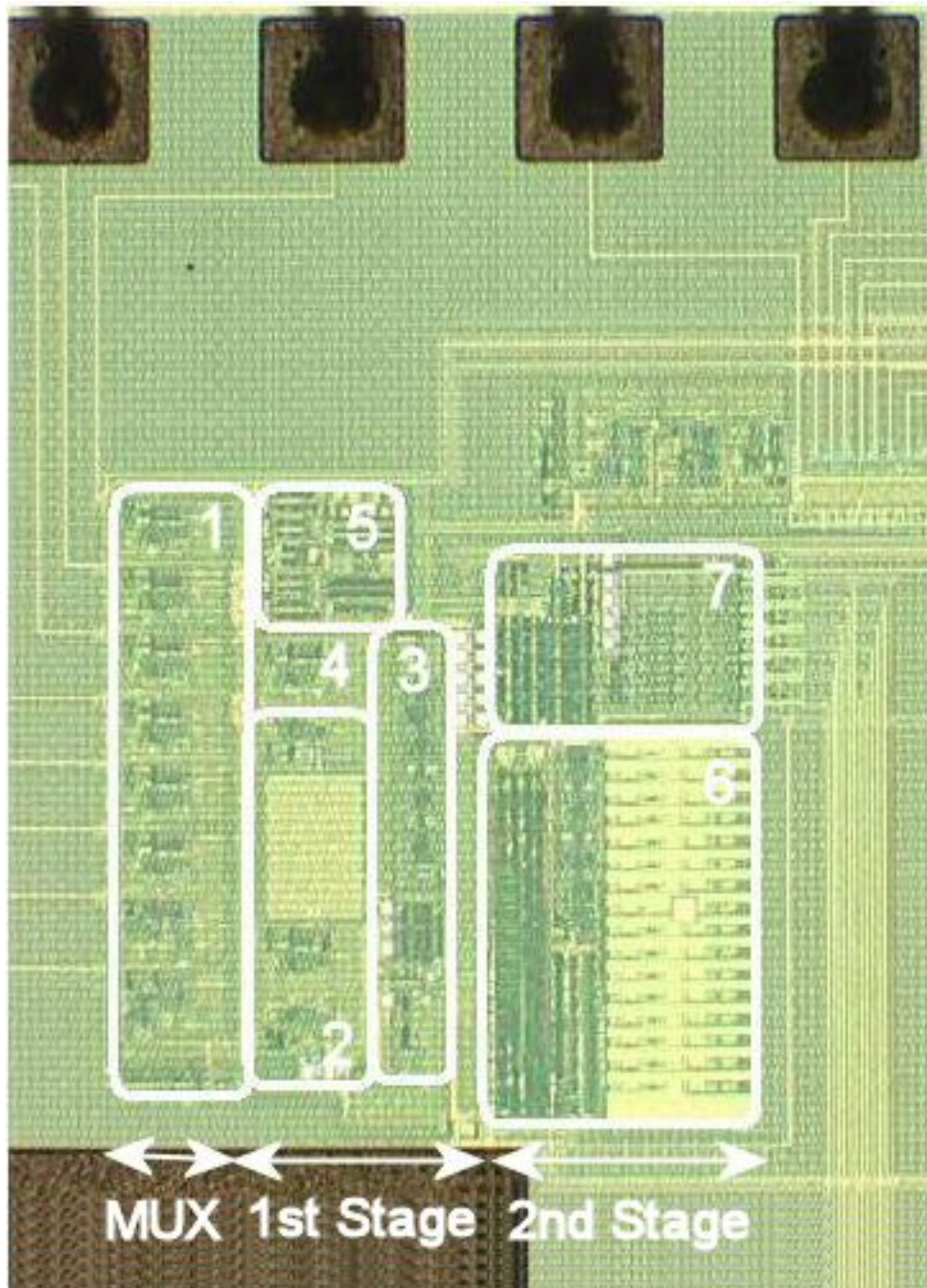
Figure 5.1. Die Photo of 11 bit Sub-Ranging ADC
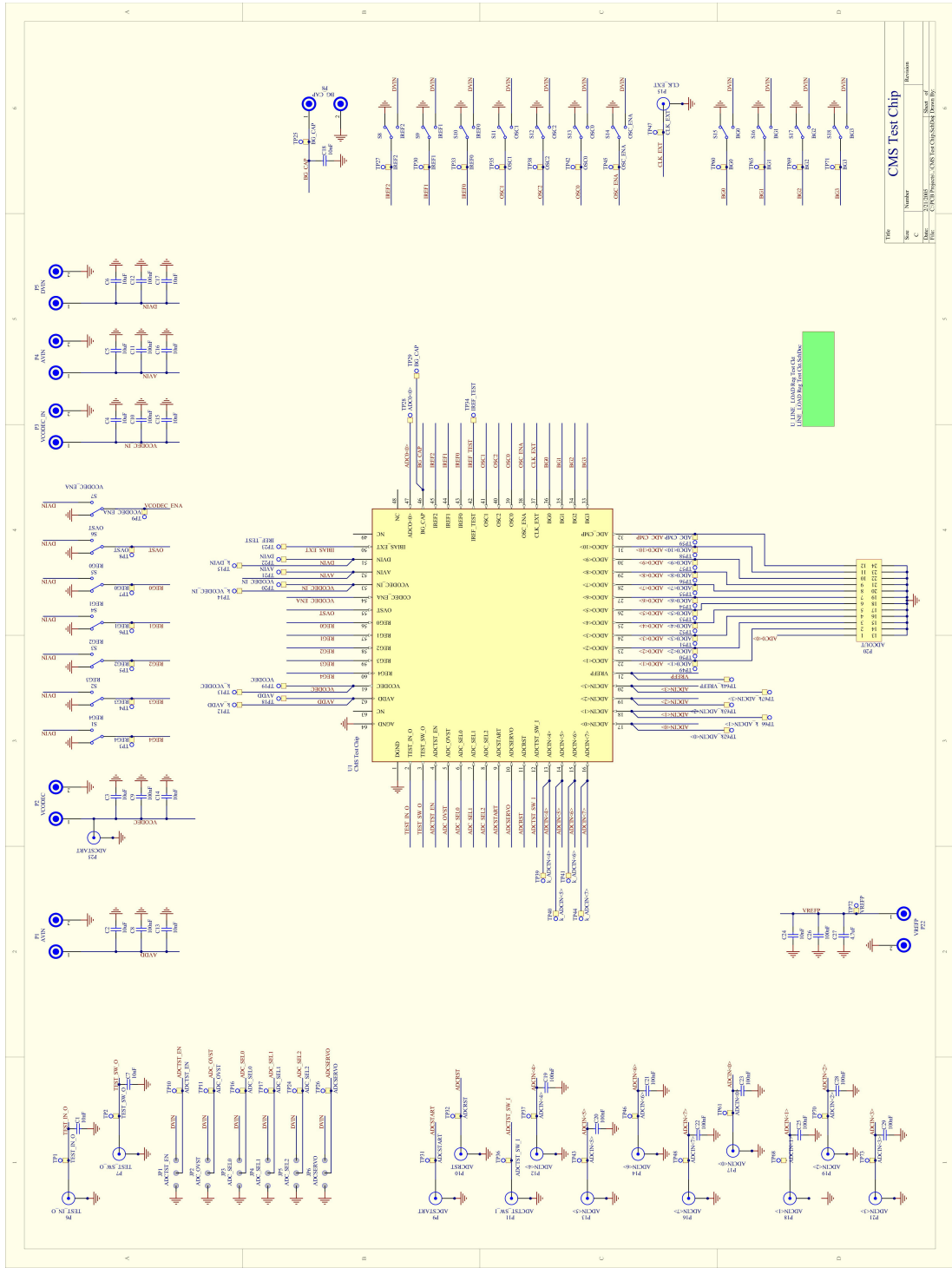
Figure 5.2. PCB Board Schematic
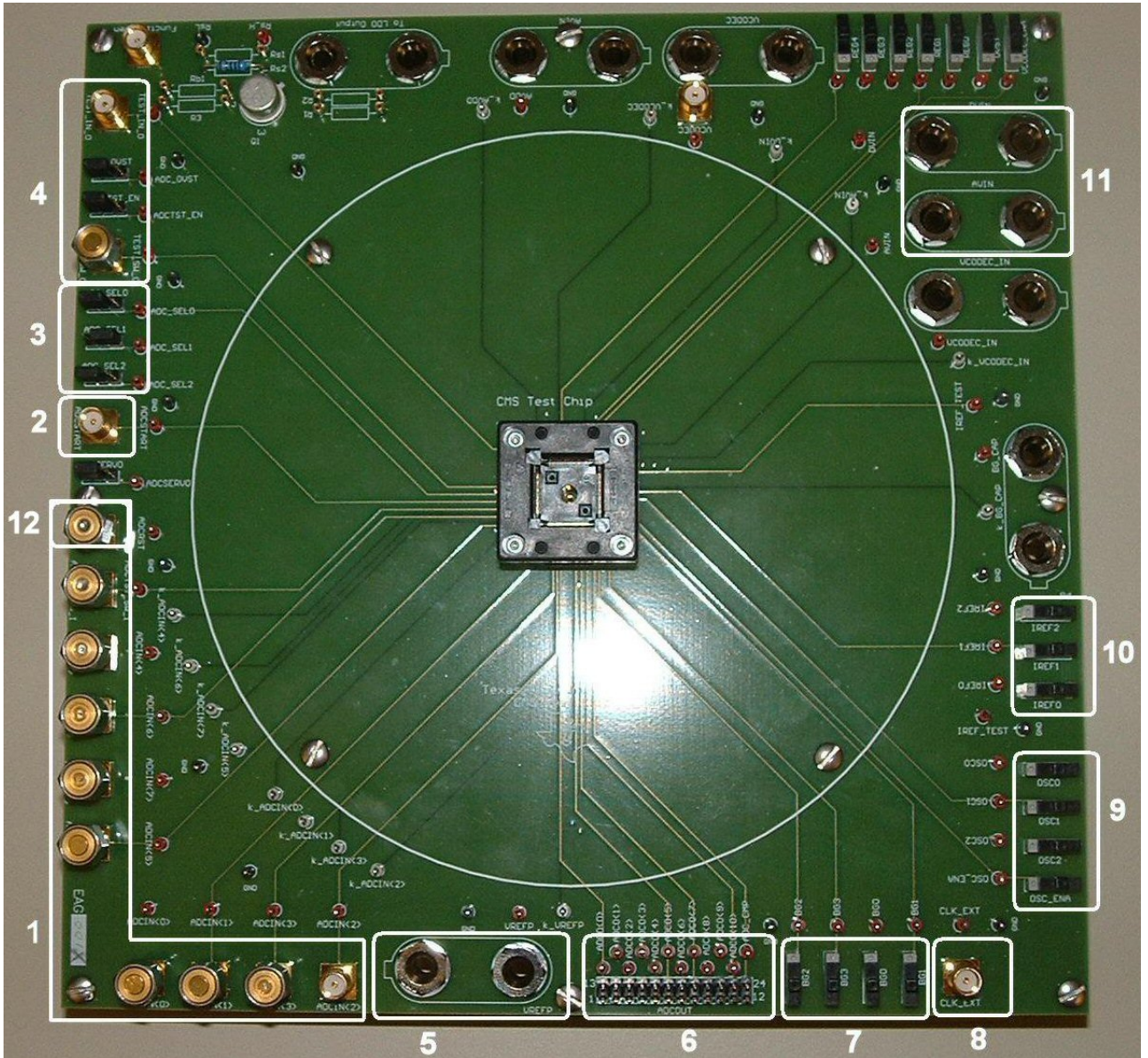
Figure 5.3. PCB Board Photo

5.2 Test board design

The 11 bit ADC, together with other blocks of the power management IC, is enclosed within a 64-pin TQFP package. The pins dedicated to the analog to digital converter are

- 8 analog input channels
- 11 digital output bits and End of Conversion bit
- 3 digital channel select input bits
- Reset and start bits
- Reference voltage pin
- 4 Test related pins

7 of the remaining pins are power pins and the rest are used by the remaining blocks within the systems, i.e. test mode output and test mode select bits, band gap reference and its trim bits, current reference trim bits, oscillator trim bits, voltage regulator outputs and trim bits. The system clock is either provided by the oscillator or from an external pin. The schematic of the designed PCB board is shown in Fig. 5.2. Since the ADC is intended to measure DC signal levels, large decoupling capacitors, i.e. 100nF, are connected to the input channels. The reference voltage pin was also decoupled with large capacitors.

Actual PCB test board photo is shown in Fig. 5.3. Numbered sections of the PCB board are

1. Input Channels
2. ADC start input
3. Channel select bits
4. ADC test mode inputs and bits
5. Reference Voltage Input
6. ADC Output bits
7. Bandgap Voltage Trim Bits
8. ADC clock input
9. Internal Oscillator Trim bits
10. Reference Current Trim bits
11. Digital and Analog Supply
12. ADC Reset bit

Table 5.1. Measurement Instrument List

Instruments	Basic Features	Precision
Keithley 2420	High Precision Source Meter	$40\mu V$
HP 3245A	Universal Source	$10\mu V$
Agilent 6624A	System DC Power Supply	4 channel- 40W
HP 34401A	Multimeter	6.5 digit
Tektronix TLA715	Logic Analyzer and Signal Generator	
Tektronix TDS 5054	Digital Phosphor Oscilloscope	500Mhz BW

5.3 Test Instruments, Setup and Procedure

The list of the instruments used during the measurements are given in Table 5.1. To characterize the converter, first the bandgap reference is trimmed. Next, the current reference is trimmed to provide proper bias current to the converter's comparators and to the build-in oscillator. And finally, the oscillator is trimmed when the board clock is used.

Since the ADC is designed to measure DC signals, i.e. battery voltage, the converter is characterized with DC signals. The input signal is supplied by a Keithley 2420 high precision source meter. This instrument is capable of generating DC input signals with $40\mu V$ resolution. The Tektronix TLA715 signal generator generates a trigger signal for Keithley 2420 to start 100 mV sweep and then starts the conversion process. Keithley 2420 can provide $40\mu V$ resolution only for 100mV or less voltage sweeps. This is the reason for the sweep range selection.

The logic analyzer that is again Tektronix TLA715 captures the output code while input signal is swept. Data capture is triggered with end of conversion signal generated by the converter. After multiple conversions, the process restarts again with the trigger signal of the input source. The characterization ends whenever the input signal source sweeps entire input signal range. The test procedure flow diagram is shown in Fig. 5.4.

The test setup is illustrated in Fig. 5.5. The supply voltage is provided by Agilent 6624A DC power supply. The reference voltage is provided to the system from HP3245A as well as from the on chip low drop out linear voltage regulator. The data captured by the Logic Analyzer is then analyzed using Matlab to extract differential and integral nonlinearity of the converter.

The input stage of the converter and in particular the passive subtractor circuit is also tested separately. One of the embedded test mode allows to access the first stage output from a test pin. In order to characterize the passive subtractor staircase input signal is
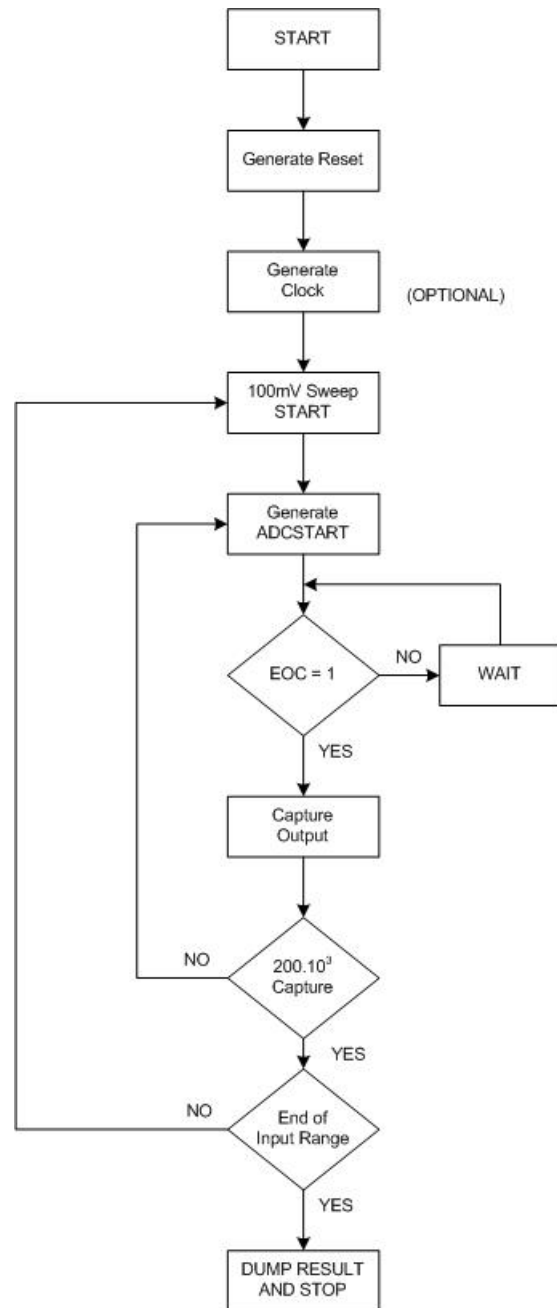
Figure 5.4. Test Procedure
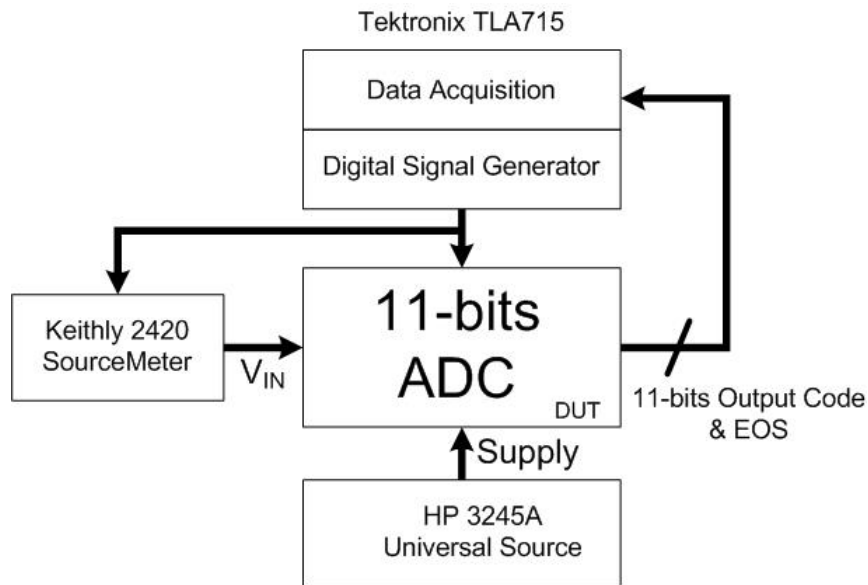
Figure 5.5. Test Setup

applied to the selected input channel and input signal minus the reference voltage will be observed from the output as shown in Fig. 3.20.

To be able to characterize the HVB switch, all three versions[1] of the high-voltage bootstrapped switch are also integrated separately. By properly selecting the test mode, the terminals of those switches can be made accessible through the test pins. A sine wave is applied to the input of the switches and the input signal is sampled onto the parasitic input capacitance of the oscilloscope probe and this waveform is observed from the oscilloscope. Due to the heavy capacitive load created by the probe, this test is rather a functional test. Therefore, the dynamic characterizations of the switches are not done.

5.4   Measurement Results

The measurement data are collected from 18 sample IC. All of the measured IC are functional. The bandgap reference has two sets of trim bits. One set is used for temperature trim and the second set is used for voltage trim. The output is set to 1V. The untrimmed output voltages of all measured bandgap references are shown in Fig. 5.6. The average output voltage is 1.050V.

---

[1]The one presented within chapter 3 and the remaining two shown in Appendix E.
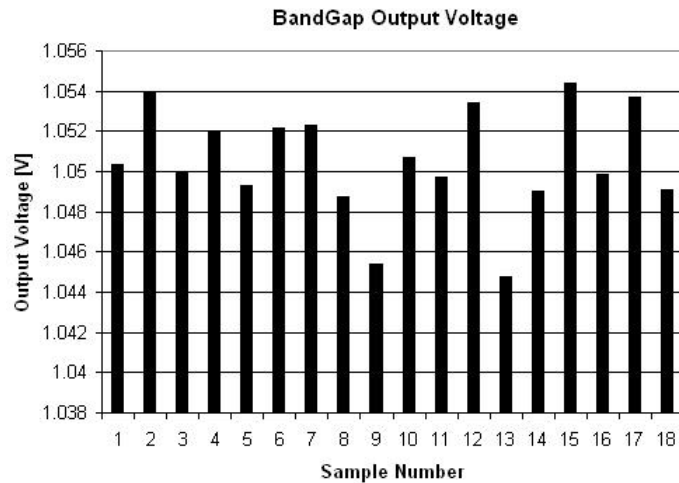
Figure 5.6. Measured Untrimmed BandGap Voltages with respect to sample number.

5.4.1 High-Voltage Bootstrapped Switch

The HVB switches are measured separately. For this purpose, the input of the switches are driven with a sinusoidal wave and this waveform is sampled. The experiment is exactly same as observing the output of a simple track and hold circuit made of a hold capacitor and a pass transistor. The hold capacitor here is the load capacitor of the oscilloscope probe. The equivalent load of the active probe is 2pF//1MOhm. All three versions of the HVB switch operates properly for 2.75V supply voltage and 0-5.5V input signal range. First and second implementation versions[2] can operate with supply voltage level down to 1.9V and the third version presented in section 3.3 can operate with supply voltage level down to 1.2V. The measurement results showing the operation of the HVB switch for 2.75V supply level and 1.2V supply level are given in Fig. 5.7 and Fig. 5.8. respectively. The results are as expected for 2.75V supply voltage case. This is the supply voltage level for which the switch is optimized.

The pass transistors of the HVB switches are not optimized to operate with large load capacitor and a low supply voltage level such as 1.2V. Therefore, during the second measurement the input signal frequency and the sampling frequency has to be decreased substantially. The hold phase is not apparent in the figure. This is due to the input leakage of the oscilloscope probe discharging the output node. While the input signal reaches to 6V, the output signal cannot follow the input due to the reduced gate voltage as a result of the capacitive division.

---

[2]First and second versions are presented in Appendix E
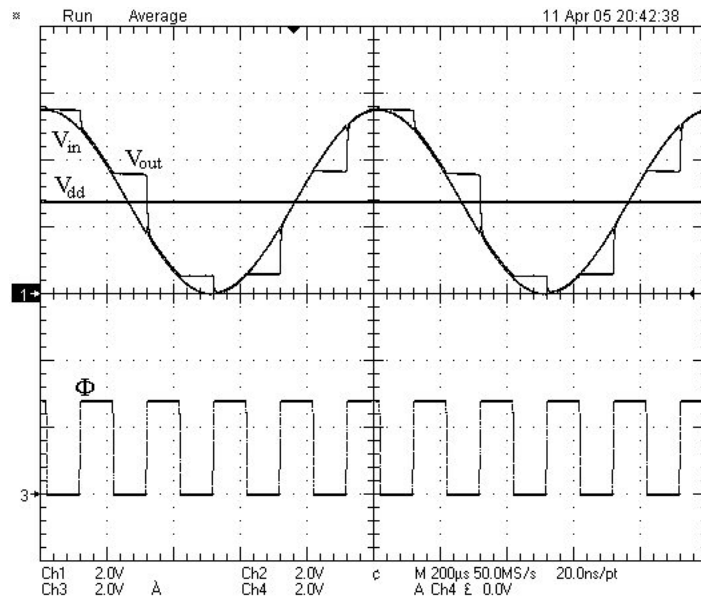
Figure 5.7. Measurement result of the High-Voltage Bootstrapped Switch for maximum $V_{IN} = 5{\cdot}5V$ and $V_{dd} = 2{\cdot}75V$
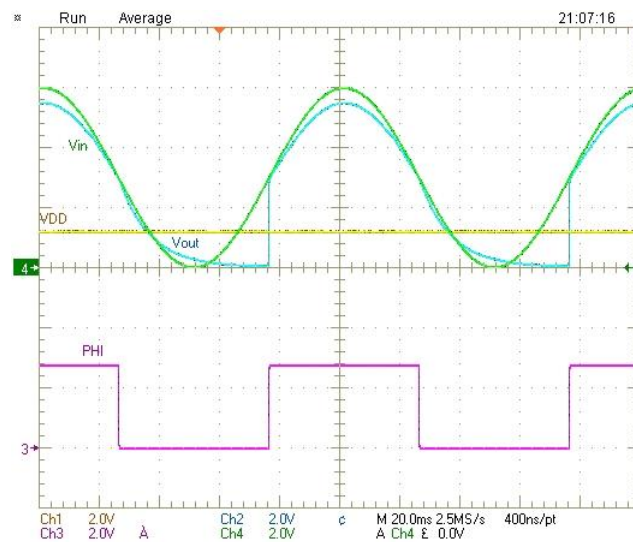
Figure 5.8. Measurement result of the High-Voltage Bootstrapped Switch for maximum $V_{IN} = 6V$ and $V_{dd} = 1{\cdot}2V$
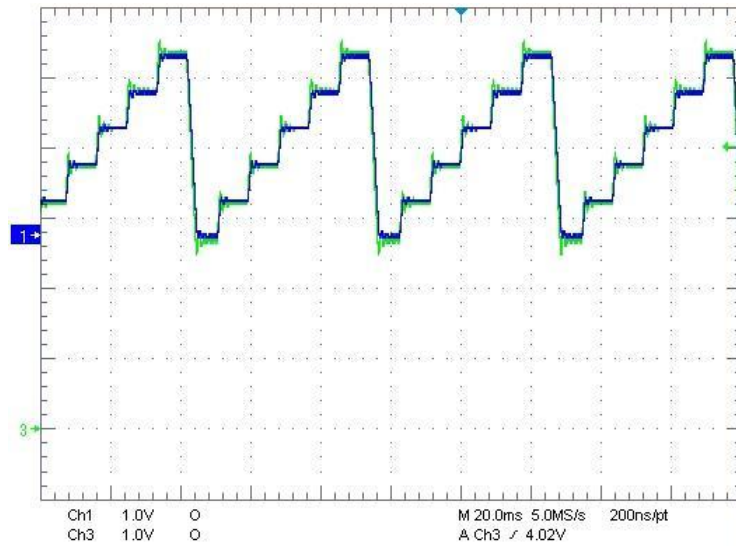
Figure 5.9. Measurement result of the High-Voltage Bootstrapped Switch for maximum $V_{IN} = 5 \cdot 5V$ and $V_{dd} = 2 \cdot 75V$

5.4.2 High-Voltage Passive Subtractor

The output of the first stage can be observed through the test pin with proper test mode setting. Hence, it is possible to test functionally the high-voltage passive subtractor block. A staircase input signal is applied to the selected input channel and the output of the first stage is observed. Of course, the input signal is chosen greater than the reference voltage (supply voltage) all the time so that the passive subtractor block starts operating.

Fig. 5.9 shows the input and output signals. DC signal shift is apparent from the reference voltage level signs of the two channels at left side of the figure. Notice that the ringing of the input signal is attenuated at the output of the passive subtractor. This is due to the low-pass filtering of the block.

During the measurements, the IC latched-up occasionally. This is because of the fact that the output of the first stage is high impedance and during this test mode the high-impedance first stage output is connected directly to the output pin. Latch-up condition never happened during regular measurement of the analog to digital converter.

5.4.3 11 bit Sub-Ranging ADC Performance

Since the converter is designed to operate with very low input signal frequencies, i.e. DC, only static linearity characterization of the ADC is done. After properly trimming the bandgap voltage, bias currents and the reference voltage, the input signal was swept across the input signal range (0-5.5V) with 100mV subranges while the converter operated and the number of hits of each output code was stored. The input source has $44\mu V$ output voltage resolution
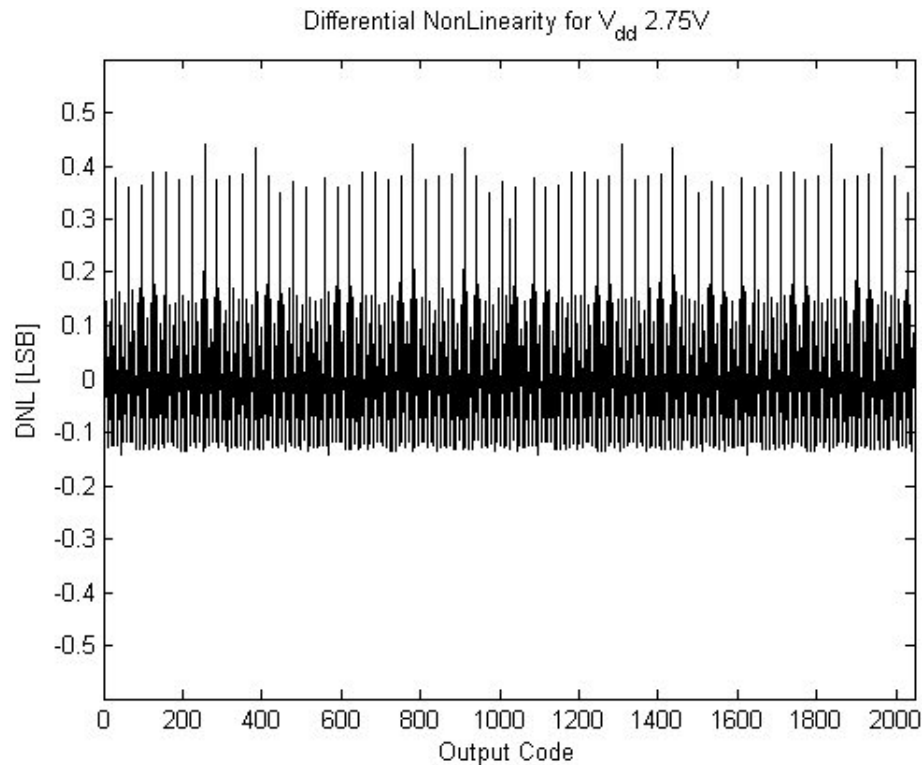
Figure 5.10. Differential Nonlinearity of the 11 bit Sub-Ranging ADC

within 100mV signal range. This procedure is detailed in section 5.3. Extracted numbers of hits of each code are then processed with Matlab to obtain the differential nonlinearity of the 11 bit Sub-Ranging ADC.

The differential nonlinearity of the converter is extracted from the normalized deviation of the individual hit of every output code with respect to the average hit per code, as shown by eq. 5.1.

$$DNL(code) = \frac{Code\ Hit - Average\ Hit}{Average\ Hit} \tag{5.1}$$

The integral nonlinearity is the cumulative sum of the DNL vector. The DNL plot of the converter is shown in Fig. 5.10. The INL plot of the converter is shown in Fig. 5.11. The jump of the INL curve at the mid of the input signal range shows the effect of the passive subtractor block. The DNL and INL of the 11-bit ADC is $0{\cdot}45LSB$ and $0{\cdot}38LSB$, respectively.

The converter draws a total of $120\mu A$ current from 2.75V analog and digital supply. The reference voltage current is around $20\mu A$ with a 2MHz clock frequency[3]. Finally the input current is less than $5\mu A$. The shoot through current of the level-shifter structure within the high-voltage bootstrapped switch is the dominant cause of the input current. Relatively high reference voltage current is due to large shoot through current of the passive subtractor due

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[3]To measure the reference terminal current, the reference voltage is provided externally.
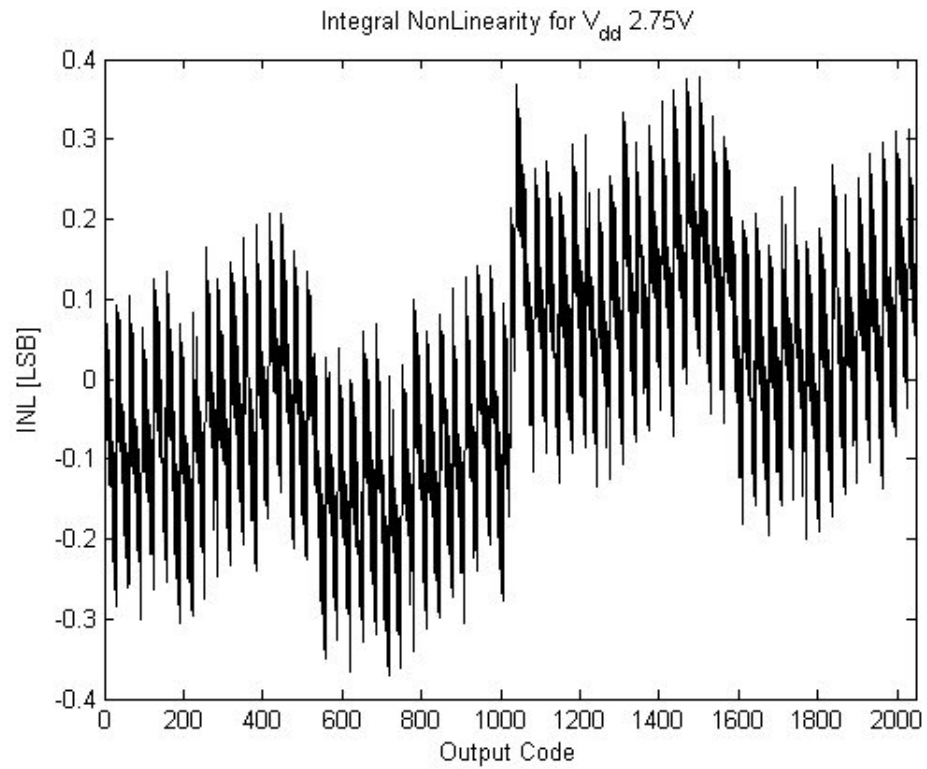
Figure 5.11. Integral Nonlinearity of the 11 bit Sub-Ranging ADC

to the heavy capacitive load. The current measurement data clearly proves that the parasitic body diodes are not forward biased during the operation.

Table 5.2 summarizes the performance and the features of the 11 bit Sub-Ranging Analog to Digital converter.

Table 5.2. Performance Summary of 11 bit Sub-Ranging Analog to Digital Converter

Parameter	Value	Unit	Note
Supply Voltage	2.75	V	Operates down to 1.8V
Reference Voltage	2.75	V	Equal to V_{dd}
Input Signal Range	5.5	V	Equal to $2V_{REF}$
Input Signal Bandwidth	DC	Hz	
Number of Input Channel	8	-	
Conversion Time	< 10	μs	$< 5\mu$s for $V_{IN} \leq V_{REF}$
System Clock Frequency	2	MHz	
Resolution	11	bit	
LSB	2.688	mV	
DNL	0.45	LSB	
INL	0.38	LSB	
Supply Voltage Current	120	μA	
Reference Voltage Current	20	μA	
Input Pin Current	5	μA	
Silicon Area	560$\times$ 560	μm^2	
Technology	LBC7 $0{\cdot}35\mu m$ CMOS		

CHAPTER 6

SOFTWARE VALIDATION

6.1 Introduction

This chapter is organized to prove the efficiency of the SSA Tool using examples. The goal is not a detailed and complete analysis of the presented circuits but it is to define the different analysis needs and to show how to use the tool to obtain these results. Therefore, repetitive analyses will be skipped for the sake of brevity. The chapter contains 4 examples, two $\Sigma\Delta$ modulator with different architecture and complexity, one example shows the nonlinear analysis of a linear circuit, i.e. emitter follower and finally one example showing the efficiency of the tool for linear analysis.

The symbolic analysis of a very complex $\Sigma\Delta$ modulator structure will be given in section 6.2. The modulator consists of 3 discrete-time integrators, 1 discrete-time adder, 4 multi-bit quantizer and therefore feedback DAC, digital differentiator. This is a 2-1 MASH Time-Interleaved $\Sigma\Delta$ modulator. Since the modulator is multi-rate, the modulator up-sampled output is obtained by combining the outputs using post-processing module.

The analysis of a 4th order $\Sigma\Delta$ modulator will be presented in section 6.3. The main design issues for higher order single bit modulator are the stability and the sensitivity of the modulator. The transfer function of the modulator together with its stability and sensitivity analysis can be found in this section.

This tool is used extensively while optimizing and analyzing the distortion performance of switched emitter follower (SEF) structure that is a very popular circuit to implement high-speed and linear track and hold amplifier. Section 6.4 provides the use of the tool while analyzing basic emitter follower circuit which is the core of the SEF and how to evaluate the analysis results and compare them with the numerical simulation results.

Finally, the linear analysis of the preamplifier of the comparator used within the 11 bits sub-ranging analog to digital converter is given in section 6.5 to show the efficiency of the tool in linear analysis.

6.2 Example : Analysis of the 2-1 MASH Time Interleaved $\Sigma\Delta$ Modulator

The Simulink schematic of the 2-1 MASH Time-Interleaved $\Sigma\Delta$ modulator is shown in Fig. 6.1. This complex multi-bit modulator is suitable to obtain large signal bandwidth
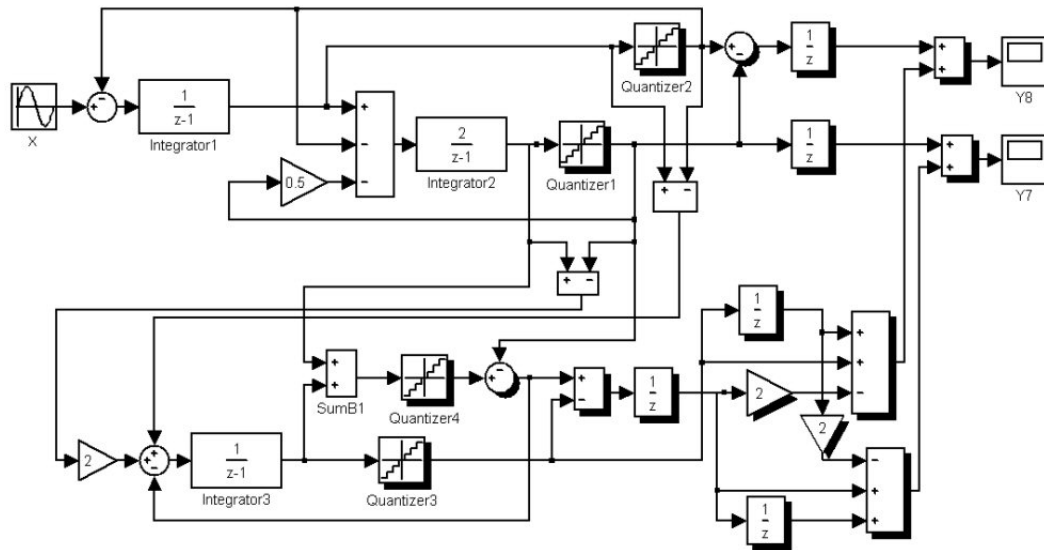
Figure 6.1. 2-1 Mash Time Interleaved $\Sigma\Delta$ Modulator Schematic

and resolution with low over sampling ratio[1] (OSR). Since the modulator architecture is 2-1 MASH, it is inherently stable.

The modulator has two outputs, i.e. Y_7 and Y_8. Since, this is a multi-rate system, the outputs should be up-sampled and combined. Up-Sampling of a signal N times is equivalent to replacing the discrete-time frequency variable z with z^N. Of course, the variable N for this system is 2.

The up-sampling transformation can be achieved only using post-processing module because of the fact that the symbolic solver assumes that the definition of the variable z is the same for all the blocks within the system. The following post-processing code is used to generate the output signal.

```
% This is a postprocessing file
% The circuit solution equations should start with ssacirsol
syms z
Y7=subs(ssacirsol.Y7_eq11,z,z^2);
Y8=subs(ssacirsol.Y8_eq11,z,z^2);
Y=(Y8/z+Y7)/2;
```

The output signal of the modulator is Y. The modulator has 4 multi-bit quantizers. While evaluating the symbolic expressions for numerical comparison purpose, the quantizer step sizes are chosen 0.25 of full scale input signal for ϵ_1 and ϵ_2, 0.125 of full scale input signal for ϵ_3 and ϵ_4. Finally, the over sampling ratio of the system is equal to 20. Let us now proceed with the analysis of the system.

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[1]Or equivalently, with low clock frequency.

6.2.1 Output Signal and In Band Noise Power

The output of the ideal modulator is given in equation 6.1. Of course, this is the most important expression. Throughout the different analyses, the output signal will reveal the effect of different non-idealities introduced. As it is apparent, the quantization noise signals of Quantizer1 and Quantizer2 are fully canceled at the output. Only, the quantization noise signals of the cascade stage, i.e. Quantizer3 and Quantizer4, are present at the output. As expected, the modulator has third order noise shaping.

$$Y(z) = \frac{1}{2}z^{-5}X(z) + \frac{1}{2}z^{-1}(1 - z^{-1})^3(\epsilon_3 + z^{-1}\epsilon_4) \tag{6.1}$$

The $\Sigma\Delta$ modulator analysis module extracts the ideal modulator's in band quantization noise power

$$P_Q = 10\log\left(4\frac{\Delta^2}{12}\frac{\pi^6}{7}\frac{1}{OSR^7}\right) = 10\log\left(4\frac{0{\cdot}125^2}{12}\frac{\pi^6}{7}\frac{1}{20^7}\right) = -92{\cdot}5 \ dB \tag{6.2}$$

Notice that the in band noise power is multiplied by 4 instead of 2 because ϵ_3 and ϵ_4 are correlated[2].

6.2.2 Voltage Swing of the Internal Nodes

In terms of circuit implementation, there are 3 kinds of signals whose swing is important. These are

1. analog signals at the amplifier outputs (integrators and summing blocks),
2. analog feedback signals at the output of the digital to analog converters,
3. digital signal at the output of the quantizers

It is highly desirable for all these signals to have small magnitude. From the amplifier design point of view, it is important because large swing means longer settling time, higher non-linearity, tighter constraints to achieve required small signal gain, etc... From DAC converter design point of view, large signal swing[3] yields to a higher DAC resolution. Finally, from quantizer design point of view, the swing sets required number of comparators.

The signal swing of each node is accessible through the symbolic solver output variable ssacirsol.eq11 . This variable may become quite large and unreadable for large systems. An alternative way is to extract these signals using Scope blocks[4].

Example:

The voltage swing at the output of the analog summing block (sumB1)

$$O_{SUM} = -z^{-1}(2\epsilon_1 + 3\epsilon_2 + \epsilon_4) \tag{6.3}$$

---

[2]Both of the noise signal is substituted with Δ
[3]Since the quantization step size is fixed
[4]Exactly the same technique used to extract the output signals Y_7 and Y_8

The voltage swing of the digital summing block at the output of fourth quantizer

$$O_{SUMD} = \epsilon_4 - \epsilon_1 - z^{-1}(\epsilon_4 + \epsilon_1 + \epsilon_2) \tag{6.4}$$

6.2.3 Noise analysis of the system

While optimizing the $\Sigma\Delta$ modulator, it is important to extract the sensitivity of the modulator performance to the noise signals injected at different nodes. This information is needed for example to determine the shielding strategy of the sensitive nodes during the system layout or to optimize power consumption of different amplifiers within the system, since it is possible to trade noise with power consumption.

The noise signal can be modeled additive, since it is small in magnitude. Therefore, in order to analyze the noise sensitivity of a node, it is enough to connect a summing block to that specific node and add the noise signal V_N[5].

Example: The output of the modulator, while a noise source V_N is present at the input of the second integrator, can be expressed as:

$$Y(z) = \frac{1}{2}z^{-5}X(z) + z^{-4}(1 - z^{-1})V_N + \frac{1}{2}z^{-1}(1 - z^{-1})^3(\epsilon_3 + z^{-1}\epsilon_4) \tag{6.5}$$

As it is obvious, the noise signal is filtered with first order noise shaping function. Therefore, its power is attenuated by 20dB at the modulator output. As expected, the most noise sensitive block of this structure is the input of the first integrator because the noise signal appears at the output without any noise shaping, exactly same as the input signal, as it is clear from equation 6.6.

$$Y(z) = \frac{1}{2}z^{-5}[X(z) + V_N] + \frac{1}{2}z^{-1}(1 - z^{-1})^3(\epsilon_3 + z^{-1}\epsilon_4) \tag{6.6}$$

It is possible to verify with this analysis that the noise contribution of only first integrator will dominate at the output of the modulator. There is no need to optimize other amplifiers within the system for noise performance.

6.2.4 The effect of the finite amplifier gain

To determine the effect of the amplifier finite gain, the ideal integrator function

$$V_{O\_INT}(z) = \frac{K}{z - 1} \tag{6.7}$$

where K is the integrator gain, should be modified. There are several work presented in the literature deriving equivalent z-domain transfer function of the discrete-time integrator

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[5]Exactly same model that we use for quantizer block

having an amplifier with finite small signal gain. In this analysis, the following non-ideal z-domain transfer function will be used:

$$V_{O\_INT}(z) = \left[1 - \frac{b}{A}\right] \frac{K}{z - \left[1 - \frac{c}{A}\right]} \tag{6.8}$$

where A is the finite amplifier gain and the parameters c and b changes between 1-2 and 2-3 times of the integrator gain. The details of the derivation can be found in appendix A.1.

In order to analyze the effect of the finite amplifier gain, the ideal integrators of the system will be replaced with the transfer function shown in (6.8). The non-ideal transfer function will create extra noise terms at the output of the modulator. From these extra terms, the degradation of the modulator signal to noise ratio will be extracted, as defined in appendix B.

Example: The second integrator is replaced with its non-ideal equivalent. The SSA Tool gives the following expression as the modulator output:

$$Y(z) = \frac{1}{2}\frac{X}{z^5} + \frac{1}{2}\frac{(z-1)^3}{z^4}\epsilon_3 + \frac{1}{2}\frac{(z-1)^3}{z^5}\epsilon_4 + \underbrace{\frac{b_2 z^2 - b_2 + c_2}{z^5(A_2 z^2 - b_2 + c_2)}(z-1)(\frac{1}{2}\epsilon_1 + \epsilon_2)}_{ExtraTerm} \tag{6.9}$$

Since in general, the small signal gain A_2 is much bigger than both b_2 and c_2, it is possible to further simplify 6.9:

$$Y(z) = \frac{1}{2}\frac{X}{z^5} + \frac{1}{2}\frac{(z-1)^3}{z^4}\epsilon_3 + \frac{1}{2}\frac{(z-1)^3}{z^5}\epsilon_4 + \underbrace{\frac{1}{2}\frac{b_2(z+1)(z-1) + c_2}{z^7 A_2}(z-1)(\epsilon_1 + 2\epsilon_2)}_{ExtraTerm} \tag{6.10}$$

First three terms of the equation (6.10) is the ideal transfer function of the modulator and due to the finite gain of the amplifier, an extra fourth term appears at the output. The extra term is a function of the quantization noise signals of Quantizer1 and Quantizer2[6]. It is possible to separate this extra term to two separate terms: First one is filtered with second order noise shaping and the second one is filtered with first order noise shaping. The SNR degradation extracted by the SSA Tool is

$$\Delta SNR = -10\log\left[1 + \frac{7}{5}\left(\frac{6b_2}{A_2}\right)^2\left(\frac{OSR}{\pi}\right)^2 + \frac{7}{3}\left(\frac{3c_2}{A_2}\right)^2\left(\frac{OSR}{\pi}\right)^4\right] \tag{6.11}$$

Notice that ϵ_1 and ϵ_2 are correlated noise signals. Since the integrator gain is 2, the parameter b_2 changes within the range 3-5 and the parameter c_2 changes within the range 2-4. Substituting the system parameter within equation (6.11) shows that less than 3dB SNR degradation requires more than 57dB small signal gain from the second integrator's amplifier. Comparison of the Simulink simulations with the analytical model describing the SNR degradation due to the second integrator's amplifier finite small signal gain is given in Fig. 6.2.

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[6]Normally they should be canceled by the cascade stage.

Figure 6.2. Comparison of the Simulink Simulation Results with the Analytical Expression modeling the effect of the second Integrator's Amplifier Finite DC Gain

The comparison results are quite satisfactory. Required minimum DC gain of each amplifier within the system including the amplifier of the summing block can be extracted with this method.

6.2.5 The effect of the Integrator Gain Error, Amplifier Linear Settling error and Non-Zero On-Resistance of the MOS Switches:

All three of the error types mentioned above introduce gain error to the ideal discrete-time integrator transfer function. Therefore, the ideal transfer function given in (6.7) should be modified as follows:

$$V_{O\_INT}(z) = [1 - b] \frac{K}{z - 1} \tag{6.12}$$

where the parameter b represents the gain error. Of course, it is possible to relate this parameter to the unity gain bandwidth, Integration capacitor mismatch or switch on resistance using appropriate equations. The integration capacitor mismatch can be directly extracted from b. The derivation of the unity gain bandwidth and switch on resistance is given in appendixes C and D, respectively.

We will follow the same path that we used for the analysis of the effect of the finite amplifier gain. The ideal integrators of the system will be replaced one by one by the transfer function shown in (6.12). The non-ideal transfer function will create extra noise terms at the output of the modulator. From these extra terms, the degradation of the modulator signal to noise ratio will be extracted.

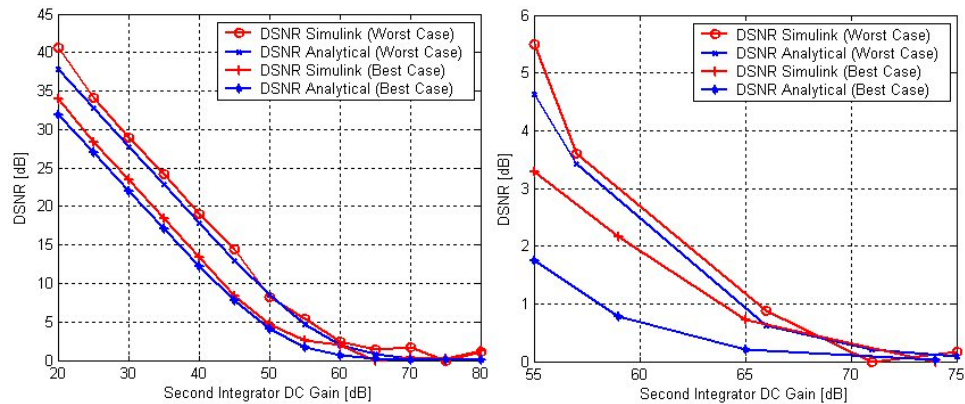Example: The second integrator transfer function is replaced with its non-ideal equivalent
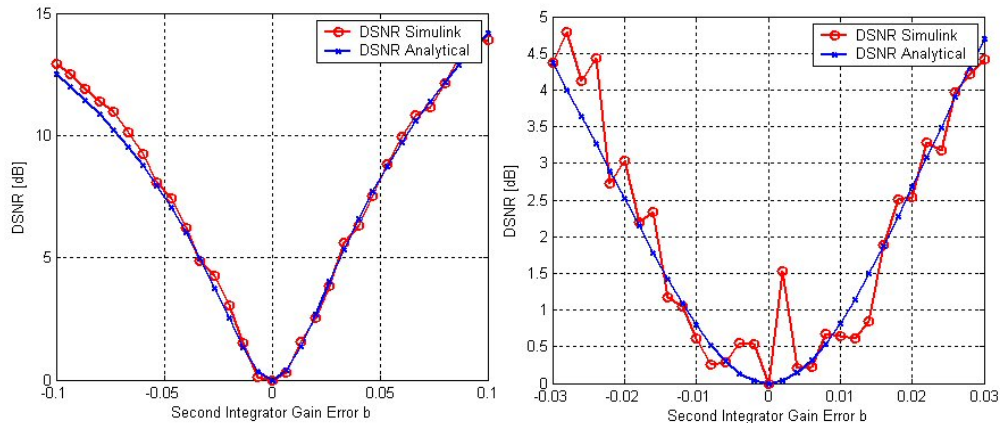
Figure 6.3. Comparison of the Simulink Simulation Results with the Analytical Expression modeling the effect of the second Integrator's Gain Error

within the system. This modification yields

$$Y(z) = \frac{1}{2}\frac{X}{z^5} + \frac{1}{2}\frac{(z-1)^3}{z^4}\epsilon_3 + \frac{1}{2}\frac{(z-1)^3}{z^5}\epsilon_4 + \underbrace{\frac{1}{2}\frac{b_2(z+1)(z-1)^2}{z^5(z^2-b_2)}(\epsilon_1 + 2\epsilon_2)}_{ExtraTerm} \qquad (6.13)$$

The SNR degradation extracted by SSA Tool from equation 6.13 is

$$\Delta SNR = -10\log\left[1 + \frac{7}{5}\left(\frac{6b_2}{1-b_2}\right)^2\left(\frac{OSR}{\pi}\right)^2\right] \qquad (6.14)$$

Substituting system parameters in (6.14) shows that less than 3dB SNR degradation requires b_2 to be less than 0.02. Comparison of the Simulink simulations with the analytical model describing the SNR degradation due to the second integrator's amplifier settling error is given in Fig. 6.3.

6.2.6   The effect of the Imbalance among the Input Branches

The integrator gain error analysis done previously models only the mismatch at the integration capacitance, hence it does not take into the consideration sampling capacitor mismatches leading to the imbalance between the input branch coefficients. To model the imbalance created by the mismatch at the sampling capacitance, a gain stage is cascaded with that input branch and the gain is set to $(1-b)$. The results of this analysis will allow determining the criticality of the matching between the integration capacitance and the sampling capacitance of a given integrator input.

Example: As an example, we will analyze the effect of the imbalance introduced to the third integrator's fifth input[7]. The rational behind this selection is to show the efficiency of the

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[7]Gain block is connected in between the output of the Digital Subtractor at the output of the Quantizer 4 and the third integrator.
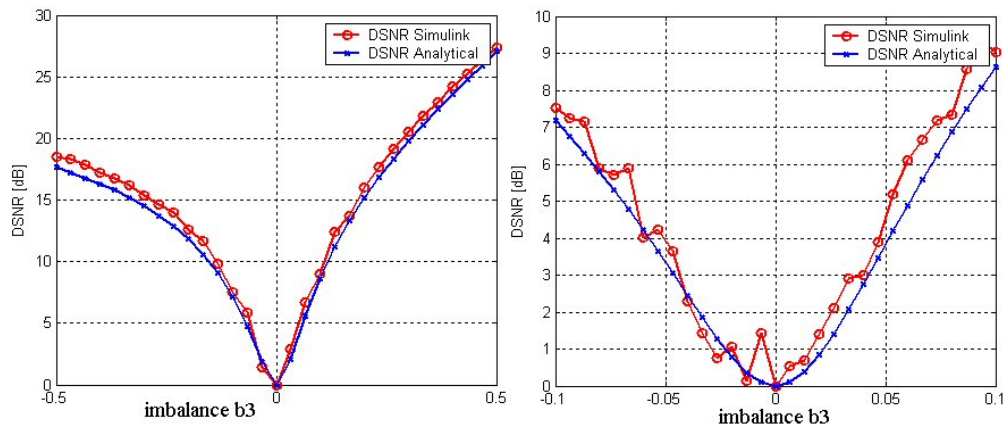
Figure 6.4. Comparison of the Simulink Simulation Results with the Analytical Expression modeling the SNR degradation due to the imbalance introduced by b_3

tool handling complex equations. After the introduction of the imbalance, the output of the modulator is modified as

$$Y(z) = \frac{1}{2}\frac{X}{z^5} + \frac{1}{2}\frac{(z-1)^3}{z^4}\epsilon_3 + \underbrace{\frac{1}{2}\frac{(z+b_3)(z-1)^3}{z^4(z^2-b_3)}\epsilon_4}_{ModifiedTerm} \underbrace{-\frac{1}{2}\frac{b_3(z^2+1)(z-1)^2}{z^5(z^2-b_3)}\epsilon_1 - \frac{1}{2}\frac{b_3(z-1)^2}{z^5(z^2-b_3)}\epsilon_2}_{ExtraTerms} \qquad (6.15)$$

Assuming that $b_3 >> 1$, equation (6.15) can be simplified to

$$Y(z) = \frac{1}{2}\frac{X}{z^5} + \frac{1}{2}\frac{(z-1)^3}{z^4}\epsilon_3 + \frac{1}{2}\frac{(z-1)^3}{z^5}\epsilon_4 + \underbrace{\frac{1}{2}\frac{b_3(z+1)(z-1)^3}{z^7}\epsilon_4 - \frac{1}{2}\frac{b_3(z^2+1)(z-1)^2}{z^5(z^2-b_3)}\epsilon_1 - \frac{1}{2}\frac{b_3(z-1)^2}{z^5(z^2-b_3)}\epsilon_2}_{ExtraTerms}$$

$$(6.16)$$

The SNR degradation extracted from equation (6.15) is

$$\Delta SNR = -10\log\left[1 + b_3^2 + \frac{7}{5}\left(\frac{3b_3}{1-b_3}\right)^2\left(\frac{OSR}{\pi}\right)^2\right] \qquad (6.17)$$

Therefore, to be able to keep the overall SNR degradation less than 3dB, the parameter b_3 should be chosen less than 0.04. Comparison of the Simulink simulations with the analytical model describing the SNR degradation due to the imbalance introduced by b_3 is given in Fig. 6.4.

6.3   Example :

Stability and Sensitivity Analysis of a 4th order Single Bit $\Sigma\Delta$ Modulator

In this section, a complex 4th Order Single-Bit $\Sigma\Delta$ modulator will be analyzed. The block diagram of the modulator is given in Fig. 6.5. The noise transfer function of the modulator has 4 zeros. Two of them are placed at DC and the remaining 2 shifted inside of the
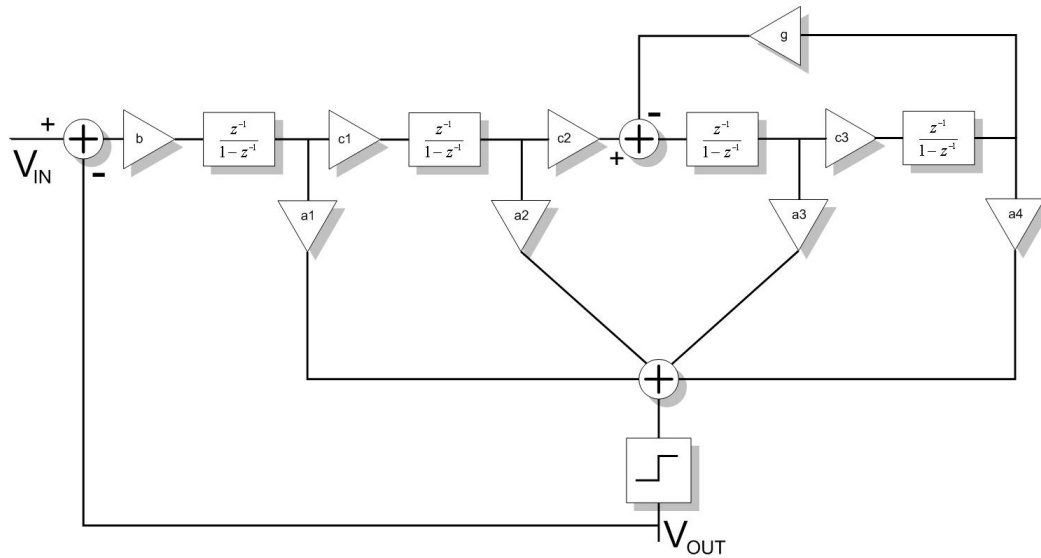
Figure 6.5. 4th Order Single Bit $\Sigma\Delta$ Modulator Schematic

Table 6.1. Coefficient Values of the 4th Order $\Sigma\Delta$ Modulator

Parameter	Value
a1	2
a2	2
a3	1.5
a4	1.5
b	0.4
c1	0.4
c2	0.3
c3	0.1
g	0.0025

signal bandwidth using the resonator formed with the feedback. The nominal values of the modulator coefficients are given in Table 6.1. The details of this modulator can be found in[80].

The cadence schematic shown in Fig. 6.6 is used to analyze the modulator. The schematic contains the cell optsd to configure the $\Sigma\Delta$ analysis module and the modulator output is acquired with the Scope block.

Figure 6.6. 4th Order Single Bit $\Sigma\Delta$ Modulator Cadence Schematic
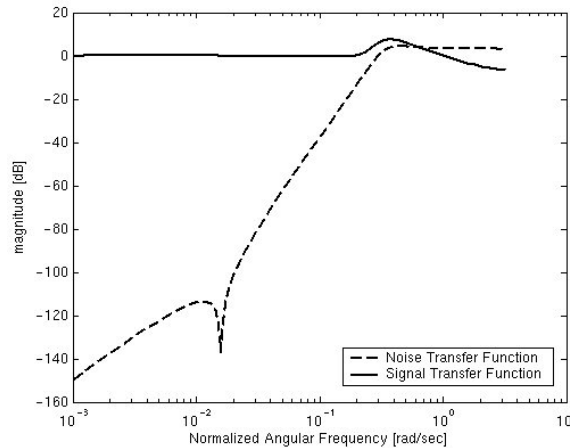
Figure 6.7. Signal and Noise Transfer Function of the $\Sigma\Delta$ Modulator

6.3.1 The Modulator Output Signal

As one would expect, the output signal of the modulator has a quite complex expression. The expression is obtained immediately using SSA Tool. It is

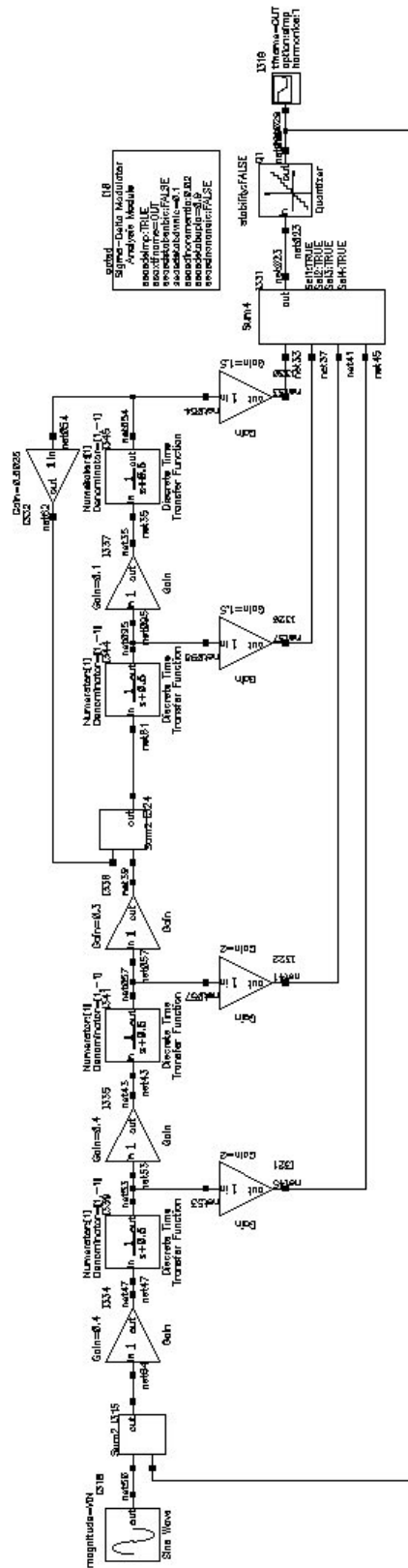$$V_{OUT} = \underbrace{\frac{0{\cdot}4(2z^3 - 5{\cdot}2z^2 + 4{\cdot}5805z - 1{\cdot}3623)}{z^4 - 3{\cdot}2z^3 + 3{\cdot}92025z^2 - 2{\cdot}1683z + 0{\cdot}45533}}_{SignalTransferFunction} V_{IN} + \underbrace{\frac{0{\cdot}25(4z^2 - 8z + 4{\cdot}001)(z - 1)^2}{z^4 - 3{\cdot}2z^3 + 3{\cdot}92025z^2 - 2{\cdot}1683z + 0{\cdot}45533}}_{NoiseTransferFunction} \epsilon$$

(6.18)

It is apparent from equation (6.18) that the noise transfer function has 4 zeros. The $\Sigma\Delta$ modulator analysis module plots the signal and noise transfer function of the modulator, as shown in Fig. 6.7. The transmission zeros due to the resonator controlled by the parameter g are apparent within the figure.

The module provides also a simplified expression of the in band quantization noise. This expression is obtained by integrating the noise transfer function within the signal band and simplifying the final expression by assuming that over sampling ratio is much larger than 1. The simplified in band noise power is

$$P_Q = \frac{125}{529984} \frac{\pi^4}{OSR^5} \frac{\Delta^2}{12}$$

(6.19)

6.3.2 Stability analysis

It is also possible to use SSA Tool to analyze the stability of the modulator. Linear root locus method is the technique adopted by the tool. For this purpose, the stability switch of the quantizer block is enabled and the cell optsd is properly configured. When the stability switch is disabled, the gain of the quantizer block, shown in Fig. 4.6. is set to 1. On the other hand, if the switch is enabled, the gain is substituted with a variable so that the noise
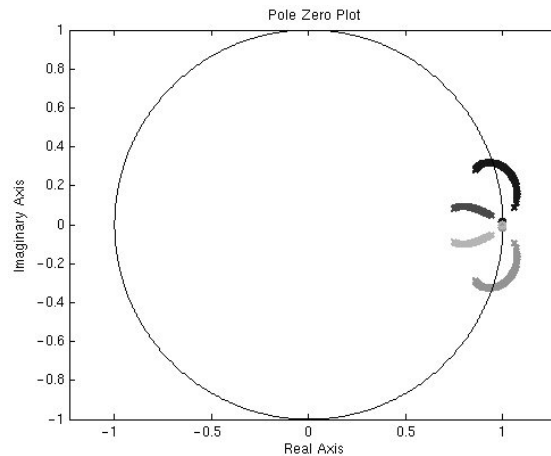
Figure 6.8. Root Locus Plot of the $\Sigma\Delta$ Modulator for varying Quantizer Gain

transfer function of the modulator can be expressed in terms of the quantizer gain K. Again, the SSA Tool provides the needed NTF immediately. It is equal to

$$NTF = \frac{0{\cdot}25(4z^2 - 8z + 4{\cdot}001)(z - 1)^2}{z^4 + (0{\cdot}8K - 4)z^3 + (6{\cdot}00025 - 2{\cdot}08K)z^2 + (1{\cdot}8322K - 4{\cdot}0005)z + 1{\cdot}00025 - 0{\cdot}54492K}\epsilon \quad (6.20)$$

The tool sweeps the quantizer gain K from 1 to 0 and calculates the location of the noise transfer function's poles and zeros as a function of the quantizer gain. Finally, it plots the root locus as shown in Fig. 6.8. As a result, it is possible to verify that the modulator is actually becoming unstable for K values below 0.567 . This is the critical quantizer gain for which the poles of the noise transfer function are on the unit circle.

6.3.3   Sensitivity analysis

It is also possible to determine the STF and NTF of the modulator as function of one or more parameters for sensitivity analysis purpose. For example, the output expression of the modulator as a function of the parameter a_4 is

$$V_{OUT} \quad = \quad \frac{0{\cdot}4(2z^3 - 5{\cdot}2z^2 + 4{\cdot}5805z - 1{\cdot}3803 + 0{\cdot}012a_4)}{z^4 - 3{\cdot}2z^3 + 3{\cdot}92025z^2 - 2{\cdot}1683z + 0{\cdot}44813 + 0{\cdot}0048a_4}V_{IN}$$
$$+ \frac{0{\cdot}25(4z^2 - 8z + 4{\cdot}001)(z - 1)^2}{z^4 - 3{\cdot}2z^3 + 3{\cdot}92025z^2 - 2{\cdot}1683z + 0{\cdot}44813 + 0{\cdot}0048a_4}\epsilon \quad (6.21)$$

Fig. 6.9 shows the sensitivity of the modulator's noise transfer function to the parameter g. For this purpose, the SSA Tool extracted the modulator NTF as a function of g.
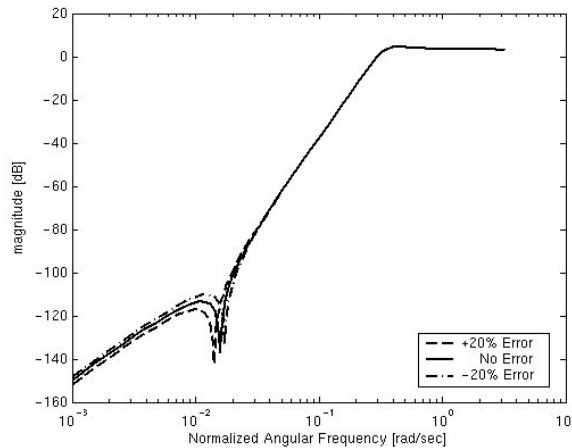
Figure 6.9. Sensitivity of the Noise Transfer Function to the parameter g

6.4 Example : Non-Linear Analysis Of Switched Emitter Follower: How to improve its linearity.

6.4.1 Problem Definition

Track-and-Hold amplifiers are one of the most important building blocks of the analog to digital converter systems. Obtaining high sampling resolution together with high speed is the main challenge of the design process. Classically, it is possible to separate Track-and-hold architectures to two main groups, namely Closed-Loop and Open-Loop architectures [67].

Closed-Loop architectures contain one or more high gain amplifiers and they overcome linearity problems using their large loop gain, since loop gain suppresses the output signal's non-linear components. But, unfortunately, amplifiers gain-bandwidth requirement becomes unachievable for frequency ranges above 100Mhz. Hence, this topology is not suitable for high-frequency application.

The open-loop implementation alternative, on the other hand, is obviously faster but its linearity is determined by the linearity of its input and output buffers and sampling switch. Typically, attainable linearity is not better than -60 to -90 dB. Among different open-loop architectures, the switched emitter follower structure is widely used within high-resolution high speed converter systems.

During the tracking mode, the switched emitter follower, as shown in Fig. 6.10. is basically nothing but a simple emitter follower[8]. Therefore, it is important to analyze the non-linear response of the emitter follower to improve the linearity performance of the switched emitter follower. That is the basic motivation of the analysis conducted here.

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[8]Q1, Q2 and the bias current I_B form an emitter follower.

Figure 6.10. Switched Emitter Follower and its equivalent circuit during the tracking mode

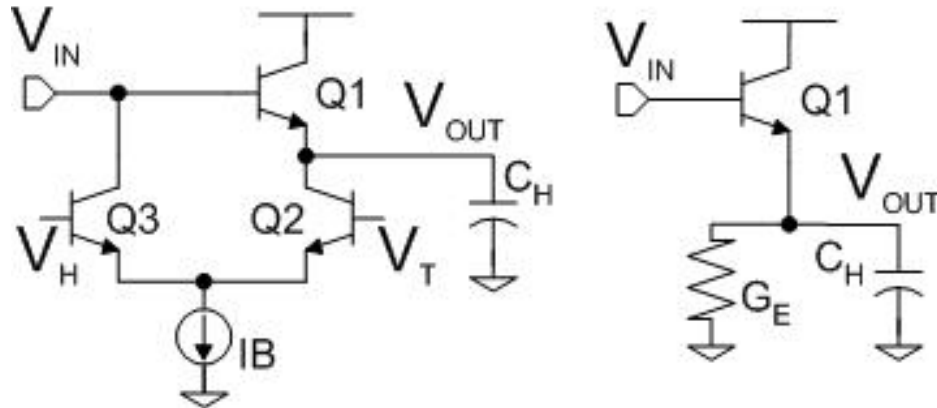All precise applications use fully differential or pseudo-differential structures for track-and-hold implementations: the differential processing cancels out the even-order harmonic distortion. Assuming the use of differential architectures, the analysis that will follow focus on the dominant odd-order harmonic, i.e. the third order term. Moreover, since the third order harmonic of a pseudo-differential track-and-hold is 6 dB higher than the single-ended counterpart the analysis will be conducted on the single-ended version only.

6.4.2 Nonlinear Bipolar Junction Transistor Device Model Selection

Selecting the most suitable nonlinear device model is very important in order to obtain accurate numerical results from the nonlinear transfer functions. Of course, the most suitable model changes with respect to the biasing point, operating frequency or in general operating condition of the circuit.

As it will be clear later in this section, the third order harmonic distortion transfer function of the simple emitter follower is dominated by the BJT output conductance nonlinearity at low operating frequencies and by its transconductance nonlinearity at high operating frequencies. Therefore, it is important to choose before hand an accurate device model so that the coefficients of these two different nonlinearities can be calculated correctly.

$$I_C = I_S \left(1 + \frac{V_{CE}}{V_A} \right) \exp\left(\frac{V_{BE}}{V_T} \right) \tag{6.22}$$

Equation (6.22) shows classical collector current of a bipolar junction transistor. For the sake of simplicity, the early voltage V_A is generally chosen as a constant.

Even though this is a pretty good approximation for hand calculation, it is useless for nonlinear modeling because the output conductance is modelled completely linearly.

The collector current of bipolar junction transistor is determined by the BJT transistor's base region length. The changes of this length due to the length modulation of the

reverse biased collector-base junction's depletion region will modify the collector current. This depletion region length modulation is a function of the collector-base voltage of the device. Since, the base-emitter voltage can be assumed to be constant with high accuracy and consequently the modulation of the base-emitter depletion region length is negligible, the collector current modulation due to the collector-base voltage changes is referred to the emitter terminal in order to model the effect as the output conductance.

Here, we will compare the accuracy of three different early voltage model with respect to the real simulation data. The first model is the simple model and the early voltage is assumed to be a constant. The second model, Sansen model that is given in [81], expresses the collector current as follows:

$$I_C = I_S \left(1 + \frac{V_{CB}}{\frac{qAN_C}{c_{jc}} \left(1 + \frac{V_{BC}}{v_{jc}} \right)^{m_{jc}}} \right) \exp \left(\frac{V_{BE}}{V_T} \right) \tag{6.23}$$

where q is the electron charge, A base-collector junction area, N_C is the collector doping concentration, c_{jc} is the unit area junction capacitance, v_{jc} is the collector-base built in junction potential. And finally, the third model, Cilingiroglu model that is given in [82], expresses the collector current as

$$I_C = I_S \left[1 + \frac{V_{CB}}{G\sqrt{\frac{2q}{N_C \epsilon_{Si}} (V_{CB} + \Phi_J)} - 3V_{CB} - 2\Phi_J} \right] \exp \left(\frac{V_{BE}}{V_T} \right) \tag{6.24}$$

where G is the base metallurgical Gummel number, N_C doping concentration of the collector, ϵ_{Si} is the dielectric permittivity of the silicon, Φ_J is the collector-base built in junction potential.

Each one of the three equations yields different nonlinearity coefficient expressions at different degree of expression complexity and accuracy[9]. The comparison of these three collector current models with the real simulation data is given in Fig. 6.11. As it is clear from the figure, the Cilingiroglu model is the most accurate expression. Consequently, the nonlinearity coefficient expressions extracted from equation (6.24) are the most complex ones.

Selecting the most accurate model might not be always the best choice. For example, if these expressions will be used to model the nonlinear behavior of a track and hold amplifier, complex expressions will require very long simulation time[10]. If the expressions will be evaluated just once then of course the most accurate expression should be used.

[9]Generally speaking, the expression complexity trades with the expression accuracy.
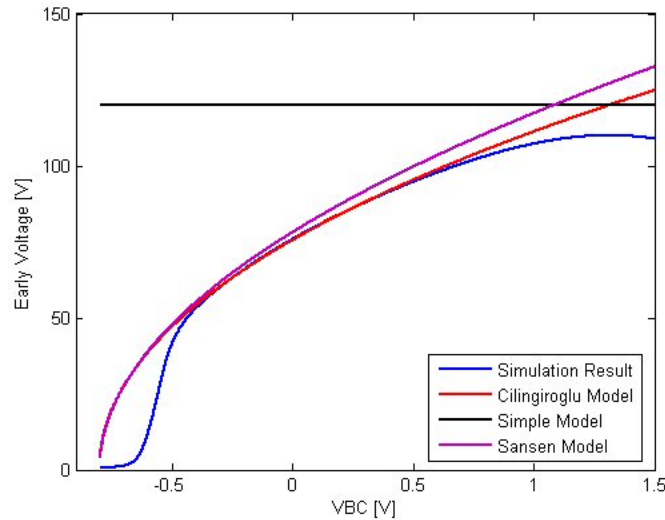[10]Although the numerical accuracy will be very high.

Figure 6.11. Variation of the Early Voltage Expressions with respect to the Base-Collector Voltage

6.4.3 Nonlinear Analysis of Emitter Follower

The nonlinear analysis of a simple emitter follower yields a complex expression. For presentation purpose, this expression can be simplified to two asymptote expressions, one valid for low operating frequencies and the other for high operating frequencies.

$$V_{OUT\_3} = \begin{cases} \dfrac{K_{3gm2go}(G_E + go) - K_{3go}(g_m + g_\pi)}{4(g_m + g_\pi)^2} V_{IN}^3 & \text{For Low frequencies} \\[4mm] \dfrac{(sC_H)^3 \left[K_{3gm}(g_m + g_\pi) - K_{2gm}^2\right]}{4(g_m + g_\pi + 3sC_H)^2(g_m + g_\pi + sC_H)^3} V_{IN}^3 & \text{For High frequencies} \end{cases} \quad (6.25)$$

where K_X are the Taylor expansion coefficients defined in section 4.9. These two asymptotes are plotted for a typical technology in Fig. 6.12. It shows that for input frequencies lower than 70 MHz the minimum expected third harmonic distortion is around -100 dB. For higher frequencies the result worsens and becomes -70 dB at 100 MHz.

The elaboration of the aforementioned equations leads to the following observations:

1. At low frequencies, the harmonic distortion mainly results from the non-linearity of the transistor's output conductance and it is due to the V_{CB} variations.

2. At high frequencies, harmonic distortion comes from the non-linearity of transistor's transconductance and it is due to the V_{BE} variations.

After identifying the causes of the nonlinear signals at the output, the natural question to ask is: How can we improve the linearity? The non-linear behavior is introduced to the analysis using the nonlinear current sources. Therefore, decreasing their magnitudes will definitely improve linearity. For example, the magnitude of second order nonlinearity current
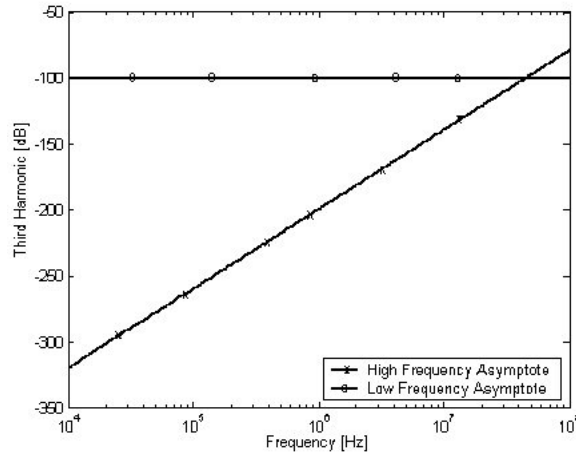
Figure 6.12. Low and High Frequency asymptotes of simple Emitter Follower's third harmonic.

of the collector current is

$$INL_{2ic} = \frac{K_{2gm}}{2}V_{BE,1}^2 + \frac{K_{2go}}{2}V_{CE,1}^2 + K_{gmgo}V_{BE,1}V_{CE,1} \tag{6.26}$$

A closer look to the magnitude of this current source value reveals two means to decrease it. First strategy can be to decrease non-linearity coefficients, denoted as K_{2gm}, K_{2go} and so on. But, unfortunately non-linearity coefficients are determined by the operating point of the circuit, which is generally set by the system level requirements, such as power consumption, signal bandwidth, etc.. Therefore, these coefficients cannot be determined independently.

The second strategy is to minimize the control signals, which are collector-emitter and base-emitter voltages, using suitable circuit topologies.

In short, combined with the observation stated above, we can conclude that the circuit solutions that minimize the variation of V_{CB} and V_{BE} will improve the low and high frequency linearity of the circuit, respectively.

6.4.4   Improving Low frequency Distortion Performance

At the end of the previous sub-section, we concluded that the low-frequency distortion limit arises from the output conductance of the transistor, which is controlled by its collector to emitter voltage or rather collector to base voltage as shown in the collector current equation previously. Therefore, keeping this control voltage constant should cancel related distortion components.

This basic concept is shown in Fig. 6.13. Collector terminal is connected to the base terminal with a DC voltage source.

Hence, collector voltage tracks base voltage, therefore collector to base voltage is
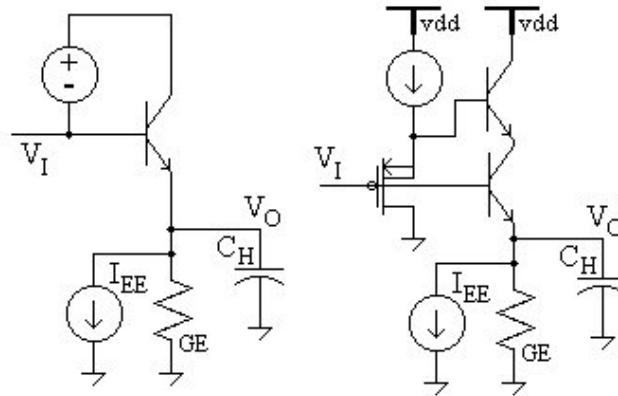
Figure 6.13. The basic idea and its circuit implementation to improve low frequency distortion performance

constant. An easy implementation of the concept is shown on right. Input voltage is shifted up with a source-follower and then fed to the collector terminal with another BJT. This design trades the voltage headroom with linearity.

$$V_{OUT\_3} = \frac{G_E^3 \left[K_{3gm}(g_m + g_\pi) - K_{2gm}^2 \right]}{4(g_m + g_\pi)^5} V_{IN}^3 \tag{6.27}$$

The distortion analysis of this circuit yields equation (6.27). Notice that this equation is very similar to the high frequency asymptote given in equation (6.25) of the emitter follower. The Spectre-RF simulations and symbolic analysis show that for the same bias conditions, low frequency distortion is decreased to −195 dB. The comparison with the circuit simulation will be shown later in the section.

6.4.5 Improving High frequency Distortion Performance

During the distortion analysis of the simple emitter follower, we also concluded that the distortion at high frequency originates from the transconductance nonlinearity of the transistor, which is in turn controlled by the base to emitter voltage. According to our collector current model, given by equation (6.24), since the collector-base voltage is kept constant, the only variable that can change the base-emitter voltage is the collector current. Therefore, if we can somehow keep the emitter current constant, which is equal to α_F times collector current, it is possible to keep the base-emitter voltage constant. The concept is shown in Fig. 6.14.

The current at the emitter changes because of the finite output resistance of the current generator and the capacitive current on the capacitive load. Typically, for high-resolution applications, it is necessary to use relatively large sampling capacitors (to have a low kT/C noise floor). Therefore, for high frequency applications the capacitive current is dominant with respect to the in-phase term. Its magnitude, of course, increases with the
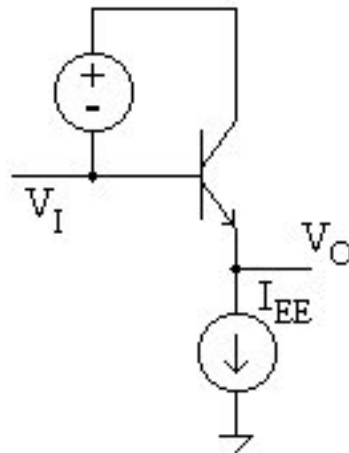
Figure 6.14. The basic idea to improve high frequency distortion performance

frequency[11]. Therefore, in order to reduce the high-frequency distortion, it is necessary to compensate this capacitive current.

One possible implementation for compensating the hold capacitor current is shown in Fig. 6.15. The basic idea is to create somewhere else the same capacitive current and then compensate the original sampling switch using it. The replica switch is loaded with a reference capacitor C_{HR} and its current is fed to the original switch from the emitter of transistor Q2. If the reference capacitor current matches to the hold capacitor current, it is possible to cancel the Q1s emitter current variation due to the hold capacitor, as shown by the equation (6.28). This design trades area and power with linearity.

$$I_{E(Q_1)} \cong I_{EE} - I_{CHR} + I_{CH} \cong I_{EE} \tag{6.28}$$

The issue on the design of this structure is the determination of the reference capacitor value. Intuitively, it is possible to say that these two capacitors, C_{HR} and C_H, should be chosen equal. But since, the collector-base voltage and emitter current of Q2 is not constant, its base-emitter voltage is also not constant, resulting that at high frequencies reference capacitor current does not match to the hold capacitors current.

In literature, the reference capacitor is chosen as half of the hold capacitor value. However, the Spectre-RF simulations and symbolic distortion analysis results, that will be presented later, show that up to a certain frequency, around 200 Mhz, equal capacitor configuration has better distortion performance. Bottom line, optimal reference capacitor value depends on the operating frequency and bias point of the circuit.

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[11]It increases as cube of the frequency, since the signal of interest is the third order harmonic distortion.
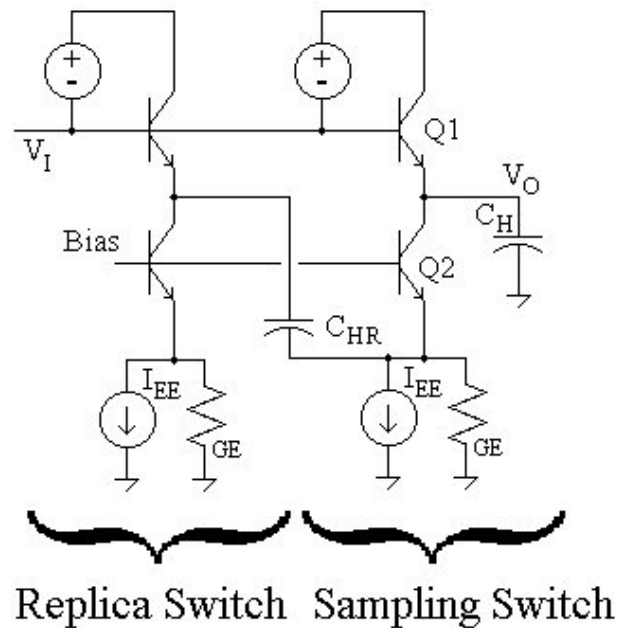
Figure 6.15. Replica Switch Implementation to improve high frequency distortion performance

6.4.6 Comparison of the Analytical Results with the Simulation Results

SpectreS simulations have verified the circuit solutions presented in the previous sections for $1{\cdot}5$ V_{PP} input signal, 3mA bias current and 1.6pF hold capacitor. The technology used is a 0.8 μm SiGe process. In order to outline the distortion contribution of the emitter follower transistor, simulations with ideal components except the emitter follower transistor itself have been performed. These simulations are then compared with the symbolic analysis results. The non-linearity coefficients used within the symbolic expressions are evaluated using equation (6.24). The results are shown in Fig. 6.16. The derived numbers almost perfectly fit the simulation results. Therefore, the used nonlinear device model and the calculation approach used in the symbolic analysis are proved to be quite accurate.

6.5 Example : Small Signal Analysis of ADC Comparator Input stage

In this section, I will analyze the small signal transfer function of the input stage of the comparators used within the 10 bit SAR ADC section of the designed ADC. This is a very simple input stage having cross coupled positive feedback transistor as load to improve the gain of the stage. The schematic of the input stage is shown here once more in Fig. 6.17.

The analysis schematic contains the transconductance and output conductance of each transistor shown in the schematic. The capacitors loading the output nodes and the common node of the differential pair are explicitly included to the analysis. The small signal
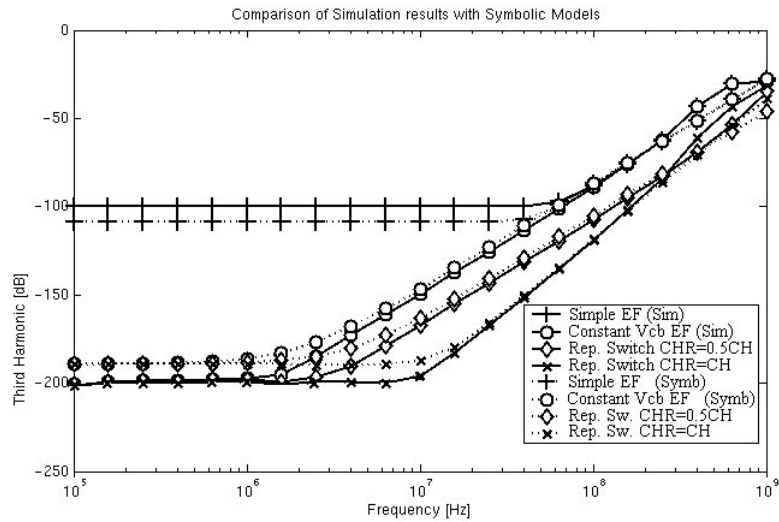
Figure 6.16. Comparison of the Simulation and symbolic results.
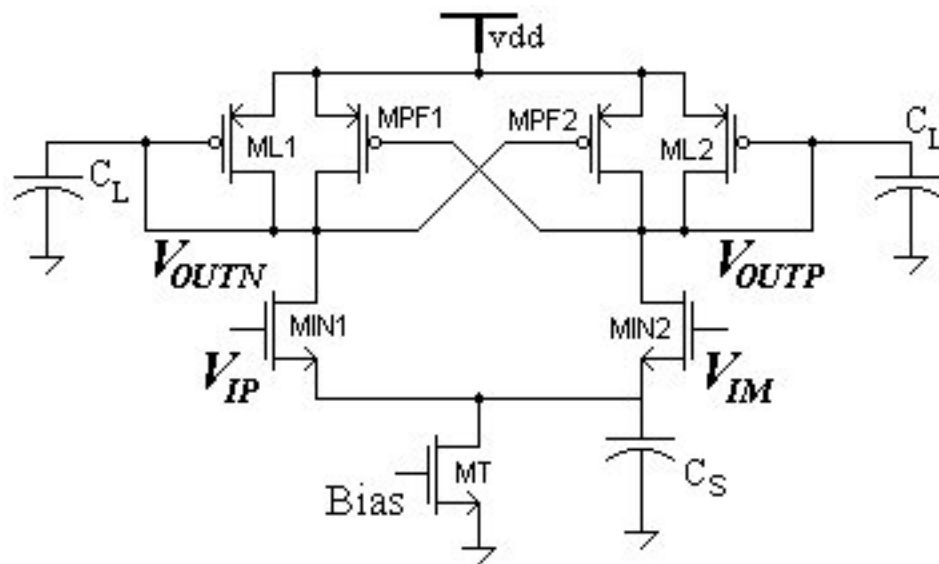
Figure 6.17. Input Stage of the Comparator

parameters of matching devices (i.e. input differential pair transistors, diode connected load transistors, cross coupled positive feedback transistors) are assumed to be equal. Under these conditions, the transfer function of the input stage can be expressed as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{gmin}{s\ Cl + gml + gol + goin + gopf - gmpf} \tag{6.29}$$

where $gmin$, gml and $gmpf$ are the transconductance parameter of the input differential pair transistors, diode connected load transistors and cross coupled positive feedback transistors, respectively; $goin$, gol and $gopf$ are the output conductance parameters of the respective transistors and finally Cl is the output terminal load capacitor value.

Notice that since the circuit is perfectly symmetrical, the common node at the source of the input differential pair transistors' is ac ground and therefore, the transfer function does not contain neither the output conductance of the tail current transistor nor the capacitor loading the common node.

For the sake of experiment, a mismatch between the input differential pair transistors is introduced. The transfer function for this case is shown in Fig. 6.18 where $gmin1$ and $gmin2$ are the transconductance parameters of the transistors whose gate terminals are connected to positive and negative input terminals respectively. By inspecting this equation, it is really easy to appreciate the effectiveness of the tool. This equation is the direct output of the SSATool.

```
                                              2   2
1/2 VIN ((gmin2 + gmin1) Cs Cl j  w1  + (4 gmin2 Cl gmin1

        + (gmin2 + gmin1) Cs gopf + (gmin2 + gmin1) Cl got

        + ((gmin2 + gmin1) Cs + (2 gmin2 + 2 gmin1) Cl) goin

        + (gmin2 + gmin1) Cs gol + (gmin2 + gmin1) Cs gml

        + (gmin2 + gmin1) Cs gmpf) j w1

        + ((2 gmin2 + 2 gmin1) gopf + (gmin2 + gmin1) got) goin + %1 gol

        + 4 gmin2 gopf gmin1 + (gmin2 + gmin1) gopf got + %1 gml + %1 gmpf)

          /                                              2   2
         /  ((j w1 Cl + gopf + gml + gol + goin - gmpf) (j  w1  Cl Cs + (
        /

        (gmin2 + gmin1) Cl + gopf Cs + Cl got + (Cs + 2 Cl) goin + gol Cs

        + gml Cs + gmpf Cs) j w1 + (got + 2 gopf) goin

        + (2 goin + gmin2 + gmin1 + got) gol + (gmin2 + gmin1) gopf

        + gopf got + (2 goin + gmin2 + gmin1 + got) gml

        + (2 goin + gmin2 + gmin1 + got) gmpf))

    %1 := 4 gmin1 gmin2 + (gmin2 + gmin1) got + (2 gmin2 + 2 gmin1) goin
```

Figure 6.18. New transfer function as result of Input differential pair mismatch.

CHAPTER 7

CONCLUSION

In this dissertation a novel Sub-Ranging analog to digital converter capable of processing high input signal voltage level (up to twice the supply voltage) without any signal conditioning is presented. For this purpose, two novel high voltage signal processing circuits, i.e. high-voltage bootstrapped sampling switch and high-voltage passive subtractor are developed. The sampling switch allowed the converter to expand its input signal range beyond the supply voltage while the passive subtractor enabled us to process this high voltage level input without any precision loss or device reliability issue. Proposed ADC is the concept proof that the resolution of the analog to digital converter can be extended not only towards the LSB by resolving smaller and smaller voltage differences but also towards the MSB by successfully resolving higher than supply input signal levels. Proposed converter is implemented using Texas Instrument LBC7 process as a part of a power management IC dedicated for portable applications and the performance of the converter was measured. The measurement results proved the expected accuracy as well as the noise resilient. Obtained measurement results were well within the the expected performance. As a result, proposed analog to digital converter is a good candidate for power management applications.

In addition to the designed analog to digital converter, a symbolic circuit analyzer capable of analyzing linear and/or nonlinear behavior of an arbitrary circuit and system is developed and presented. Goal oriented simplification technique is used to simplify the results of the symbolic analysis. This technique proves to be very useful for system level design and optimization problems such as Sigma-Delta modulator system design. The capabilities of the tool is presented in detail together with a brief explanation of the weakly nonlinear circuit analysis technique implemented within the tool.

APPENDIX A

The Effect of the finite Amplifier Gain to the performance of an SC Integrator

The effect of the finite amplifier gain to the z-domain transfer function of a discrete-time integrator is analyzed usign the circuit shown in Fig. A.1. Two parasitic capacitances, i.e. C_{PN1} and C_{PNS}, that are effecting the transfer function are also included into the analysis. C_{PN1} constitutes of amplifier's input capacitance, top plate fringing capacitance of the integration capacitor and the switch transistor junction capacitance. C_{PNS} constitutes of the top plate fringing capacitance of the sampling capacitor and the switch junction capacitances. Since the remaining parasitic capacitances are driven with low impedance sources, they are ignored during the analysis. The non-ideal transfer function of the discrete-time integrator can be expressed as

$$TF(z) = \frac{C_S}{C_I} \frac{1}{1 + \frac{1}{A}\left(1 + \frac{C_S + C_{PNS} + C_{PN1}}{C_I}\right)} \frac{1}{z - \frac{1 + \frac{1}{A}\left(1 + \frac{C_{PN1}}{C_I}\right)}{1 + \frac{1}{A}\left(1 + \frac{C_S + C_{PNS} + C_{PN1}}{C_I}\right)}} \tag{A.1}$$

Assuming that the small signal gain A is sufficiently large, it is possible to simplify A.1 further as

$$TF(z) = \frac{C_S}{C_I}\left[1 - \frac{1}{A}\left(1 + \frac{C_S + C_{PNS} + C_{PN1}}{C_I}\right)\right] \frac{1}{z - \left[1 - \frac{1}{A}\left(1 + \frac{C_S + C_{PNS}}{C_I}\right)\right]} \tag{A.2}$$

Therefore, to analyze the effect of the finite amplifier gain, the ideal integrator function
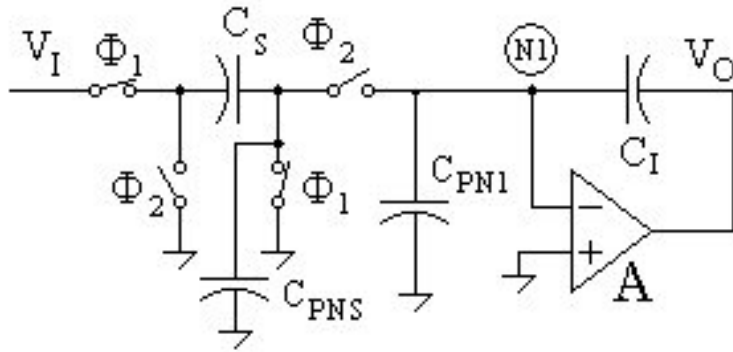
Figure A.1. Non-Ideal Discrete-Time Integrator

should be replaced with

$$TF(z) = \left(1 - \frac{b}{A}\right) \frac{K}{z - \left(1 - \frac{c}{A}\right)} \tag{A.3}$$

where K is the integrator gain and the values of b and c can be estimated from A.2.

APPENDIX B

Signal to Noise Ratio Degradation Due to Excess In Band Noise: Definition of ΔSNR

The signal to noise ratio at the output of a system can be expressed as

$$SNR = 10 \log \left(\frac{P_S}{P_N} \right) \tag{B.1}$$

where P_S is the power of the signal of interest at the output and P_N is the noise power at the output.

The noise signal at the output of an ideal $\Sigma\Delta$ modulator consists of only quantization noise P_Q. Assuming that a generic N^{th} order $\Sigma\Delta$ modulator noise transfer function can be expressed as

$$NTF(z) = \left(1 - z^{-1} \right)^N \tag{B.2}$$

the quantization noise power is

$$P_Q = \int_{-f_B}^{f_B} |NTF(f)|^2 \, S_Q^2(f) df = \int_{-f_B}^{f_B} \left| 2 \sin \left(\frac{\pi f}{F_S} \right) \right|^{2N} \frac{\Delta^2}{12 F_S} df \tag{B.3}$$

where F_S is the sampling frequency, Δ is the quantization step size and f_B is the modulator bandwidth. Assuming that the sampling frequency is much higher than the bandwidth, the equation B.3 can be simplified as:

$$P_Q = \int_{-f_B}^{f_B} \left| \frac{2 \pi f}{F_S} \right|^{2N} \frac{\Delta^2}{12 F_S} df = \frac{\Delta^2}{12} \frac{\pi^{2N}}{2N+1} \left(\frac{2 f_B}{F_S} \right)^{2N+1} \tag{B.4}$$

The ratio $F_S/2f_B$ is commonly referred to as oversampling ratio (OSR). Therefore, the quantization noise power of a $\Sigma\Delta$ modulator having N^{th} order noise shaping is

$$P_Q = \frac{\Delta^2}{12} \frac{\pi^{2N}}{2N+1} \left(\frac{1}{OSR} \right)^{2N+1} \tag{B.5}$$

Now that we defined quantitatively the quantization noise, we can continue with the definition of ΔSNR. Theoretical upper limit of achievable SNR can be obtained by replacing the noise power in B.1 with the quantization noise power expressed in B.5. In reality, any circuit non-ideality will change the in band noise power and degrade the SNR. Therefore, without loosing generality, the signal to noise ratio can be expressed as

$$SNR = 10 \log \left(\frac{P_S}{P_Q + \Delta P} \right) = 10 \log \left(\frac{P_S}{P_Q \left[1 + \frac{\Delta P}{P_Q} \right]} \right)$$

$$\begin{aligned}
SNR &= 10\log\left(\frac{P_S}{P_Q}\right) - 10\log\left(1 + \frac{\Delta P}{P_Q}\right) \\
SNR &= SNR_{ideal} + \Delta SNR
\end{aligned} \tag{B.6}$$

Therefore, ΔSNR is defined as

$$\Delta SNR = -10\log\left(1 + \frac{\Delta P}{P_Q}\right) \tag{B.7}$$

APPENDIX C

The Effect of the Linear Settling Error of the Amplifier

During the settling the amplifier can be modeled as shown in fig C.1. This is a unity gain configured amplifier. Assuming that the amplifier has single pole behavior, its transfer function can be expressed as

$$K(s) = \frac{K}{\frac{s}{p} + 1} \tag{C.1}$$

where K is the DC gain and p is the pole frequency. The transfer function of the circuit can be expressed as:

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = H(s) = \frac{K}{\frac{s}{p} + 1 + K} \tag{C.2}$$

assuming that the DC gain is large enough, equation C.2 can be simplified to

$$H(s) = \frac{Kp}{s + Kp} = \frac{GBW}{s + GBW} \tag{C.3}$$

For a step function input, the output can be expressed in time domain as

$$V_{OUT}(t) = 1 - \exp(-2\pi f_U t) = 1 - b \tag{C.4}$$

Therefore, the linear settling error introduces only a gain error to the transfer function. In order to quantify required gain bandwidth product for a given gain error, let us assume that allowed settling time is equal to $T_{CLK}/2\alpha$, where T_{CLK} is the sampling period and $1/\alpha$ is a parameter to set the percentage of half period used for settling. Therefore, the unity gain frequency can be expressed as

$$f_U = -\frac{\alpha f_{CLK} \ln(b)}{\pi} \tag{C.5}$$
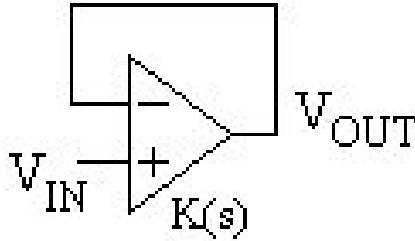
Figure C.1. Equivalent Circuit of an SC Block During Settling

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APPENDIX D

The Effect of the Switch On-Resistance

The effect of the switch non-zero on resistance can be modeled as shown in Fig. D.1. C_S represents equivalent sampling capacitance; C_I is integration capacitance or summing capacitance; R_{on} is equivalent on resistance of the switches connecting sampling capacitance to the floating node V_{N1} and to the input node V_{IN}. Assuming that the amplifier has infinite DC gain, the transfer function can be expressed as:

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = -\frac{C_S}{C_I}\left(\frac{1}{2sR_{on}C_S + 1}\right) \tag{D.1}$$

The term C_S/C_I in D.1 is the ideal transfer function of the circuit. The effect of the switch on resistance is introduced to transfer function with the second term. The time domain output signal of the circuit for a step function input can be expressed as follows:

$$H(s) = \frac{C_S}{C_I}\left[1 - \exp\left(-\frac{t}{2R_{on}C_S}\right)\right] \tag{D.2}$$

Therefore, as it is obvious from equation D.2, the error introduced by the non-zero on-resistance of the MOS switches can be modeled as a gain error at the output of the amplifier. It can be included to the simulations by modifying the ideal transfer function with

$$H(s) = [1 - b]\, H_{ideal} \tag{D.3}$$

where the parameter b is equal to

$$b = \exp\left(-\frac{t}{2R_{on}C_S}\right) \tag{D.4}$$

In order to calculate the required time constant of the switched capacitor circuit, let us assume that allowed settling time is equal to $T_{CLK}/2\alpha$, where T_{CLK} is the sampling period
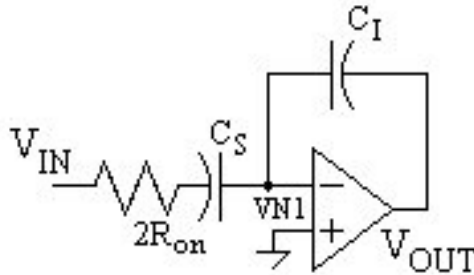
Figure D.1. The model for the effect of switch on resistance

and $1/\alpha$ is a parameter to set the percentage of half period used for settling. Therefore, required time constant is:

$$R_{on}C_S = -\frac{1}{4\alpha f_{CLK}\ln(b)} \tag{D.5}$$

APPENDIX E

High Voltage Bootstrapped Sampling Switches: Evolution

During the quest to sample signal levels exceeding the supply voltage level, two earlier versions of the High-Voltage Bootstrapped sampling switch, presented in section 3.3, are developed. Although, they are identical in terms of functionality, they are very different in terms of performance, requirements and the scheme used to protect the PMOS pass transistor. Here, I will briefly describe these earlier versions and the trade-offs involving their designs to give an idea to the reader about the evolution of the HSB switch.

E.1 First Version of The Sampling Switch

First version of the high-voltage sampling switch is shown in Fig. E.1. The bootstrapped switch is the NMOS connected to the OUT terminal. It will take one clock period for the switch to reach its steady state operation, which is also the same amount of cycles it takes the traditional switch to reach its steady state. After that first clock cycle has passed all the capacitors C_1, C_2, C_3 and C_4 can be assumed to have initial conditions of V_{dd}.

To understand easily the operation of this switch one needs to start from aforementioned initial conditions and with the clock PHI being low. The state of every device, and every node in the circuit needs to be identified just before PHI transitions from low to high. The same thing should then be done at the instance just before PHI goes from high to low. The summary below records that state of the circuit at each one of those two instances:
When PHI is low:

- M_{N9} will turn on, M_{N10} will turn off.

- Bottom plate of C_3 will be grounded

- N_5 will be pushed to $2V_{dd}$ since the bottom plate of C_1 will be at V_{dd}

- M_{N6} will therefore turn on charging top plate of C_3 (N_7) to V_{dd}

- N_4 will be at V_{dd} and the bottom plate of C_2 will be grounded

- M_{N7} is off, M_{N4} is on and M_{N3} is off

- M_{N8} is on grounding the bootstrapped NMOS switch
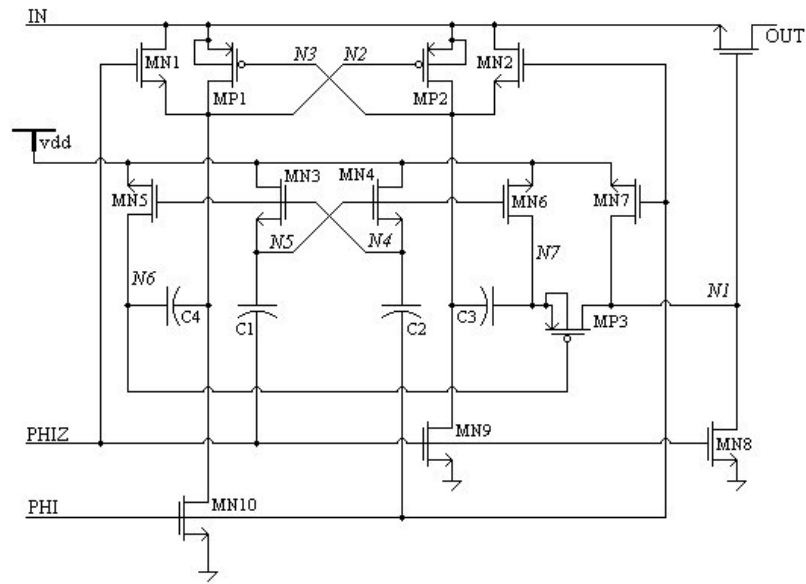
Figure E.1. First Version of High-Voltage Bootstrapped Sampling Switch

- Top plate of C_2 will be charging to V_{dd} because N_5 is pushed to $2V_{dd}$

- N_6 gets pushed to $V_{dd} + V_{IN}$ since the bottom plate of C_4 is pushed to V_{IN}.

- M_{N5} will be off and no body diodes will be turned on since N_6 (the drain of M_{N5}) is at a higher voltage than both its source and its bulk.

- M_{P3} is off because its gate (N_6) is at $V_{dd} + V_{IN}$, while its source (N_7) is at V_{dd}. (It should be noted that M_{P3} must have a V_{GS} breakdown voltage that is higher than V_{IN}). Again no body diodes will be turned on because the drain of M_{P3} is at zero.

- If V_{IN} is low M_{N1} will do the job of M_{P1} and charge the bottom plate of C_4 to V_{IN}.

In summary, during this phase, the switch is turned off and the capacitor C_3 is charged to V_{dd}.

When PHI is high:

- M_{N10} will turn on, M_{N9} will turn off

- Bottom plate of C_3 will be pushed to V_{IN} as a result.

- N_4 will be pushed to $2V_{dd}$ since the bottom plate of C_2 will be pushed to V_{dd}.

- N_5 will be at V_{dd} and the bottom plate of C_1 will be grounded

- M_{N3} will be on and M_{N4} will be off

- M_{N5} will be on and the top plate of C_4 will charge to V_{dd}

- M_{N8} is off and therefore the node driving the bootstrapped switch (N_1) is released.

- N_7 will be pushed to $V_{dd} + V_{IN}$ since the bottom plate of C_3 is pushed to V_{IN}

- M_{N6} will be off and no body diodes will be turned on since N_7 (the drain of M_{N6}) is at a higher voltage than both its source and its bulk.

- M_{N7} will want to charge N_1 to $V_{dd} - V_{tn}$. M_{N7} will be on but conducting only in the other direction (ie from source to drain) until N_1 reaches $V_{dd} - V_{tn}$

- M_{P3} is on because its gate (N_6) is at V_{dd}, while its source (N_7) is at $V_{dd} + V_{IN}$. V_{GS} of M_{P3} is therefore equal to V_{IN}. This will short N_1 to N_7 which is at $V_{dd} + V_{IN}$ for all V_{IN} values greater than the threshold voltage V_{tp} of M_{P3}

- In the event that N_1 goes to a higher voltage than V_{dd} (ie if M_{P3} is on) M_{N7} will turn off and no body diodes will be turned on.

- In the event that the V_{GS} of M_{P3}, which is equal to $V_{dd} - (V_{dd} + V_{IN}) = V_{IN}$, is not sufficient to turn on M_{P3} (low values of V_{IN}) M_{N7} will still charge N_1 to $V_{dd} - V_{tn}$.

In summary, during this phase, M_{N7} charges the floating N_1 till $V_{dd} - V_{tn}$; then if the input signal exceeds the threshold voltage of M_{P3}, this transistor turns on and the voltage on node N_7, i.e. $V_{dd} + V_{IN}$, appears at the gate of the sampling switch. Notice that the gate-to-source voltage of M_{P3} is bounded within $\pm V_{IN}$.

From the above statements, it is obvious that the V_{GS} of the bootstrapped switch will at least be equal to $V_{dd} - 2V_t$. This condition happens when V_{IN} is slightly less than V_{tp} of M_{P3}. Since the worst case gate voltage of the bootstrapped switch is at $V_{dd} - V_{tn}$ and it happens for V_{IN} is equal to V_{tp}, the worst case V_{GS} is at least $V_{dd} - 2V_t$. This will be more than enough to turn on the bootstrapped switch when PHI is high for the current system specifications. For V_{IN} values that are greater than V_t of M_{P3} the V_{GS} of the bootstrapped switch will always be at V_{dd}. It can also be seen that no body diodes are activated for the entire V_{IN} range and that the energy losses in this switch are limited to shoot-through currents when the switch changes state as well as the charging and discharging of the capacitive nodes in the circuit.

The simulation results of the first high-voltage sampling switch is given in Fig. E.2. The results are extracted from transient simulations. The clock frequency is 2 MHz and the supply voltage is 2.75 V. As expected, the maximum gate to source voltage of M_{P3} is equal to the input voltage. The gate overdrive of the bootstrapped switch is decreasing for very low values of the input signal, as explained previously. Once the input signal exceeds the threshold voltage of M_{P3}, the switch overdrive increases again. While the input signal keeps increasing, the over-drive voltage starts decreasing slowly once more. The reason for this
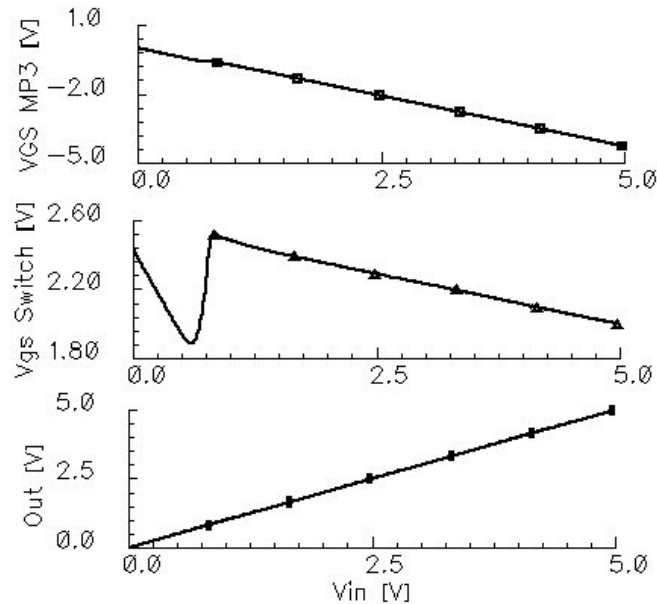
Figure E.2. Simulation Results Of First Version of High-Voltage Bootstrapped Sampling Switch

decrease is the parasitic capacitance associated with node N_1. This loss of overdrive voltage can be minimized by increasing the value of C_3.

E.2 Improved Version of the Sampling Switch

The second version of the high-voltage sampling switch is shown in Figure E.3. The circuit takes only one clock cycle to reach steady state operation. After the first clock cycles have passed the capacitors C_1, C_2, and C_3 can all be assumed to have charged to an initial condition of V_{dd}.

To easily understand the operation of this switch one needs to record the state of the switch before and after every timing event. Fig. E.4 shows the timing diagram of the various clock signals needed for the operation of the switch. Two clock signals are needed for proper operation, i.e. PHI and PHID. PHID has the exact same falling edge as PHI but a slightly delayed rising edge. Straightforward logic techniques can be easily employed to derive PHI and PHID from a standard clock signal.

The timing points at which the state of the switch is recorded are t_0, t_1, t_2 and t_3: t_0 is the initial condition, t_1 is after PHI goes high but before PHID goes high, t_2 is when both PHI, and PHID are high and t_3 is when both PHI and PHID go back to low again. Table E.1 summarizes the state of every node in the switch at times t_0, t_1, t_2 and t_3. The reader should note the following as they walk through different states in Table E.1:

Figure E.3. Improved Version of High-Voltage Bootstrapped Sampling Switch
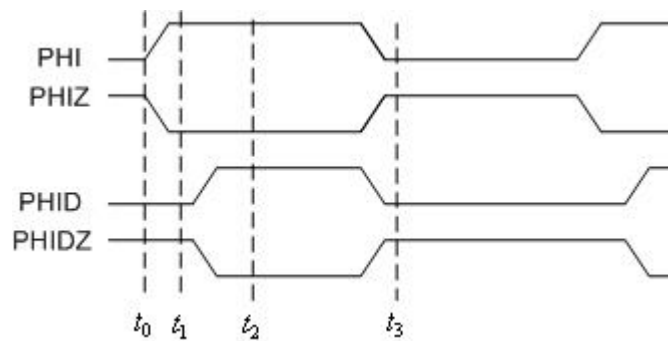
Figure E.4. Clock Timing Diagram of Second Sampling Switch

Table E.1. State of the Nodes at Timing Points

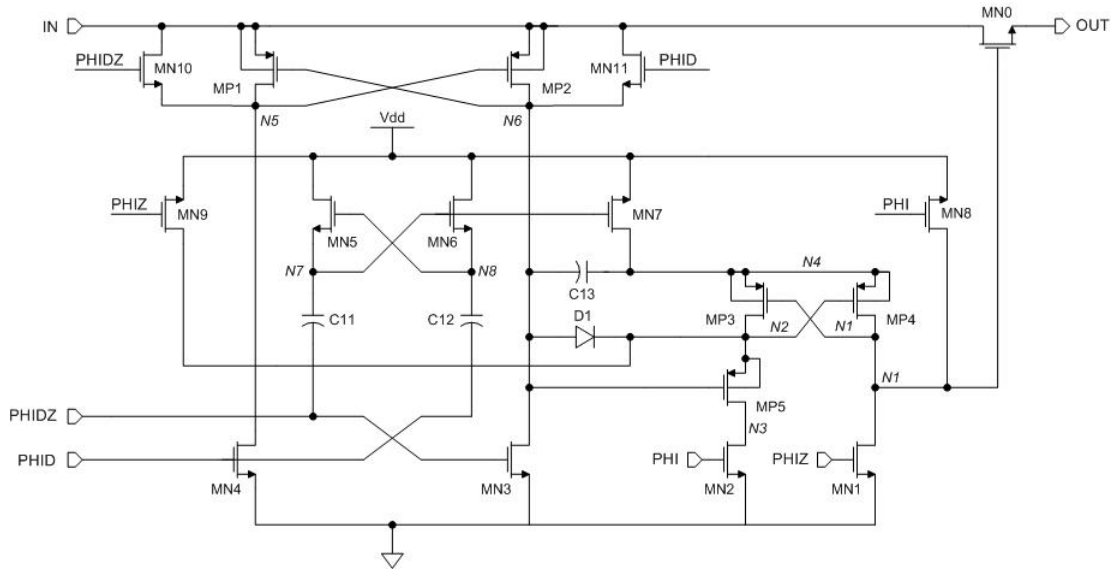| Node	$t = t_0$	$t = t_1$	$t = t_2$	$t = t_3$
PHI	0	V_{dd}	V_{dd}	0
PHIZ	V_{dd}	0	0	V_{dd}
PHID	0	0	V_{dd}	0
PHIDZ	V_{dd}	V_{dd}	0	V_{dd}
N_1	0	V_{dd}	$V_{dd} + V_{in}$	0
N_2	V_{dd}	$0 + V_{tp}$	$V_{in} - V_d$	V_{dd}
N_3	V_{dd}	0	0	V_{dd}
N_4	V_{dd}	V_{dd}	$V_{dd} + V_{in}$	V_{dd}
N_5	V_{in}	V_{in}	0	V_{in}
N_6	0	0	V_{in}	0
N_7	$2V_{dd}$	$2V_{dd}$	V_{dd}	$2V_{dd}$
N_8	V_{dd}	V_{dd}	$2V_{dd}$	V_{dd}

- At $t = t_0$, D_1 prevents N_2 from being shorted to ground via M_{N3} since both M_{N3} and M_{P3} are on (N_2 is at V_{dd} while N_6 is at ground)

- At $t = t_1$, N_2 goes initially to ground through M_{N2} and M_{P5} to turn on M_{P4} and N_1 is charging to V_{dd} via M_{N8} and M_{N7} which are both on. Note that the drain and source of both M_{N7} and M_{N8} reverse roles at t_1 since MOSFETs are symmetrical devices.

- At $t = t_2$, The bottom plate of C_{13} is pushed to V_{IN}, therefore $V_{dd} + V_{IN}$ appears at N_4 and N_2 is pulled to $V_{IN} - V_d$ through the diode D_1 to bound the gate-to-source voltage of M_{P4} within the supply voltage. Thanks to M_{P5}, the current path from the input node to ground will be cut after N_2 reaches to $V_{IN} - V_d$.

- At $t = t_2$, since M_{P4} is on, N_1 goes to $V_{dd} + V_{IN}$ M_{N8} turns off as N_1 goes to $V_{dd} + V_{IN}$ since its gate (PHI) is at V_{dd}, its source is at V_{dd} and its drain (N_1) is at voltage greater than its gate or source voltages.

- At $t = t_2$, V_{DS} of M_{P4} (V_{GS} of M_{P3}) is at 0, while the V_{GS} of M_{P4} (V_{DS} of M_{P3}) is at $V_{dd} + V_d$, where V_d is the forward diode voltage of D_1.

- At t_3 the charging of N_4 to V_{dd} happens through M_{N7}

- M_{N10} and M_{N11} help charge nodes N_5 and N_6 respectively to V_{IN} for very low values of V_{IN} where M_{P1} and M_{P2} are not strongly turned on.

E.3 Comparison of All three Sampling Switch

First version is the simplest one of all three sampling switches. Consequently, it occupies smaller silicon area compared to other two versions. This sampling switch has two down sides:

1. The input signal range is restricted with the Gate-to-Source Breakdown voltage of M_{P3}.

2. The switch gate overdrive is not constant throughout all the input range.

The first condition is somewhat more severe because this switch requires high-voltage rated devices to implement M_{P3}. The variation of the switch overdrive makes this version unsuitable for systems having dynamic input signals. For the power management systems on the other hand, this structure is suitable since the input signals are near DC.

The second version of the switch solves both of the problems described above. It has a constant switch overdrive voltage within the entire input signal range. The V_{GS} of the PMOS pass transistor M_{P4} is equal to $V_{dd} + V_d$. Therefore, the input signal range is restricted with the drain-to-source breakdown voltage of this device. Of course, everything has a price, the cost here is:

1. Increased area and complexity

2. 2 clock phases

3. Extra current consumption from the input terminal and the power supply.

The third version that is presented in section 3.3 combines the good features of these two earlier versions with of course better reliability and current consumption. The extra cost of the third version is its increased complexity.

Table E.2 summarizes the comparison of all three version of the high-voltage bootstrapped switches, together with the traditional one. Of course, the input signal range of all three switches presented here can exceed the supply voltage whereas the traditional implementation is bounded with it for proper operation.

E.4 Extending the Range of the Level Shifter Or Thin Oxide Implementation

As discussed in section 3.3, the input signal range of all the switches presented here is restricted with the gate-to-source breakdown voltage of the cross coupled PMOS transistors within the level shifter circuit, i.e. M_{P1} and M_{P2} in Fig. E.3. Since the technology with which the switches are designed has suitable transistors rated for the targeted input signal range, these PMOS transistors are implemented using high-voltage devices. It is also possible to

Table E.2. Comparison of the Bootstrapped Switches

Switch Version	Traditional	Version 1	Version 2	Version 3
Area Consumption	Best	Best	Good	Bad
Power Consumption	Best	Good	Bad	Good
Switch Gate Overdrive	Good	Bad	Good	Good
Clocking Complexity	Good	Good	Bad	Good
Device Reliability	Good	Bad	Good	Good
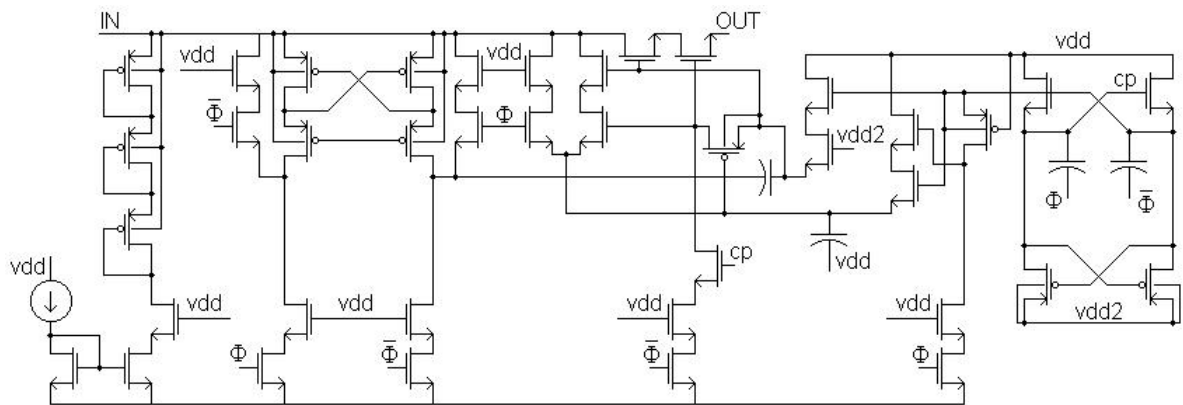
Figure E.5. 3.3V Core CMOS transistor implementation of the High Voltage Bootstrapped Switch

implement the whole ADC using core 3.3V CMOS transistors. Fig. E.5 this implementation. The cascoding technique to protect gate oxide is used at every high voltage node. As it is clear from the figure, this circuit is far more complex than the implementation using high voltage devices.

It is possible to shown that the relevant breakdown voltage for the implementation shown in Fig. E.5 is the drain breakdown voltage or BV_{dd} of the transistors. Notice that it is possible to sample up to twice the rated drain breakdown voltage of the employed transistors. Using high voltage drain extended transistors, the input signal range can be made very large. The sole trade off is the size of the flying capacitor that is connected in between source and gate of the switch transistor. The flying capacitor should be chosen large enough so that after the flying capacitor's top plate is pushed to high voltage, there should be enough gate overdrive voltage for the switch.
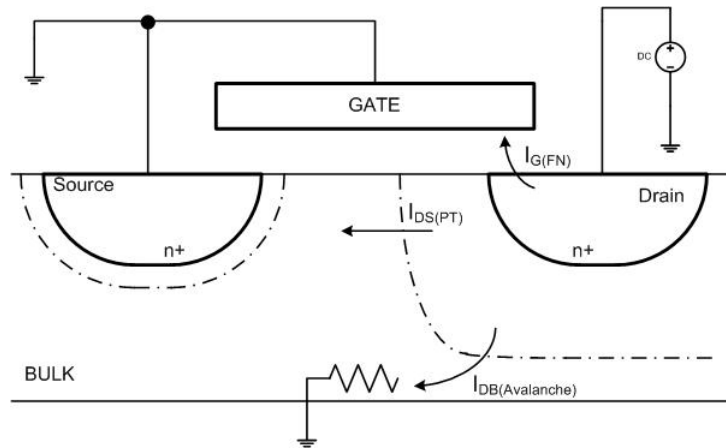
Figure E.6. Experiment for NMOS device reliability

E.5 Reliability issues, Switch performance degradation, Device/Circuit life-time

It is important to understand several existing high-voltage related breakdown mechanisms intrinsic to the proposed switch. Some of these mechanisms, i.e. avalanche breakdown and channel hot electron injection, are non-destructive but degrade the performance of the sampling switch whereas another mechanism, i.e. gate oxide degradation under high voltage stress, eventually yields the destruction of the device but has minimal effect on the performance of the device.

In order to understand the reliability issues related to the presented bootstrapped switch, as well as to the classical bootstrapped switch, it is necessary to analyze the breakdown mechanisms present within the basic circuit configuration shown in Fig. E.6. The experiment conducted here is increasing the drain terminal voltage of the NMOS transistor while gate, source and bulk terminals are all grounded, in other words, while the transistor is in cut-off region. This operation configuration exists at several places in the proposed bootstrapped switch, and as well as in the classical bootstrapped switch.

Under these conditions, there exist three distinct breakdown mechanisms, two of them happen at the drain diffusion region and the other happens at the drain-gate overlap capacitance region.

While increasing the drain voltage, the electrical field across the reverse biased drain-bulk PN junction also increases. Under such conditions, there are two different phenomena that give rise to the drain current: 1) The punchthough current or subsurface drain induced barrier lowering 2) avalanche breakdown current due to the impact ionization.

While the drain voltage rises, the depletion region width at the drain side also in-

creases. The punchthrough current occurs at the channel side of the drain diffusion and is associated to the merging of the source and drain depletion regions of the MOSFET [83]. Therefore, this phenomenon is more pronounced for short channel devices and of course it is closely related to the bulk doping concentration. In order to prevent punchthrough current for high drain voltage levels, more than minimum channel length values have to be chosen.

With the increase of the drain voltage, the electrical field across the reverse biased drain-bulk PN junction reaches to a critical values at which the carriers traveling through the depletion region acquires sufficient energy to create new electron-hole pairs by impact ionization [84]. These highly energetic carriers can collide few more time to generate more carriers before reaching to the electrodes. This multiplication process results an avalanche breakdown current flowing through the drain terminal. The breakdown voltage is inversely proportional with the doping concentration of both regions and the critical electrical field is independent of the doping to a first approximation. The junction breakdown voltage of the used process is higher than 9V in worst case.

The effect of the punchthrough and/or avalanche breakdown currents to the sampling switch performance can be assessed as follows: The high voltage levels within the bootstrapped switch are generated using charge pumping technique meaning that the output impedance of the high voltage source, i.e. the pumping capacitor, is high. Therefore, the high voltage level cannot sustain to compensate the punchthrough or avalanche breakdown currents. As a result, if the transistors are driven to give rise to these breakdown currents, the effect will manifest itself as decreased effective gate-overdrive of the switch NMOS transistor for high input voltage levels, in addition to the losses due to the parasitic capacitances loading its gate terminal. This will of course degrade the on resistance linearity of the sampling switch and yield to nonlinear distortion during the sampling of the time varying signals. If these breakdown currents happen at the drain side of the NMOS switch transistors, they will appear as an extra load to the input source.

If the breakdown currents can be sustained, i.e. if the input signal itself is high enough to cause these currents, increasing the drain voltage further will yield to the destruction of the device with the debiasing of the transistor bulk. When the drain voltage exceeds the transistor snap-back voltage, the parasitic NPN bipolar transistor formed by drain, bulk and source diffusion regions turns on and the drain current rapidly increases. This high current heats the parasitic bipolar device which in turn raises further the drain current due to the positive feedback created by the self-heating effect. Eventually thermal-runaway occurs and the device is destroyed. Typically, the destruction occurs with the melting of the metal and/or via connections.

Besides to the larger channel length selection, there exists layout techniques exploiting

lightly doped drain (LDD) implant to improve further the breakdown voltage [23]. Alternatively, the breakdown problem can be solved using drain-extended MOS (DEMOS) transistor structure. The doping profile of the drain diffusion of this type of transistor is engineered so that the breakdown voltage at the drain side can be made very large. The advantages of DEMOS transistor are improved reliability, digital process compatibility and its low(no)-cost [85]. Its disadvantages are large silicon area and increased RDS_ON (or slower response). DEMOS transistors provide also an easy solution to the oxide reliability problems that will be analyzed next.

The second breakdown mechanism, present within the circuit shown in Fig. E.6. is the oxide breakdown. With the increase of the drain voltage, the electrical field across the gate-drain oxide overlap region reaches to a critical value at which the electrons are injected into the conduction band of the oxide with Fowler-Nordheim (FN) tunneling mechanism [83]. While accelerating towards the anode, i.e. drain side, some of these highly energetic electrons generate electron-hole pairs and again due to their relatively low mobility some of these generated holes get trapped within the oxide creating a localized positive charge which in turn causing the tunneling current density to increase at these points. This positive feedback mechanism yields in time to higher trap densities at that point and eventually the oxide breakdown occurs. It worth noting that the generation of these traps is cumulative and irreversible. The reliability of the oxide is generally characterized with the amount of charge passed through it and it is quantified with charge-to-breakdown parameter, i.e. QBD.

It is possible to asses the performance degradation of the bootstrapped sampling switch under the assumption that a gate current starts flowing due to the FN tunneling as follows: The effect of the gate current will be similar to the effects of the punchthrough or avalanche breakdown currents. These effects are discussed above. It is also worth noting that generally speaking the current level due to FN tunneling is very low compared to the other breakdown currents. Until the oxide breakdown occurs at the drain side of the transistors, the effect of the trap generation mechanism on the performance of the switch is negligible. The threshold voltage of the transistors at the drain side decreases due to the trapped positive charges within the oxide. Of course, in time the stressed oxide degrades and breakdown. This will cause a short between the gate and drain terminals of the stressed transistors [83].

There are several nodes within the proposed bootstrapped switch having high voltage swing that can potentially create oxide reliability problems for the connected transistors. It is also worth noting that the gate oxide breakdown voltage is much higher compared to the process rated voltage for the reliable operation of a gate oxide when the over voltage stress is applied as described in Fig. E.6, i.e. only the gate-drain overlap region is stressed [86]. There are two ways to improve the reliability. It is possible to use DEMOS transistors as

pointed out earlier. Alternatively, it is also possible to use the cascoding technique used within the classical bootstrapped switch to reduce the oxide stress.

The circuit designers are interested of course with the estimated life time of the circuit/device for a given worst case temperature and operation conditions. An empirical model is provided in [83] to estimate the oxide life time or time-to-breakdown (tbd). The tbd of the oxide is a very strong function of the operating temperature, electrical field across the oxide and the duty cycle or the duration of the over voltage stress. Besides, of course, the oxide life time is also closely related to the quality of the gate oxide growth process. There are 3 groups of oxide failure mode, i.e. A-mode, B-mode and C-mode. Aforementioned model predicts the tbd for the C-mode(defect free oxide) failure group. C-mode failure group is also referred as intrinsic oxide breakdown. Using the model, the worst-case tbd of the fabricated bootstrapped switch is estimated to be slightly less than 5 years. This number agrees well with the oxide reliability curves of the process.

The channel hot electron injection phenomenon is widely known effect occurring under large lateral electrical fields along the transistor channel [84]. Since, in time it causes an increase on the threshold voltage of the effected transistor, it is important mainly for the NMOS switch transistor, in terms of performance degradation of the sampling switch.

APPENDIX F

SSA Tool Known Problem and Issues

The current version of the SSA Tool has the following limitations and features:

1. A variable name cannot start with '_' sign and cannot contain any of the following signs: \, %, #, &, $, !, |, ˜, <, > and aritmetic operation signs.

2. A variable name cannot start with prefixes 'inl' and 'ssa'.

3. eq11, eq12, eq13, eq14, eq21, eq22, eq23, eq24, eq25, eq31, eq32, eq33, eq34, eq35, eq36, components, update are reserved words.

4. Matlab and maple reserved words are also reserved words of SSA Tool.

5. Variables **s** and **z** are used for s-domain and z-domain calculations. Furthermore, the discrete and continuous time domain variables defined in Table 4.2 are reserved words, i.e. w1, w2, z11, z12, etc...

6. If a variable name and a net name coincide, symbolic solver treats them as identical. Therefore, these kind of parameter assignments result as voltage control behavior.

7. Common function names such as cos, exp, log, etc..., are treated as a function and not as a variable name

8. Instance name input has special meaning for nonlinearity analysis procedure. Tool assumes that the instances having the name input are actually the input signal and nullify them during the non-linearity analysis. Other signal sources are not nullified. Therefore, for nonlinearity analysis special voltage and current sources, nonvols and noncurs, provided within the SSALIB design library should be used. Or source instance name input should be used accordingly.

9. Tool does not control the linearity of the equation system. Non-Linearity calculations are based on the linear response of the circuit, as explained within the distortion analysis section. Hence, to guarantee a solution the node equation system should be linear with respect to node voltages otherwise symbolic solver might not found a solution. (For example, using product blocks or polynomial block or source with a magnitude of for example: net1*net2 create nonlinear equation systems).

10. Tool doesn't control the consistency of the transfer function names. If different transfer function blocks assign their output to the same MATLAB global variable, the global variable will show only one of the transfer function block definition according to the appearance (last definition) within the created netlist.

11. Tool doesn't control nomenclature check for the blocks Discrete Time Filter, Discrete Time Transfer Function, Transfer Function. Any error of numerator or denominator nomenclature will yield to crash.

12. AHDL codes present within the SSALIB don't have any simulation wise meaning. SSALIB design library is creates for the sole purpose of using the graphical user interface of the Cadence Virtuoso Schematic editor. Those cell views are created for being consistent with the netlisting procedure of Spectre.

13. Passive and active devices, such as resistor, capacitor, mos transistor, bipolar transistor,etc are not present in Simulink SSALibrary because Simulink schematic editor does not support bidirectional connection. Simulink schematic editor requires that every node has one and only one output port connected to it and one or more input port connected to it. This condition makes it impossible the realization of the bidirectional component such as resistors.

14. Spectre netlister and Simulink model file does not support hierarchical design. However, SpectreS netlister support hierarchical netlisting.

15. The tool does not control rigid voltage loop and current branches. Topology errors will result, of course, unsolvable linear equation system.

16. Symbolic solver assumes that every parameter is positive real number. If the variable have negative value, put a negative sign in front of it or modify the variable name, i.e. variable, as follows: Negative variables : $variable\_neg$; real variables : $variable\_real$; complex variables : $variable\_comp$.

APPENDIX G

Non-Linearity Coefficients of a Bipolar Transistor

The equations and the complexity of the nonlinearity coefficients of the bipolar transistor depend of course on the nonlinear model used to extract. A simple collector current model is given in [81] as

$$I_C = I_S \left(1 + \frac{V_{CE} - V_{BE}}{V_{AF}}\right) \exp\left(\frac{V_{BE}}{V_T}\right) \tag{G.1}$$

in which I_S, V_{AF} and V_T are the transistor saturation current, the forward Early voltage and the thermal voltage, respectively. The nonlinearity coefficient expressions derived from this expression are given in Table G.1.

Notice that the nonlinearity coefficients related to the output conductance are all zero due to the linear modeling of this effect within the collector current model. Therefore, the effect of the output conductance nonlinearity of the bipolar transistor cannot be investigated using this simple model. A more accurate model ,i.e. Cilingiroglu model given in [82], expresses the collector current as

$$I_C = I_S \left[1 + \frac{V_{CB}}{G\sqrt{\frac{2q}{N_C \epsilon_{Si}}(V_{CB} + \Phi_J)} - 3V_{CB} - 2\Phi_J}\right] \exp\left(\frac{V_{BE}}{V_T}\right) \tag{G.2}$$

where G is the base metallurgical Gummel number, N_C doping concentration of the collector, ϵ_{Si} is the dielectric permittivity of the silicon, Φ_J is the collector-base built in junction potential. The expressions of the nonlinearity coefficients obtained from the equation G.2 will not be presented here because they are rather long. But they can be obtained easily using the definitions given in Table G.1.

Table G.1. Nonlinearity Coefficient obtained from the collector current model given in G.1

Nonlinearity Coefficients		
Coefficient	Definition	Expression
g_m	$\dfrac{\delta i_c}{\delta v_{BE}}$	$\dfrac{I_C}{V_T}$
K_{2gm}	$\dfrac{1}{2}\dfrac{\delta^2 i_c}{\delta v_{BE}^2}$	$\dfrac{g_m}{2V_T}$
K_{3gm}	$\dfrac{1}{6}\dfrac{\delta^3 i_c}{\delta v_{BE}^3}$	$\dfrac{g_m}{6V_T^2}$
g_o	$\dfrac{\delta i_c}{\delta v_{CE}}$	$\dfrac{I_C}{V_{AF}}$
K_{2go}	$\dfrac{1}{2}\dfrac{\delta^2 i_c}{\delta v_{CE}^2}$	0
K_{3go}	$\dfrac{1}{6}\dfrac{\delta^3 i_c}{\delta v_{CE}^3}$	0
K_{2gmgo}	$\dfrac{\delta^2 i_c}{\delta v_{BE}\delta v_{CE}}$	$\dfrac{g_m}{V_{AF}}$
K_{32gmgo}	$\dfrac{1}{2}\dfrac{\delta^3 i_c}{\delta v_{BE}^2\delta v_{CE}}$	$\dfrac{g_m}{2V_T V_{AF}}$
K_{3gm2go}	$\dfrac{1}{2}\dfrac{\delta^3 i_c}{\delta v_{BE}\delta v_{CE}^2}$	0

APPENDIX H

SSA Tool Library

Because of the large volume of the SSATool library data sheet, this section is presented in electronic format. Please contact Devrim AKSIN from devrimaksin@ieee.org to obtain an electronic copy of the library data sheet.

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