Implementation of Dynamically Configurable Modulator on FPGA

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***Abstract*—Digital modulation schemes are used to make messages suitable for communication. Each modulation scheme is designed with a different approach and has advantages over others. The modulation scheme of a system is selected according to the requirements of the system. It can be required to implement multiple modulations in a single system. Yet, implementing two or more modulations individually has power and area cost. To decrease these costs, a dynamically configurable architecture can be employed. On the other hand, dynamic configuration requires configuration data. That data can be stored in memory or read from an input. In both cases, memory and time overhead occurs. In this study, a dynamically configurable modulator architecture is implemented with a novel approach. The modulator of the system can be configured as Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), Minimum Shift Keying (MSK) or Gaussian Minimum Shift Keying (GMSK) modulator. An array of blocks is implemented in the proposed system. These blocks can be activated or deactivated on run time. The combination of activated blocks results in BPSK, QPSK, MSK, or GMSK modulator. Therefore, the configuration does not cause any extra delay and does not require configuration data. The proposed system is implemented on XC7A200T Xilinx FPGA and the outputs of modulators are examined using Xilinx Vivado tool. The implementation result shows that proposed system utilizes 20% fewer resources and decreases power consumption by 20% compared to the system which implements modulators individually.**

***Index Terms*—BPSK, QPSK, MSK, GMSK, configurable, FPGA**

I. Introduction

In wireless communication, a message needs to be converted into a signal that is suitable for the transmission medium. To convert messages, modulator schemes are employed. A modulator outputs a sinusoidal signal as the result of message conversion. Amplitude, frequency, or phase of that signal are used to transmit the converted message.

The modulation schemes are grouped into two main categories as digital and analog modulation. The basic types of digital modulation are Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), and Phase Shift Keying (PSK). In the ASK modulation scheme, amplitude of modulator output signal is controlled according to the message bits. Different levels of amplitude represent the message bit as logic 0 or logic 1. The message is transmitted on the frequency of the modulator output by using FSK modulation. The frequency of FSK output signal is determined by the message bits. The PSK converts the message to a burst of carrier frequency of modulation. Among the three basic modulations, ASK, FSK, and PSK, various modulation schemes are derived from these basic modulations [1]. The Binary PSK (BPSK), Quadrature PSK (QPSK), Minimum Shift Keying (MSK) and Gaussian filtered MSK (GMSK) are derived from the PSK. While BPSK uses two signals which differ in phase as π, QPSK utilizes four signals which differ in phase as $\pi/2$. MSK and GMSK are continuous phase modulation schemes.

Modulation schemes are evaluated by their bandwidth, power efficiency, and system complexity. Therefore, a system may require a specific modulation scheme to be implemented. A configurable modulator system is able to satisfy the different requirements in a single system. The author of [2] proposed a configurable modulator that includes 2-FSK and 4-FSK modulators. The modulator of the proposed system is determined by an input of the system and configuration does not require configuration data. The carrier signal values of the system are stored in memory. The proposed system outputs these values according to selected modulator. The proposed system in [3] is a reconfigurable modulator system. The modulators of the proposed system are Amplitude Modulation (AM), Frequency Modulation (FM), FSK, PSK, and ASK. The system stores the reconfiguration data in onboard memory and it is capable of reconfiguring its modulator dynamically. The reconfiguration data size and reconfiguration time overhead are presented in the result of proposed work. Also, in [4], the authors presented a reconfigurable modulator architecture. The proposed architecture can be dynamically configured as FSK, MSK, OQPSK and UQPSK. The reconfiguration data of the proposed system is stored in memory and reconfiguration is triggered by system commands. To reconfigure the modulator of the proposed system, 639.68 μs and 2047 kB of data are required for each modulator. The authors of [5] presented a parametrizable modulator architecture. The proposed work implements both QPSK and GMSK individually and both modulators operate at run time. A multiplexer in the proposed system selects the system output as one of the implemented modulators. The individually implemented modulators increase the power consumption and resource utilization when compared to the configurable modulator systems. While the proposed systems

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in [3] and [4] are not functional during reconfiguration and they have reconfiguration overheads, our work overcomes these problems with its novel approach.

In this study, a novel approach to dynamically configurable modulator system is designed and implemented on FPGA. The PSK modulation scheme is more power-efficient than ASK and FSK. Also, PSK and ASK modulation schemes have the same spectral efficiency and it is better than FSK. Therefore, the proposed system is decided to implement PSK modulation schemes. There are advantages and disadvantages of the modulation schemes which are derived from the PSK. BPSK modulation scheme is immune to errors and its implementation is simple. Although QPSK has a complex implementation, QPSK doubles the data rate of BPSK while preserving the error immunity. The drawback of BPSK, and QPSK is that they have sidebands in the spectrum which can cause adjacent channel interference. The sidebands of BPSK, and QPSK can be filtered or that problem can be resolved by using another modulator, such as MSK. Even though MSK minimizes the sidebands, an improvement in spectral efficiency of MSK can be achieved by using GMSK. To benefit from different types of PSK modulation schemes, our proposed system implements BPSK, QPSK, MSK, and GMSK.

The architecture of our proposed system is designed as an array of blocks that can be activated or deactivated. This novel approach allows configuring the modulator of the proposed system without configuration data. Therefore, configuration can be established on run time without data and time overheads. Also, the proposed system utilizes fewer resource and consumes less power compared to the ones which implements the modulators individually. This paper is organized as follows: Section II explains the modulator schemes. The implementation of the proposed system is defined in Section III. Section IV provides the test results of implemented modulators. The paper is concluded and future works are explained in Section V.

II. Modulator Schemes

The BPKS, QPSK, MSK, and GMSK modulator schemes are described in the following subsections.

A. BPSK Modulator Scheme

A BPSK modulator modulates a message one bit at a time. To modulate, it utilizes two sinusoidal signals whose frequencies and amplitudes are the same. But, their phases differ as π. The message defines the output of BPSK modulator as one of these signals and one bit of message is conveyed by the selected signal. When the message bit is logic-0 or logic-1, the BPSK modulator outputs the signal in Eq. 1 or 2 respectively.

$$s_0(t) = -Acos(2\pi f_c t) \tag{1}$$

$$s_1(t) = Acos(2\pi f_c t) \tag{2}$$

When a transition occurs on the input of the modulator, the output's phase is shifted as π.

B. QPSK Modulator Scheme

The QPSK modulator scheme conveys two bits of message at a time. These two bits are represented with four signals which have diverse phases. The phases of these signals are defined as in Eq. 3 where θ represents the phase and $i = 1, 2, 3, 4$.

$$\theta_i = \frac{(2i-1)\pi}{4} \tag{3}$$

The output of the QPSK modulator is defined as in Eq. 4 where f_c is carrier frequency.

$$s_i(t) = Acos(2\pi f_c t + \theta_i) \tag{4}$$

The output can be written as in Eq. 5

$$s_i(t) = Acos(2\pi f_c t)cos(\theta_i) - Asin(2\pi f_c t)sin(\theta_i) \tag{5}$$

The $cos(\theta_i)$ and $sin(\theta_i)$ can be equal to either 0 or 1. Therefore, they can be used to represent the modulator input bits. There are four possible combinations of $cos(\theta_i)$ and $sin(\theta_i)$ functions which are 00, 01, 10, and 11. The left bit of these combinations is cosine function and right bit is sine function. The QPSK modulator, first, modulates two bits of message separately with its carrier signal. In the end, it subtracts the modulated bits. Therefore, two message bits is conveyed using one symbol.

C. MSK Modulator Scheme

The MSK modulator weights the message with sine and cosine signals. The weighted message bits are then modulated with carrier signal. The output of MSK modulator is in Eq. 6 where $d_k = -I_k Q_k$.

$$s(t) = Acos[2\pi t(f_c + d_k \frac{t}{4T}) + \phi_k] \tag{6}$$

The ϕ_k is equal to 0 or π when the sign of I is *+1* or *-1* respectively. The output can be written as in Eq. 7 where *T* is the bit period of the message, *I* is NRZ coded even bit and *Q* is NRZ coded odd bit.

$$s(t) = AI(t)cos(\frac{\pi t}{2T})cos(2\pi f_c t) + AQ(t)sin(\frac{\pi t}{2T})sin(2\pi f_c t) \tag{7}$$

The MSK modulator extracts the even and odd bits from its input bit sequence. These even and odd bits are modulated in in-phase (I) and quadrature (Q) channels respectively. In the I and Q channels, even bit is multiplied with cosine signal and odd bit is multiplied with sine signal. That sine and cosine signals in that channels have the same period. The period which is defined as *4T* where *T* is the period of a bit in message. Since bit width of even and odd signals is *2T*, the half period of that sine and cosine signals is multiplied with even and odd bits. The multiplied even and odd signals are then modulated with carrier signal. Finally, the final results are summed to generate MSK output. Since the input is weighted by sinusoidal signals, the output of the MSK modulator is continuous.

D. GMSK Modulator Scheme

The GMSK is a continuous phase modulation technique. The baseband message is filtered with a Gaussian filter to increase the spectral efficiency of the modulation signal. The frequency deviation of the message is also lowered as minimum as possible [6]. The output of the GMSK modulator is in Eq. 8 where *s(t)* is modulator output, f_c is carrier frequency, f_d is peak frequency deviation and *g(τ)* represents the Gaussian filtered message.

$$s(t) = Acos(2\pi f_c t + 2\pi f_d(\int_0^t g(\tau)\, d\tau\ )) \tag{8}$$

The GMSK modulator output can be writen as in the Eq. 9.

$$y(t) = Acos(2\pi f_c t)cos(2\pi f_d) - Asin(2\pi f_c t)sin(2\pi f_d) \tag{9}$$

The input signals of I and Q channels are derived from the Gaussian filter output as in Eq. 10 and Eq. 11 respectively. Then, the derived signals are multiplied with carrier signal. The result of multiplication of I is subtracted from result of multiplication of Q. That subtracted results the GMSK output.

$$I(t) = cos(2\pi f_d(\int_0^t g(\tau)\, d\tau\ )) \tag{10}$$

$$Q(t) = sin(2\pi f_d(\int_0^t g(\tau)\, d\tau\ )) \tag{11}$$

III. Implementation

The proposed system is a configurable modulator and it can be configured as BPSK, QPSK, MSK, or GMSK modulator. The architecture of the system is a pipelined array of stages and each stage consists of various block. There are multiplexers at the outputs of the stages. The multiplexers are responsible for defining the input of the following stage in the pipeline. So that, the selection input of the proposed system activates the combination of blocks and holds remaining blocks in reset. The configuration of a modulator is utilized by the activated blocks. With this approach, the proposed system does not require any configuration data. Therefore, the configuration overhead is removed by the proposed system. Also, the blocks which are held in reset decrease the dynamic power consumption. The architecture of the proposed system is in Fig. 1. The Non-Return to Zero (NRZ) block is used to encode the input. When the input of NRZ is 1 or 0, the output of the NRZ block is 1 or -1 respectively. The integrator is implemented as a first-order Finite Impulse Response (FIR) filter and it calculates the integral of its input. The Gaussian filter is a low pass filter whose impulse response is a Gaussian function. That filter is utilized to shape its input pulses. To calculate trigonometric functions, 8 rounded CORDIC algorithm is implemented. The CORDIC algorithm is used to calculate trigonometric functions with low hardware costs [7]. There are two CORDIC blocks in the system, one for carrier signal and the other for implementing MSK and GMSK modulators. The multiplexer selects its output as one of its inputs according to its selection input. The proposed system implements these

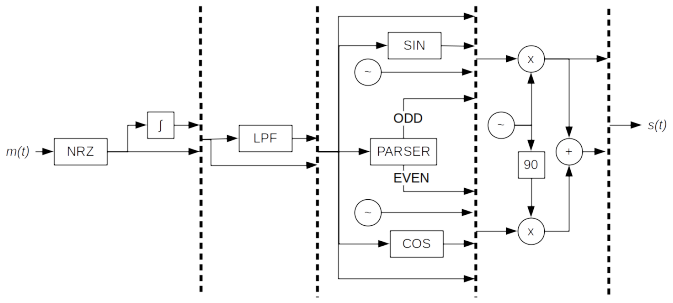

Fig. 1. System architecture

described blocks. There are 1 NRZ, 1 integrator, 1 Gaussian Filter block, 2 CORDIC ,and 6 multiplexer blocks in the proposed design. These blocks except the Gaussian Filter are designed and implemented by using VHDL. To implement Gaussian Filter, FIR Compiler tool which is provided by the Xilinx Vivado is used. That filter uses 7 slices of DSP48E1.

The architecture of the proposed system is divided into stages with the dashed vertical lines as in Fig. 1. The dashed lines also represent the multiplexers at the output of stages. The main contribution of this work is achieved with these multiplexers. The selection of individually implemented modulator systems is on the modulator level. But, the proposed system establishes the selection mechanism on the block level. This novel approach results in area saving since common blocks of modulators are implemented only once. Moreover, the configuration of the desired modulation scheme is a specific combination of multiplexers. Therefore, the configuration data is not required to configure one of the modulators. As a result, data overhead is removed by the multiplexers.

A. Configuring as BPSK Modulator

The BPSK modulator conveys the message with two identical signals with different phases. So that, to implement BPSK modulator, the NRZ, carrier signal generator, multiplier and adder are selected in the proposed system. NRZ block encodes the input as *+1* or *-1* and the output of the NRZ is multiplied with the carrier signal. When the output of NRZ is *+1* or *-1* BPSK modulator output becomes $cos(2\pi f_c t)$ or $-cos(2\pi f_c t)$ respectively.

B. Configuring as QPSK Modulator

NRZ block encodes the input and the bit extractor block provides the input of I and Q channels. That inputs of channels are multiplied with carrier signal and the output of Q channel multiplication is subtracted from the result of I channel multiplication. Therefore NRZ, bit extractor, carrier signal generator, multipliers, and adder blocks are necessary to implement QPSK modulator.

C. Configuring as MSK Modulator

The MSK modulator encodes the message with NRZ and provides the input of the bit extractor. The extractor outputs the even and odd bits. The even bit is multiplied with cosine signal and odd bit is multiplied with sine signal. This operation

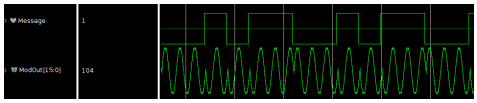

Fig. 2. BPSK modulator signals

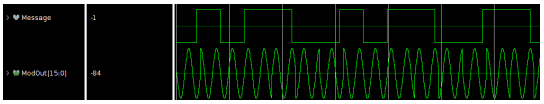

Fig. 3. QPSK modulator signals

changes phases of these signals as 0 or π. These phase-shifted sine and cosine signals are multiplied with carrier signal and summed to generate MSK modulated signal. In MSK modulator configuration, the proposed system activates NRZ, bit extractor, two signal generators, multipliers, and adder.

D. Configuring as GMSK Modulator

The GMSK encodes the message with NRZ and calculates the integral of NRZ's output. The output of integrator is then filtered with Gaussian filter. The sine and cosine functions of filter output are calculated and these values are multiplied with carrier signal. The multiplication results are subtracted from each other to generate the output of GMSK modulator. The implemented GMSK modulator consists of NRZ, integrator, Gaussian filter, two signal generators, multipliers, and adder.

IV. Test Results

The proposed system is implemented on XC7A200T Xilinx FPGA and it is tested by using Xilinx Vivado tool. The same bitstream is applied to the message input of each modulator. The bit rate of the input message is 1Mbps and the carrier frequency of all modulators is 2.5 MHz. The modulator outputs are observed. In the test results, the waveform named as *Message* represents the NRZ coded input message of modulators. Also, the *Mod Out* signal presents the output of modulators.

The BPSK modulator output is in Fig. 2. The phase of the modulation signals depends on the input.

The Fig. 3 displays the signals in QPSK modulator. The modulator output is formed by subtracting *Q Ch* from *I Ch*.

The MSK modulator output is presented in Fig. 4. The *I Ch* and *Q Ch* are multiplied with carrier. Results of multiplications are summed to generate modulator output.

The Fig. 5 displays the GMSK modulator output.

The resource usage of the proposed system is in Table I. The column named as *Individual* shows the resource usage of the system which implements BPSK, QPSK, MKS, and GMSK individually. The *Saving* shows the saving that the proposed

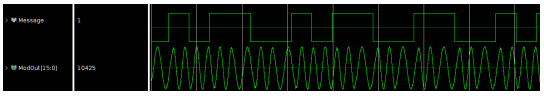

Fig. 4. MSK modulator signals

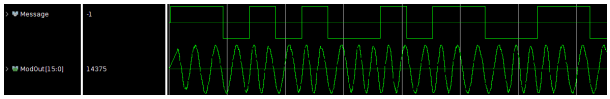

Fig. 5. GMSK modulator signals

TABLE I: Comparison of resource usage

Utilization	Proposed System	Individual	Saving
Slices LUTs	845	1180	28%
Slice Registers	861	976	11%

work provides. Implementation results show that the proposed system utilizes 20% less resources in total. While the proposed system consumes 0.041 W dynamic power, the individually implemented modulator system uses 0.053 W dynamic power.

V. Conclusion and Future Works

This study proposes a novel approach to implement a configurable modulator architecture. The BPSK, QPSK, MSK, and GMSK are combined and implemented as an array of blocks. By activating the sequence of blocks, the proposed system modulates the message with the selected modulator. It is shown that the proposed work reduces resource usage and decreases power consumption. Also, the proposed system does not have the configuration time and area overheads.

As a future work, it is planned to add a controller to the system. That controller will modify the parameters of modulators such as carrier frequency and filter parameters. It is also planned to add FSK, M-ary PSK, Offset QPSK modulators to the system. In the end, the resulting system will be wrapped up as an accelerator and it will be attachable to a system that needs to modulate the message.

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