Ayse YILMAZER METIN, Ph.D.

Assistant Professor
Istanbul Technical University
Computer Engineering Department
Maslak, Istanbul, 34469
Email: yilmazerayse@itu.edu.tr

SUMMARY

I am currently working as an Assistant Professor at Computer Engineering Department of Istanbul Technical University (Istanbul) and planning to take a sabbatical leave for 9-12 months starting from mid August of 2025. For my sabbatical leave, I am looking for a visiting scholar/researcher position where I could focus on hybrid (hardware & software) design approaches for improving memory system efficiency targeting particularly Machine Learning applications and FHE operations.

RESEARCH INTERESTS

Custom accelerator and Domain Specific Processor design, Heterogeneous computing, GPGPU computing, GPU microarchitecture, parallel architectures, memory hierarchy design, memory consistency and synchronization, performance analysis, compiler analysis techniques and runtime optimizations.

EDUCATION

PhD in Electrical and Computer Engineering January 2014
Northeastern University, Boston, MA
Adviser: David Kaeli

- **Dissertation title**: Micro-architectural support for improving synchronization and efficiency of SIMD execution on GPUs.

MS in Electrical and Computer Engineering May 2007
University of Rhode Island, Kingston, RI
Adviser: Resit Sendag

- **Thesis title:** Investigating the Effects of Wrong-path Memory References in Shared-memory Multiprocessors.

B.Sc. in Computer Science and Engineering January 1998
Hacettepe University, Ankara, Turkey

HONORS AND AWARDS

- **IPDPS 2006 Best Paper Award** for "Quantifying and Reducing the Effects of Wrong-Path Memory References in Cache-Coherent Multiprocessor Systems".

GRANTS

Completed:

- **Programmable Synchronization Architecture.** Granted by TUBITAK within Career Development Program (3501) Project Number: 117E053. Role: PI.

PATENTS

- ***System and Method for Cache Replacement***, with Resit Sendag and Augustus K. Uht, US Patent #7,721,048, issued in May 2010. https://patents.google.com/patent/US7721048B1/en
- ***Method and Apparatus for Regulating Processing Core Load Imbalance***, with M. S. Orr, S. Che, B. M. Beckmann, US Patent #9,678,806, issued in June 2017. https://patents.google.com/patent/US9678806B2/en
- ***Processor and Methods for Remote Scoped Synchronization***, with M. S. Orr, S. Che, B. M. Beckmann, M. D. Hill, D. A. Wood, US Patent #9,804,883, issued in October 2017. https://patents.google.com/patent/US9804883B2/en

JOURNAL PAPERS

- YILMAZER, AYŞE (2022) "Using a static naming approach to implement remote scope promotion," *Turkish Journal of Electrical Engineering and Computer Sciences*: Vol. 30: No. 5, Article 6. https://doi.org/10.55730/1300-0632.3903
- Yilmazer-Metin A. sRSP: An efficient and scalable implementation of remote scope promotion. *Concurrency Computat Pract Exper*. 2022; 34(9):e6483. https://doi.org/10.1002/cpe.6483
- Ayse Yilmazer-Metin, "Graph-Waving architecture: Efficient execution of graph applications on GPUs", Journal of Parallel and Distributed Computing, Volume 148, 2021, Pages 69-82, ISSN 0743-7315, https://doi.org/10.1016/j.jpdc.2020.10.005.
- Fatemeh Azmandian, Ayse Yilmazer, Jennifer G. Dy, Javed A. Aslam, David R. Kaeli, "Harnessing the Power of GPUs to Speed Up Feature Selection for Outlier Detection", *Journal of Computer Science and Technology (JCST)*, 2014, Vol. 29 (3): 408-422. (SCI-Expanded). https://doi.org/10.1007/s11390-014-1439-4
- Resit Sendag, Ayse Yilmazer, Joshua J. Yi, and Augustus K. Uht, "The Impact of Wrong-Path Memory References in Cache-Coherent Multiprocessor Systems", *Journal of Parallel and Distributed Computing (JPDC), Special Issue on Best Papers in IEEE International Parallel and Distributed Processing Symposium*, vol. 67, no. 12, pp. 1256-1269, Dec., 2007. (SCI-Expanded). https://doi.org/10.1016/j.jpdc.2007.03.005

REFEREED CONFERENCE PAPERS

- Eymen Unay, Ni Tarim, **Ayse Yilmazer-Metin**, "CKKS Fully Homomorphic Encryption Based Comparison and Bitonic Sorting", 2024. ***Submitted to:*** *International Conference on Electrical and Electronics Engineering, (ELECO 2024).*
- Beyazit B. Yuksel, **Ayse Yilmazer-Metin**, "ECG-PPS: Privacy Preserving Disease Diagnosis and Monitoring System for Real-Time ECG Signals", 2024. ***Accepted to:*** *17th International Conference on Security of Information and Networks (SIN 2024).*
- C. I. R. Koksal, N. M. Cicek, **A. Yilmazer-Metin** and B. Ors, "Optimizing Data Availability and Utilization in Deep Learning Accelerator SoCs," *2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Istanbul, Turkiye, 2023, pp. 1-4, doi: 10.1109/ICECS58634.2023.10382797.
- C. I. R. Koksal, N. M. Cicek, **A. Yilmazer-Metin** and B. Ors, "Lookupx: Next-Generation Quantization and Lookup Techniques for Empowering Performance and Energy Efficiency," *2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Istanbul, Turkiye, 2023, pp. 1-4, doi: 10.1109/ICECS58634.2023.10382787.
- T. Tekdoğan, S. Göktaş and **A. Yilmazer-Metin**, "gSuite: A Flexible and Framework Independent Benchmark Suite for Graph Neural Network Inference on GPUs," *2022 IEEE International Symposium on Workload Characterization (IISWC)*, Austin, TX, USA, 2022, pp. 146-159, doi: 10.1109/IISWC55918.2022.00022.
- B. Aslan and **A. Yilmazer-Metin**, "A Study on Power and Energy Measurement of NVIDIA Jetson Embedded GPUs Using Built-in Sensor," *2022 7th International Conference on Computer Science and Engineering (UBMK)*, Diyarbakir, Turkey, 2022, pp. 1-6, doi: 10.1109/UBMK55850.2022.9919522.
- R. O. Yıldız and **A. Yılmazer-Metin**, "Design and Implementation of TLS Accelerator," *2022 IEEE 15th Dallas Circuit And System Conference (DCAS)*, Dallas, TX, USA, 2022, pp. 1-4, doi: 10.1109/DCAS53974.2022.9845527.
- R. O. Yıldız and **A. Yilmazer-Metin**, "Implementation of Dynamically Configurable Modulator on FPGA," *2021 29th Telecommunications Forum (TELFOR)*, 2021, pp. 1-4.
- R. O. Yıldız and **A. Yilmazer-Metin**, "CORDIC Accelerator for RISC-V," *2021 29th Telecommunications Forum (TELFOR)*, 2021, pp. 1-4.
- Beyazit Bestami Yuksel, Serif Bahtiyar, and **Ayse Yilmazer**. 2020. Credit Card Fraud Detection with NCA Dimensionality Reduction. In 13th International Conference on Security of Information and Networks (SIN 2020). Association for Computing Machinery, New York, NY, USA, Article 18, 1–7.
- Furkan Kurt, Deniz Turgay Altilar, **Ayse Yilmazer Metin**, Implementations of the Needleman-Wunsch Algorithm for GPU Architectures, 7. Ulusal Yüksek Başarımlı Hesaplama Konferansı (BASARIM), Istanbul, 11-13 Mayis, 2022.
- **Ayse Yilmazer-Metin**, sRSP: GPUlarda Asimetrik Senkronizasyon İçin Yeni Ölçeklenebilir Bir Çözüm, 6. Ulusal Yüksek Başarımlı Hesaplama Konferansı (BASARIM), Ankara, 8-9 Ekim, 2020.
- M. S. Orr, S. Che, **A. Yilmazer**, B. M. Beckmann, M. D. Hill, D. A. Wood; "Synchronization Using Remote-Scope Promotion", *In Proceedings of the Twentieth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '15).* Association for Computing Machinery, New York, NY, USA, 73–86.
- **Ayse Yilmazer**, Zhongliang Chen, and David Kaeli, "Scalar Waving: Improving the Efficiency of SIMD Execution on GPUs," *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, May 2014.
- **Ayse Yilmazer** and David Kaeli, "HQL: A Scalable Synchronization Mechanism for GPUs", *International Parallel and Distributed Processing Symposium (IPDPS)*, May 2013.
- Fatemeh Azmandian, **Ayse Yilmazer**, Jennifer Dy, Javed Aslam, and David Kaeli, "GPU-Accelerated Feature Selection for Outlier Detection using the Local Kernel Density Ratio", *IEEE International Conference on Data Mining (ICDM)*, December 2012. https://ieeexplore.ieee.org/document/6413785
- James Goodman, David Kaeli, Dana Schaa, **Ayse Yilmazer**, "Accelerating a Hyperspectral Inversion Model for Submerged Marine Ecosystems using High-

WORKSHOP PAPERS

- **Ayse Yilmazer**, Resit Sendag, and Joshua J. Yi, "Quantifying and Comparing the Impact of Wrong-Path Memory References in Multiple-CMP Systems," (*CMP-MSI): Workshop on Chip Multiprocessor Memory Systems and Interconnects,* in conjunction with the 13th Annual International Conference on High-Performance Architecture (HPCA-13), February 2007.
- **Ayse Yilmazer**, Resit Sendag, Joshua J. Yi, and Augustus K. Uht, "Investigating the Effects of Wrong-Path Memory References in Shared-Memory Multiprocessor Systems", *Boston Area Architecture Workshop (BARC)*, February 2006.

PROFESSIONAL ACTIVITIES

- Program committee for HPCA 2023.
- Program committee for Computing Frontiers (CF) 2018, 2019, 2020, 2021.
- Program committee for SBAC-PAD 2021, 2022, 2024
- Program committee for ICCD 2020.
- Program committee for Workshop on General Purpose Computing using GPUs (GPGPU 2018)
- Organizing committee for 5th National High Performance Computing Conference (BASARIM-2017).
- Program committee for 4th National High Performance Computing Conference (BASARIM-2015), 5th National High Performance Computing Conference (BASARIM-2017), and Workshop about General Purpose Computing using GPUs (GPGPU-10), 2017.
- Reviewer for IEEE Transactions on Parallel and Distributed Systems, Journal of Parallel and Distributed Computing, Concurrency and Computation: Practice and Experience.

EMPLOYMENT HISTORY

Computer Engineering Department, Istanbul Technical University, Istanbul, Turkey Jan. 2018 –

- Currently doing research in various areas including accelerator and domain specific processor design targeting sparse operations and FHE, compiler optimizations targeting ML applications and FHE, accelerated computing, memory consistency and synchronization, GPU microarchitecture and performance analysis.
- Teaching Computer Architecture, Microprocessor Systems classes at the undergraduate level and teaching GPU Computing Using CUDA, Enhanced Processor Architecture, Parallel Algorithms classes at the graduate level.
-

Computer Engineering Department, Altinbas (Istanbul Kemerburgaz) University, Istanbul, Turkey Feb. 2015 – Dec. 2017

Assistant Professor in Computer Engineering Department and Information Technologies Department Chair in Graduate School of Science and Engineering

- Taught classes at the graduate and undergraduate level including classes: Advanced Computer Architecture, Computer Architecture, Parallel and distributed Computing, Algorithm Analysis, Computer Organization, Microprocessors, and Programming with C which was taken by all first year engineering students (undergrad level).
- Served as a chair for Information Technologies Department in Graduate School of Science and Engineering

Advanced Micro Devices (AMD), Bellevue, WA Feb. 2014 – Feb. 2015

Senior Design Engineer

- Worked on research ideas towards Exascale computing. My research was focused on synchronization and memory consistency on HSA enabled GPUs to improve the support for task parallelism.

ECE Department, Northeastern University, Boston, MA Sept. 2007 – Dec. 2013

Research/Teaching Assistant

- Worked as a teaching assistant for courses including High Level Design of Hw-Sw, Computer Architecture, and Digital Design.
- Worked on a visualization tool utilizing GPU computing which is used for proton therapy research at Massachusetts General Hospital, Boston.
- Conducted research on synchronization and improving efficiency of SIMD Execution on GPUs. Developed a hardware based blocking synchronization mechanism for mutual exclusion, including definition of new primitives, queuing at caches, synchronization protocol for queuing and implementation in simulator for evaluation and analysis. Also, worked on micro-architectural techniques for improving SIMD efficiency on GPUs exploiting scalar operations.
- Performed research on profiling and the accurate attribution of performance data on virtualized environments using hardware performance counters.
- Worked on acceleration of a Hyperspectral Inversion Model for Submerged Marine Ecosystems using High-Performance Computing on GPUs.

Intel Inc., Hillsboro, OR Apr. 2011 – Aug 2011

Graduate Intern

- Worked with Binary Translation and Performance team. Used binary analysis techniques and simulation to study the memory access patterns and performance characteristics of pointer intensive benchmarks.

Advanced Micro Devices, Marlborough, MA July 2008 – Dec. 2008

Intern

- Done performance analysis and characterization for if-flattening in ATI's compiler suite and implemented an optimization for break elimination to have the compiler to perform further optimization for performance.

Cavium Networks, Marlborough, MA Feb 2007 – May 2007

Hardware Verification Engineer

- Developed a test bench for one of the unit under design using Testbuilder and performed daily and regression tests.

Freescale Semiconductor, Austin, TX June 2006 – Dec. 2006

Intern

- Made modification on Memory mapped I/O terminal emulator software to adjust internal data structures to run with 32 bit and 64 bit addressing modes. Updated test cases to include tests for modifications and regression. Code implemented with C++, using Eclipse IDE on Linux.
- Developed a functional cache simulator modeling various replacement/allocation policies implemented by different PowerPC architectures. Code implemented with C++, using Eclipse IDE on Linux.

ECE Department, University of Rhode Island, Kingston, RI Sept. 2004 – May 2006

Research/Teaching Assistant

- Worked as a teaching assistant for various computer engineering classes, including Introduction to computing Systems, Microprocessors Lab, Computer Communications, Introduction to Computer Architecture.
- Worked on ideas to quantify and reduce effects of wrong-path memory references on Shared-memory Multiprocessor systems as a research assistant.

Defense Technologies and Engineering (STM) Inc., Ankara Aug. 2001 – Sept. 2004
Software Engineer

- Took part in software development for a tactical strategic planning system. Worked on software requirements specification, analysis and design using UML. Implemented code with Java. Gained experience with design patterns.
- Implemented code for MPS (Mission Planning System) component of Mission Support System, using Visual C++, MFC, and Visual Basic.
- Developed user interface for a prototype system, used Borland C++ Builder.
- Evaluated Rational RoseRT and Tornado II as an integrated environment.

Air Defense Electronics Systems (HAVELSAN AS.) Inc., Ankara Feb. 2000 – Aug. 2001
Software Engineer

- Worked with a software development team at Thomson Marconi Sonar Ltd in England. Worked on software preliminary design of the Mine Hunting Sonar System. Used Rational Rose.
- Worked on software requirements specification, analysis and design for a computer aided training application for the Turkish Navy Sonar operators. Used UML with Rational Rose and Rational RequisitePro.

Microwave Electronic Systems (MIKES) Inc., Ankara June 1999 – Jan. 2000
Software Engineer

- Worked on the operational flight program code of ALQ 178 V.3 System. Inspected code, worked on algorithms, and fixed bugs on software.
- Took part in software engineering group to define the software development process that compatible with CMM Level 3. Prepared procedures manual for software configuration management.

Defense Technologies and Engineering (STM) Inc., Ankara Aug. 1997 – June 1999
Software Engineer

- Participated in software maintenance of Turkish Mobile Radar Complex Project (TMRC-C3), which was a real time, embedded system, developed with ADA 83. Fixed bugs in Surveillance component. Implemented code for corrective actions, tested results on target environment, and run regression tests. Experienced cross development using ADA 83 on Sun Solaris as the development environment and VxWorks as the target environment.

REFERENCES Available upon request.