Macromodels

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Outline

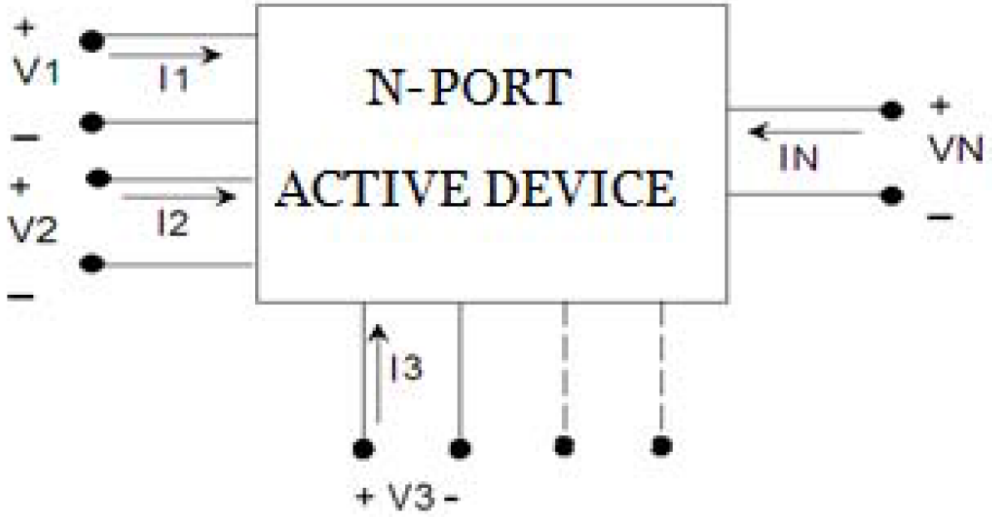
- Macromodel concept
- Macromodels for Operational Amplifiers
- Macromodels for other type active elements
  - Operational Transconductance Amplifiers
  - Macromodels for Current Conveyors
  - Macromodels for FTFN

Macromodels, Concept

- Nonlinear equivalent circuits of a device consisting of reduced number of diodes and transistors, linear circuit elements such as dependent and independent current and voltage sources, resistors, capacitors and inductors.

- The aim of macromodeling is to obtain a circuit model of an IC or a portion of an IC with reduced complexity providing less costly simulation time, or to permit the simulation of larger IC’S or IC systems without convergence problem.

Macromodels, Concept



Nonlinear N-port Active Device

- The current-voltage relations of the active device is given as

$$\begin{pmatrix} I_1 \\ I_2 \\ . \\ I_N \end{pmatrix} = \begin{pmatrix} f_1(V_1, V_2, \ldots, V_N) \\ f_2(V_1, V_2, \ldots, V_N) \\ . \\ f_N(V_1, V_2, \ldots, V_N) \end{pmatrix}$$

The general model of a nonlinear device must represent with sufficient accuracy the variations of the device characteristics with the terminal currents and voltages for every operating region.

Macromodels, Concept

- Because of the large number of active devices in large-scale IC systems, the analysis can surpass simulator circuit-size capability, or cause numerical problems.

- Even if an adequate simulator and computer are available, the required simulation time makes the analysis impractical.

- Convergence problem.

Macromodels, Concept

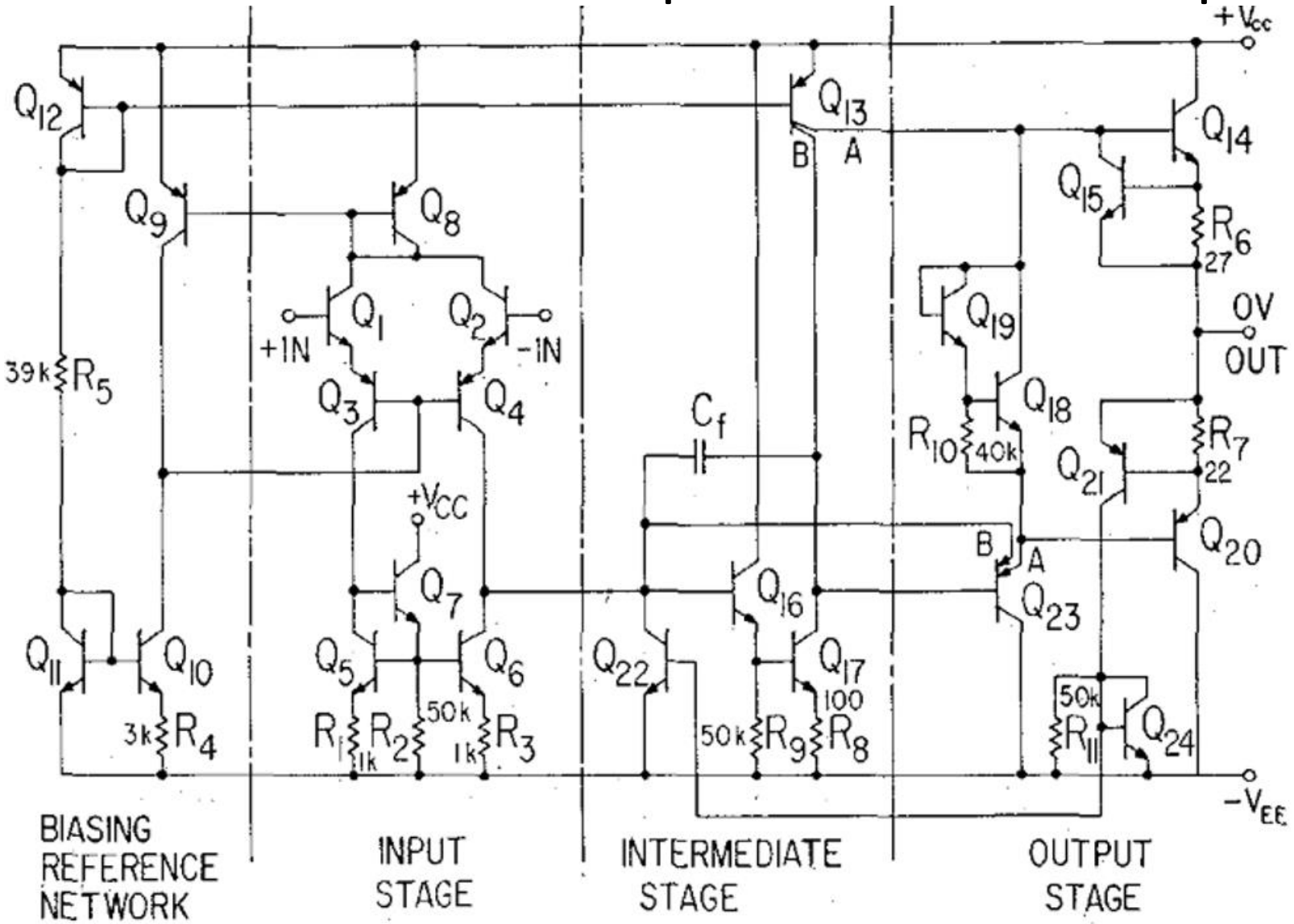
- One solution to this problem:
- macromodels
- A good macromodel fulfills two contradictory requirements:
- As simple as possible
- Simulate circuits with maximum possible accuracy

Macromodels, Concept

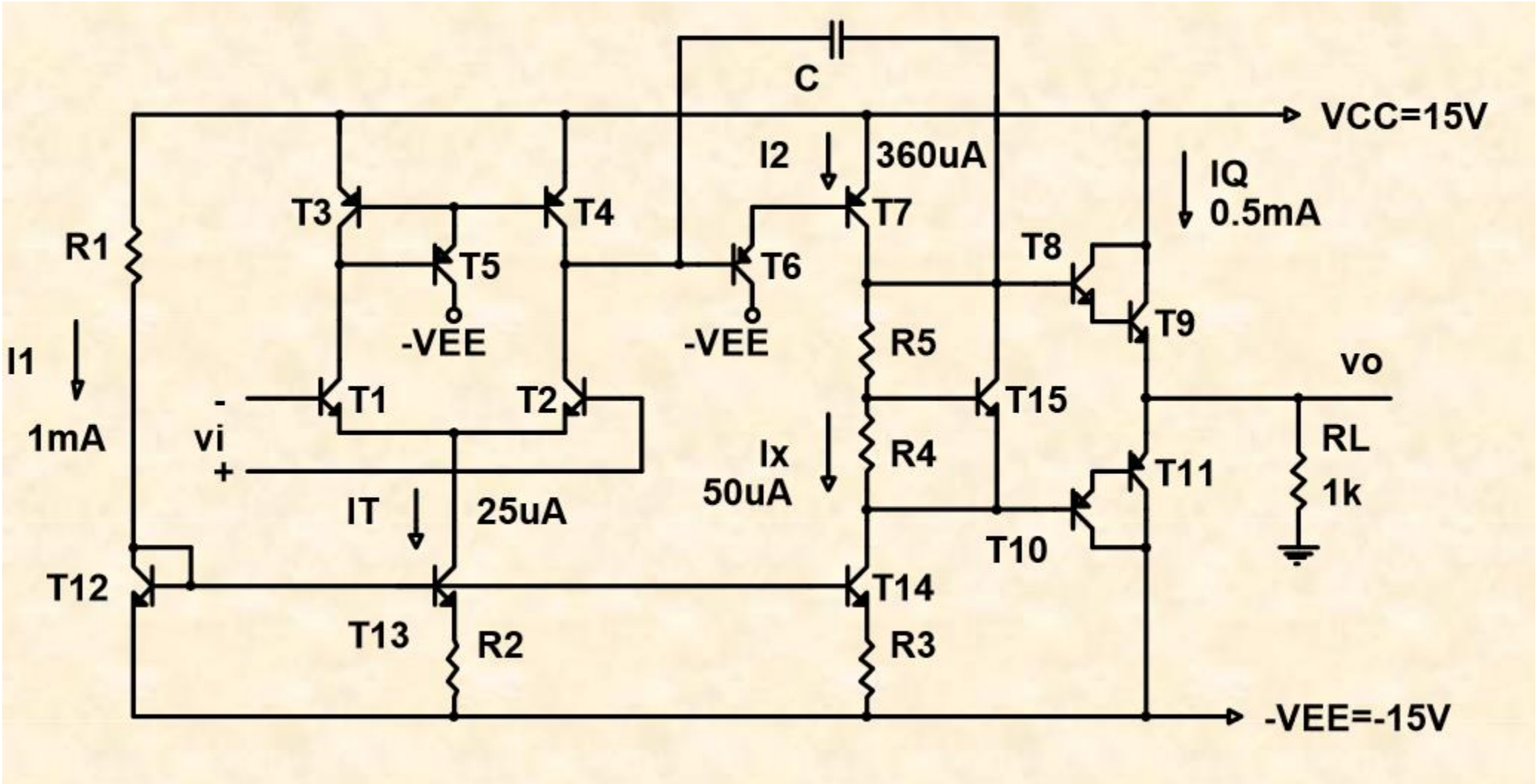
- Resorting to macromodels instead of device level models is a widely used strategy
- Reducing high computation time required when simulating complex systems with device models.

Macromodels for Operational Amplifiers

Macromodels for Operational Amplifiers



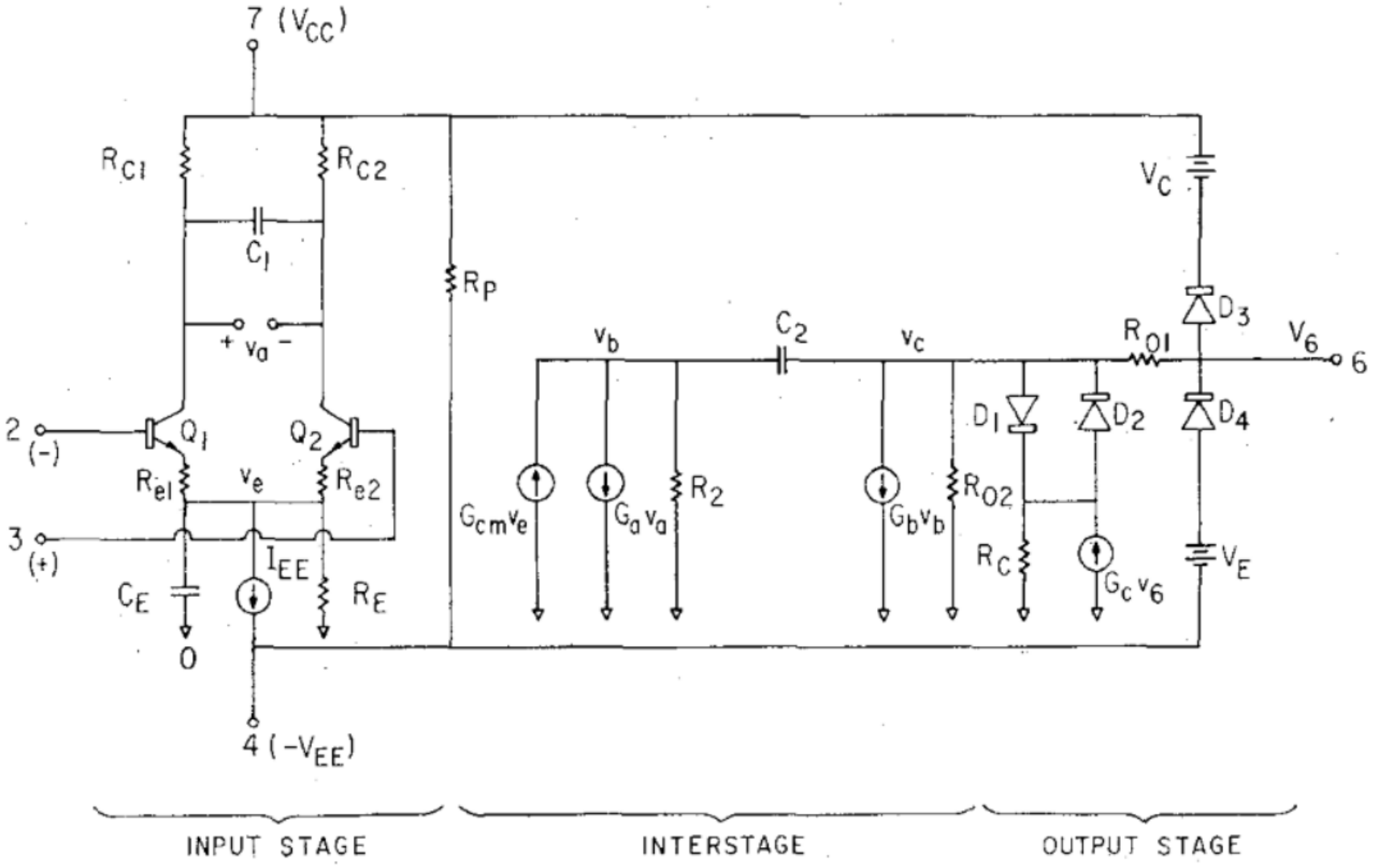
Macromodels for Operational Amplifiers



Macromodels for Operational Amplifiers

Boyle Macromodel

Macromodels for Operational Amplifiers



Macromodels for Operational Amplifiers

The circuit of Fig. 1 is subdivided into three stages.

The input stage consists of ideal transistors Q1 and Q2 and the associated sources and passive elements,

This stage produces the necessary linear and nonlinear differential-mode (DM) and common-mode (CM) input characteristics.

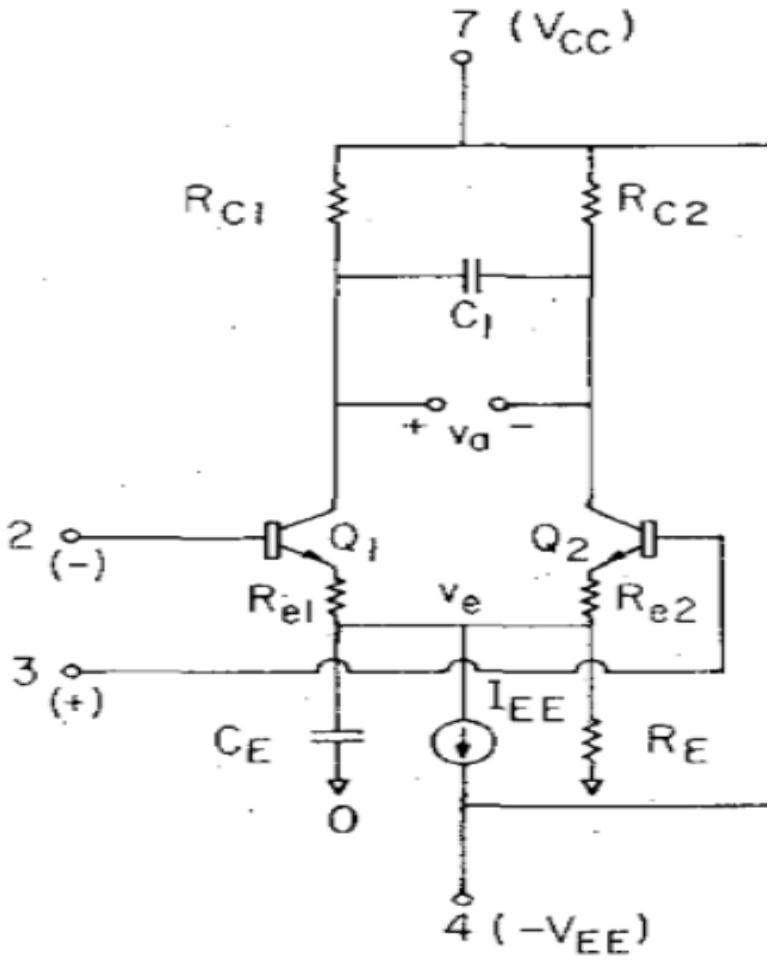
Macromodels for Operational Amplifiers

For convenience, the stage is designed for unity voltage gain.

The stage can be designed to provide desired voltage and current offsets.

the capacitor CE is used to introduce a second-order effect for the slew rate [4],

the capacitor C1 introduces a second-order effect to the phase response.



Macromodels for Operational Amplifiers

- The DM and CM voltage gains of the op amp are provided by the linear interstage and output stage elements consisting of Gm, Ga, R2, Gb, and Ro2.

- The dominant time constant of the op amp is produced with the internal feedback capacitor C2

Macromodels for Operational Amplifiers

- The output stage provides the proper dc and ac output resistance of the op amp.
- The elements D1, D2, Rc, and GC produce the desired maximum short-circuit current.
- The elements D3, Vc and D4 VE are voltage-clamp circuits to produce the desired maximum voltage swing.

Macromodels for Operational Amplifiers

- The circuit model has been developed using two basic macromodeling techniques:

- simplification and build-up.

- In the simplification technique, representative portions of op amp circuitry are successively simplified by using simple ideal elements to replace numerous real elements.

Macromodels for Operational Amplifiers

- In the build-up technique, a circuit configuration composed of ideal elements is proposed to meet certain external circuit specifications without necessarily resembling a portion of an actual op amp circuit configuration.
- The build-up technique is employed in the development of the output stage.

Macromodels for Operational Amplifiers

Design Equations for the Op AMP Maromodel

$$V_T = \frac{kT}{q} = 25.85 \text{ mV for } 300 \text{ K}$$

$$I_{S1} = I_{SD3} = I_{SD4} = 8 \cdot 10^{-16} \text{ A}$$

$$R_2 = 100 \text{ k}\Omega$$

$$I_{C1} = I_{C2} = \frac{C_2}{2} S_R^+$$

$$C_E = \frac{2I_{C1}}{S_R^-} - C_2$$

$$I_{B1} = I_B + \frac{I_{Bos}}{2}$$

$$I_{B2} = I_B - \frac{I_{Bos}}{2}$$

$$\beta_1 = I_{C1}/I_{B1}$$

$$\beta_2 = I_{C2}/I_{B2}$$

$$I_{EE} = \left(\frac{\beta_1 + 1}{\beta_1} + \frac{\beta_2 + 1}{\beta_2}\right) I_{C1}$$

$$R_E = 200/I_{EE}$$

$$R_{e1} = \left(\frac{\beta_1 + \beta_2}{\beta_1 + \beta_2 + 2}\right)\left(R_{C1} - \frac{1}{g_{m1}}\right)$$

$$C_1 = \frac{C_2}{2} \tan \Delta\phi$$

$$R_p = (V_{CC} + V_{EE})^2/(P_d - V_{CC}(2I_{C1}) - V_{EE}I_{EE})$$

$$G_a = 1/R_{c1}$$

$$G_{cm} = \frac{1}{R_{c1}\,(\text{CMRR})}$$

$$R_{01} = R_{0-ac}$$

$$R_{02} = R_{out} - R_{01}$$

$$G_b = \frac{a_{VD}R_{c1}}{R_2R_{02}}$$

$$I_X = (2I_{C1})G_bR_2 - I_{SC}$$

$$I_{SD1} = I_{SD2} = I_X \exp - \frac{R_{01}I_{SC}}{V_T}$$

$$R_C = \frac{V_T}{100I_X} \ln \frac{I_X}{I_{SD1}}$$

Macromodels for Operational Amplifiers

$$I_{S2} = I_{S1}\left(1 + \frac{V_{os}}{V_T}\right)$$

$$\frac{1}{g_{m1}} = V_T/I_{C1}$$

$$R_{c1} = 1/2\pi f_{0\ dB} C_2$$

$$G_C = 1/R_C$$

$$V_C = V_{CC} - V_{out}^{+} + V_T \ln \frac{I_{SC}^{+}}{I_{SD3}}$$

$$V_E = V_{CC} + V_{out}^{-} + V_T \ln \frac{I_{SC}^{-}}{I_{SD4}}$$

Macromodels for Operational Amplifiers

The Input Stage: Ic1 and CE

The value of the necessary collector current of the first stage is established by the slew rate of the op amp. If the op amp is connected as a voltage follower, the positive going slew rate SR+ is

$$S_R{}^+ = \frac{2I_{C1}}{C_2} \qquad I_{C1} = \tfrac{1}{2}C_2 S_R{}^+ \qquad I_{C2} = I_{C1}$$

Macromodels for Operational Amplifiers

The negative going slew rate SE- is smaller

$$S_R^- = \frac{2I_{C1}}{C_2 + C_E} \qquad C_E = \frac{2I_{C1}}{S_R^-} - C_2$$

Macromodels for Operational Amplifiers

The Transistor Parameters, offset voltage and current

$$I_{B1} = I_B + \frac{I_{Bos}}{2}, \qquad I_{B2} = I_B - \frac{I_{Bos}}{2}$$

$$\beta_1 = \frac{I_{C1}}{I_{B1}}, \qquad \beta_2 = \frac{I_{C2}}{I_{B2}}.$$

Macromodels for Operational Amplifiers

The Transistor Parameters, offset voltage and current

$$V_{os} = V_{BE1} - V_{BE2}$$

$$= V_T \ln \frac{I_{S1}}{I_{S2}}.$$

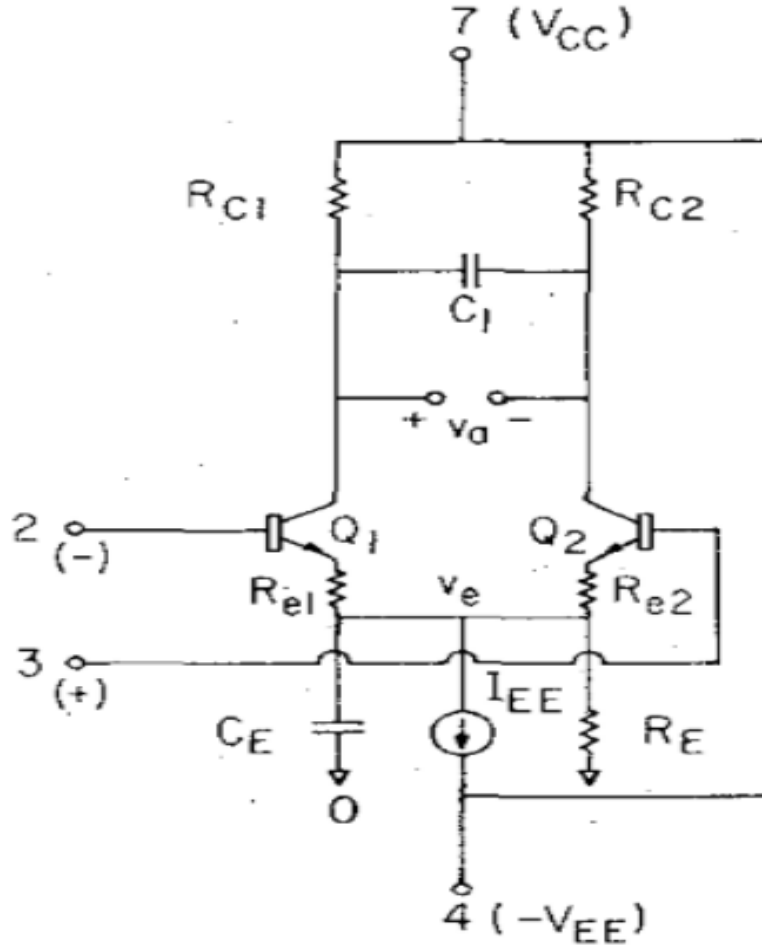
$$I_{S2} = I_{S1} \exp \frac{V_{os}}{V_T} \cong I_{S1}\left[1 + \frac{V_{os}}{V_T}\right]$$

Macromodels for Operational Amplifiers

The Input Stage: Rc1 and Re1
The corner frequency can be estimated using a Miller effect approximation in the interior stage.

$$f_{3\ \mathrm{dB}} \simeq \frac{1}{2\pi R_2 C_2 (1 + G_b R_{02})}$$

$$\simeq \frac{1}{2\pi R_2 C_2 G_b R_{02}}.$$



Macromodels for Operational Amplifiers

The DM voltage gain at very low frequencies

$$a_{VD} = (G_a R_2)(G_b R_{02})$$

Ga is chosen to be equal to l/Rc1

$$f_{0\ \mathrm{dB}} = \frac{1}{2\pi R_{c1} C_2}$$

$$R_{c1} = \frac{1}{2\pi f_{0\ \mathrm{dB}} C_2}$$

Macromodels for Operational Amplifiers

Re1 is found from the DM voltage gain of the first stage,

$$\frac{v_a}{v_{\text{in}}} = \frac{\beta_1 R_{c1} + \beta_2 R_{c2}}{\dfrac{\beta_1}{g_{m1}} + (\beta_1 + 1)R_{e1} + \dfrac{\beta_2}{g_{m2}} + (\beta_2 + 1)R_{e2}} = 1.$$

If $I_{C1} = I_{C2}$, then $g_{m1} = g_{m2}$. If also $R_{c1} = R_{c2}$ and $R_{e1} = R_{e2}$,

Macromodels for Operational Amplifiers

Re1 is found from the DM voltage gain of the first stage,

$$R_{e1} = \frac{\beta_1 + \beta_2}{\beta_1 + \beta_2 + 2}\left[R_{c1} - \frac{1}{g_{m1}}\right]$$

Macromodels for Operational Amplifiers

The resistor RE is added to provide a finite CM input resistance.

Macromodels for Operational Amplifiers

To introduce excess phase effects in the DM amplifier response, another capacitor Cl is added in the input stage. The second pole of the DM gain function is located at

$$p_2 = -1/2R_{c1}C_1$$

$$\phi_m = 90^\circ - \Delta\phi \qquad C_1 = \frac{C_2}{2}\tan\Delta\phi$$

Macromodels for Operational Amplifiers

To model the actual dc power dissipation of an op amp, a resistor RP is introduced into the macromodel.

$$P_d = V_{CC}2I_{C1} + V_{EE}I_{EE} + \frac{(V_{CC} + V_{EE})^2}{R_p}$$

$$R_p = \frac{(V_{CC} + V_{EE})}{P_d - V_{CC}2I_{C1} - V_{EE}I_{EE}}.$$

Macromodels for Operational Amplifiers

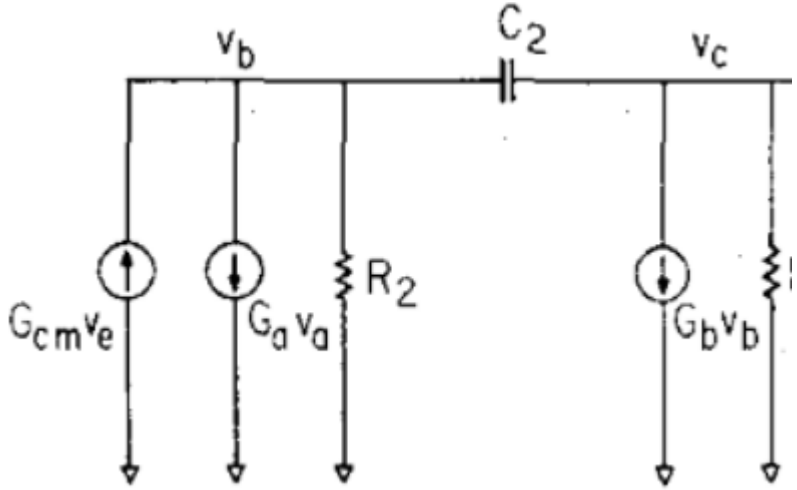
The Interstage: Ga, R2, and GCM

CM voltage gain from the input to Vb is

$$\frac{v_{b\mathrm{CM}}}{v_{\mathrm{inCM}}} \cong G_{cm}R_2$$

DM voltage gain from the input to Vb is

$$\frac{v_{b\mathrm{DM}}}{v_{\mathrm{inDM}}} = G_aR_2 = \frac{1}{R_{c1}}R_2$$



Macromodels for Operational Amplifiers

$$\mathrm{CMRR} = \frac{a_{VD}}{a_{VC}} = \frac{1}{R_{c1} G_{cm}}.$$

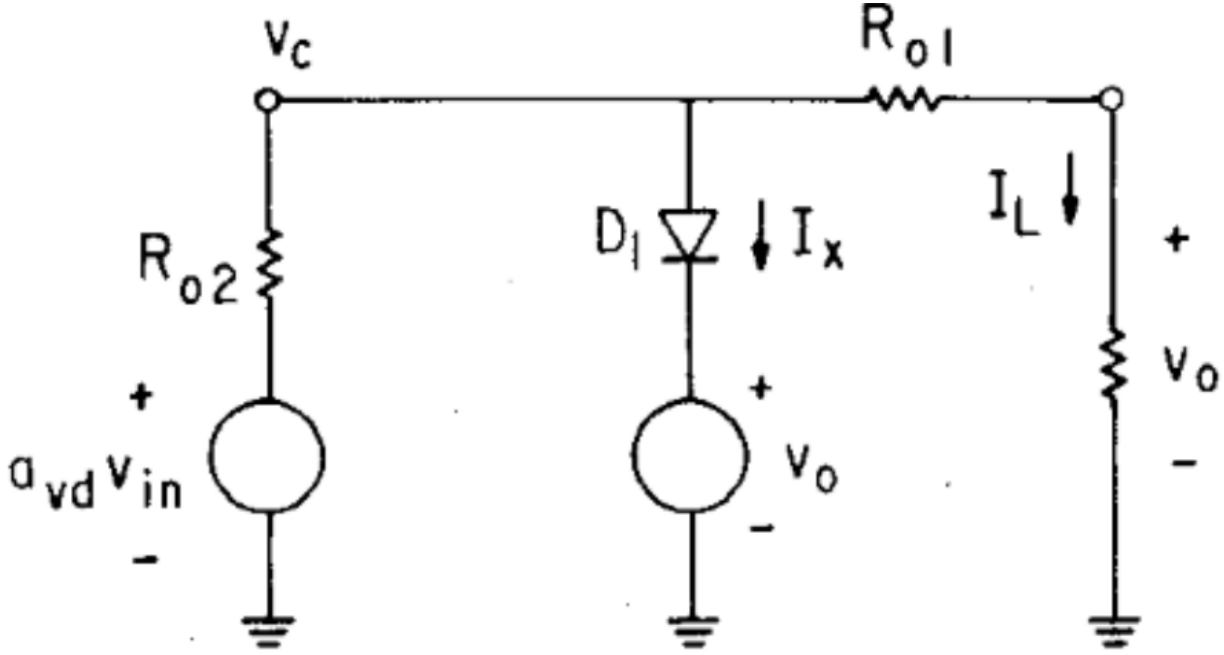
$$G_{cm} = \frac{1}{(\mathrm{CMRR}) R_{c1}}.$$

Macromodels for Operational Amplifiers

The Output Stage: Ro1, Ro2 and Gb

$$R_{out} = R_{01} + R_{02}$$

$$R_{01} = R_{0-ac}$$



Macromodels for Operational Amplifiers

The Output Stage: Ro1, Ro2 and Gb

$$R_{02} = R_{\text{out}} - R_{01}$$

$$G_b = \frac{a_{VD} R_{c1}}{R_2 R_{02}}$$

Macromodels for Operational Amplifiers

The Output Stage: Current Limiting ISC

$$I_{SC} \simeq \frac{V_D}{R_{01}}$$

Ix Maximum current through D1 or D2
Is, Saturation current of diodes D1, D2

Since Ro1 is known, ISD1 can be established once Ix is determined

$$V_D = V_T \ln \frac{I_X}{I_{SD1}}$$

$$I_X = I_{SD1} \exp \frac{I_{SC} R_{01}}{V_T}$$

Macromodels for Operational Amplifiers

The Output Stage: Voltage Limiting

The output voltage excursion is limited by the voltage source-diode clamp combinations Vc D3 and VE, D4, With a large, positive output voltage such as to forward bias D3

$$V_{\text{out}}^{+} = V_{CC} - V_C + V_{D3}$$

$$= V_{CC} - V_C + V_T \ln \frac{I_{SC}^{+}}{I_{SD3}}$$

Macromodels for Operational Amplifiers

The Output Stage: Voltage Limiting

$$V_C = V_{CC} - V_{\text{out}}^{+} + V_T \ln \frac{I_{SC}^{+}}{I_{SD3}}$$

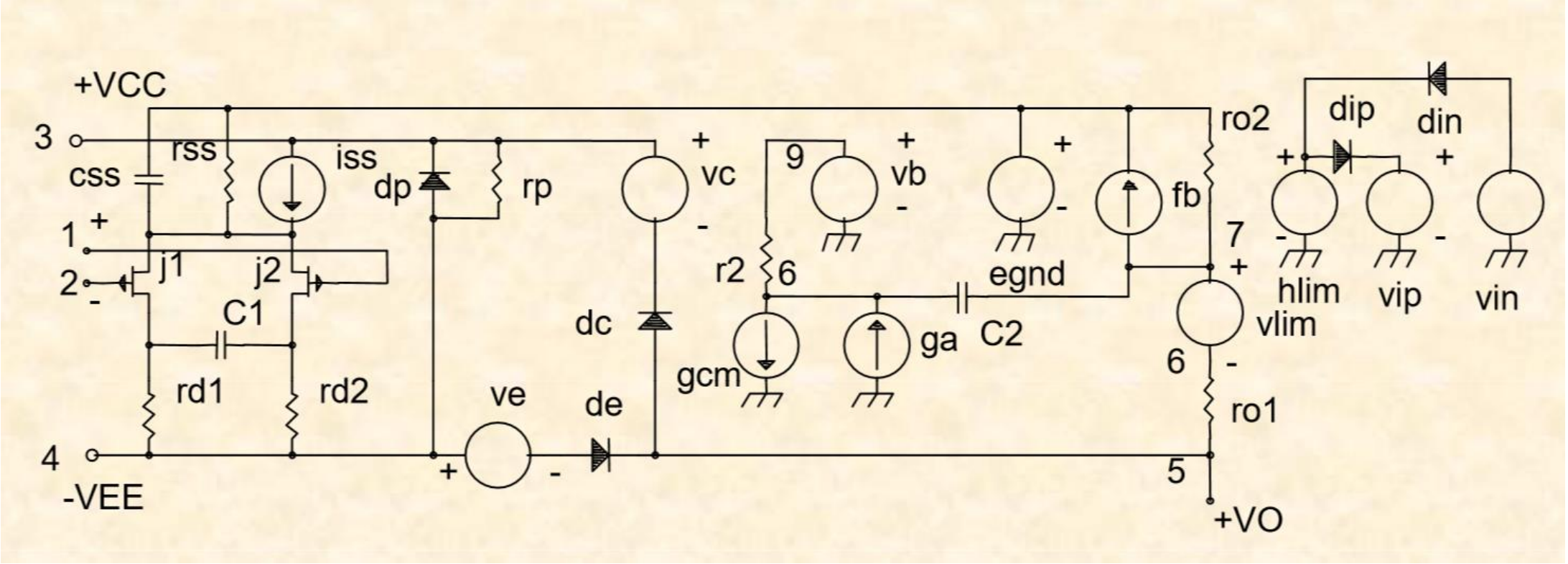
Similarly for negative voltage region

$$V_E = V_{EE} + V_{\text{out}}^{-} + V_T \ln \frac{I_{SC}^{-}}{I_{SD4}}$$

Macromodels for Operational Amplifiers

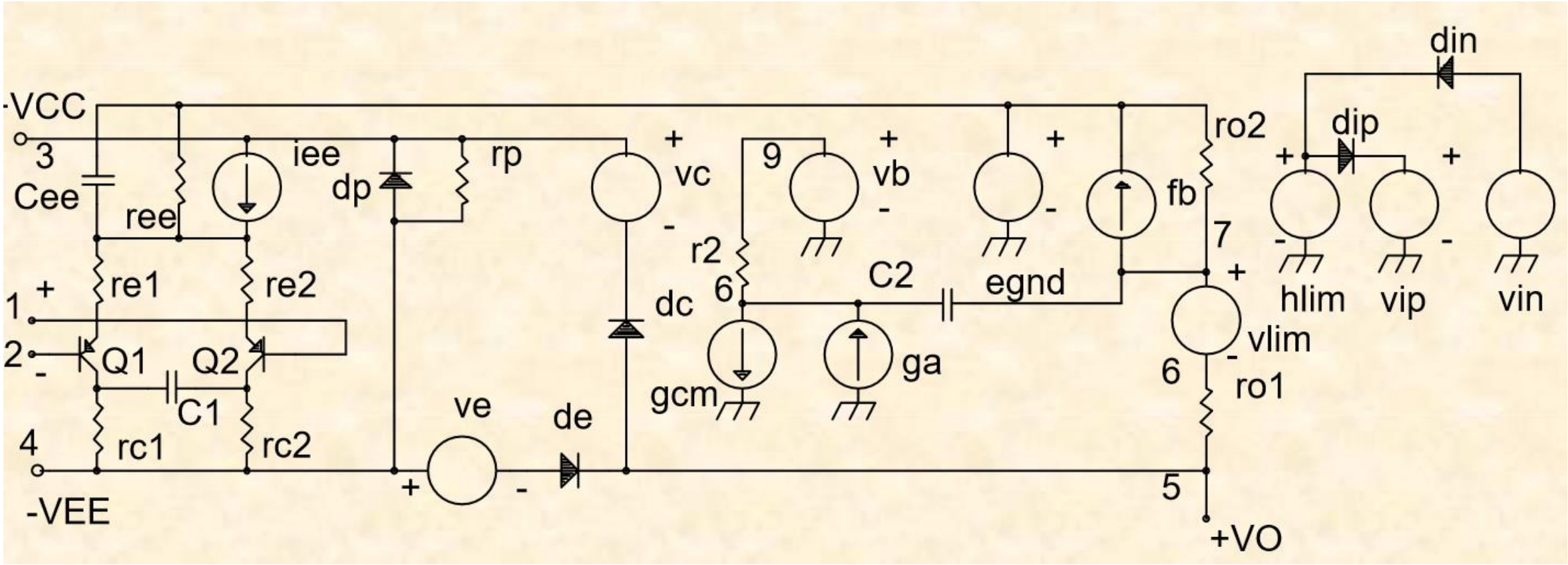
Boyle Macromodels for other type input elements

JFET input, SPICE library



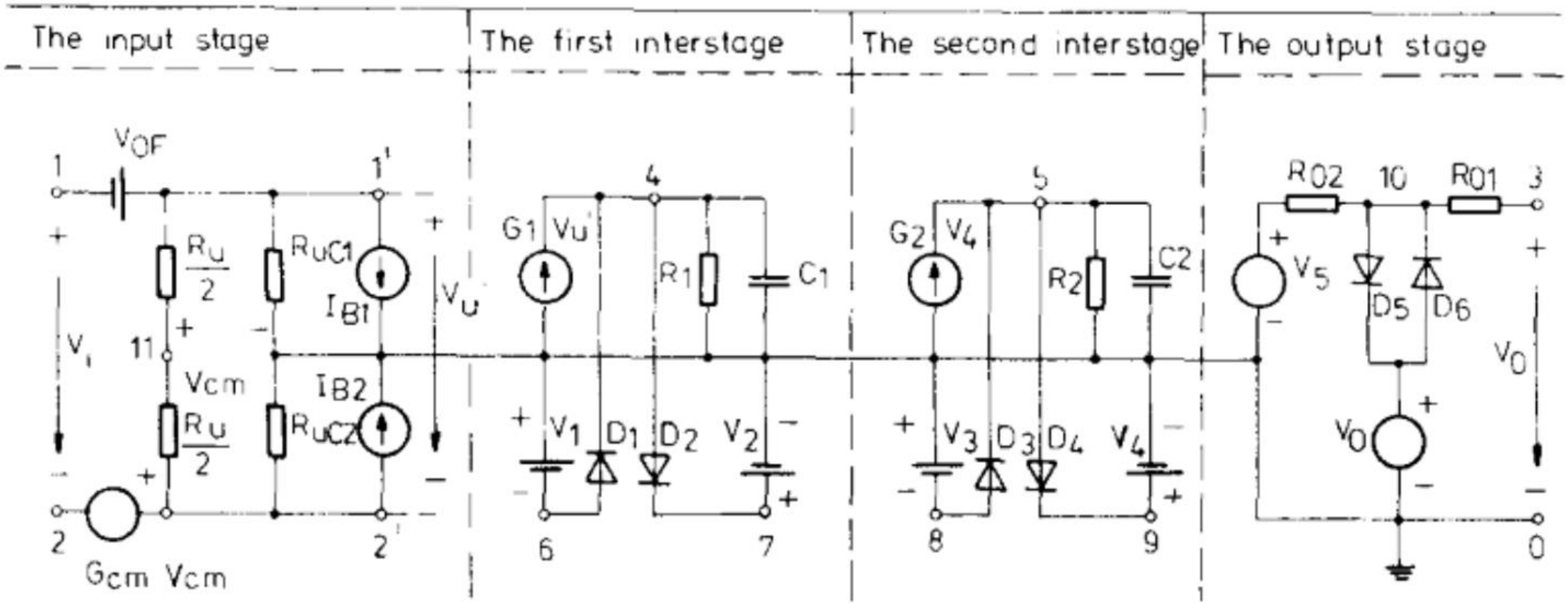
Macromodels for Operational Amplifiers

Boyle Macromodels for other type input elements
pnp input, SPICE library



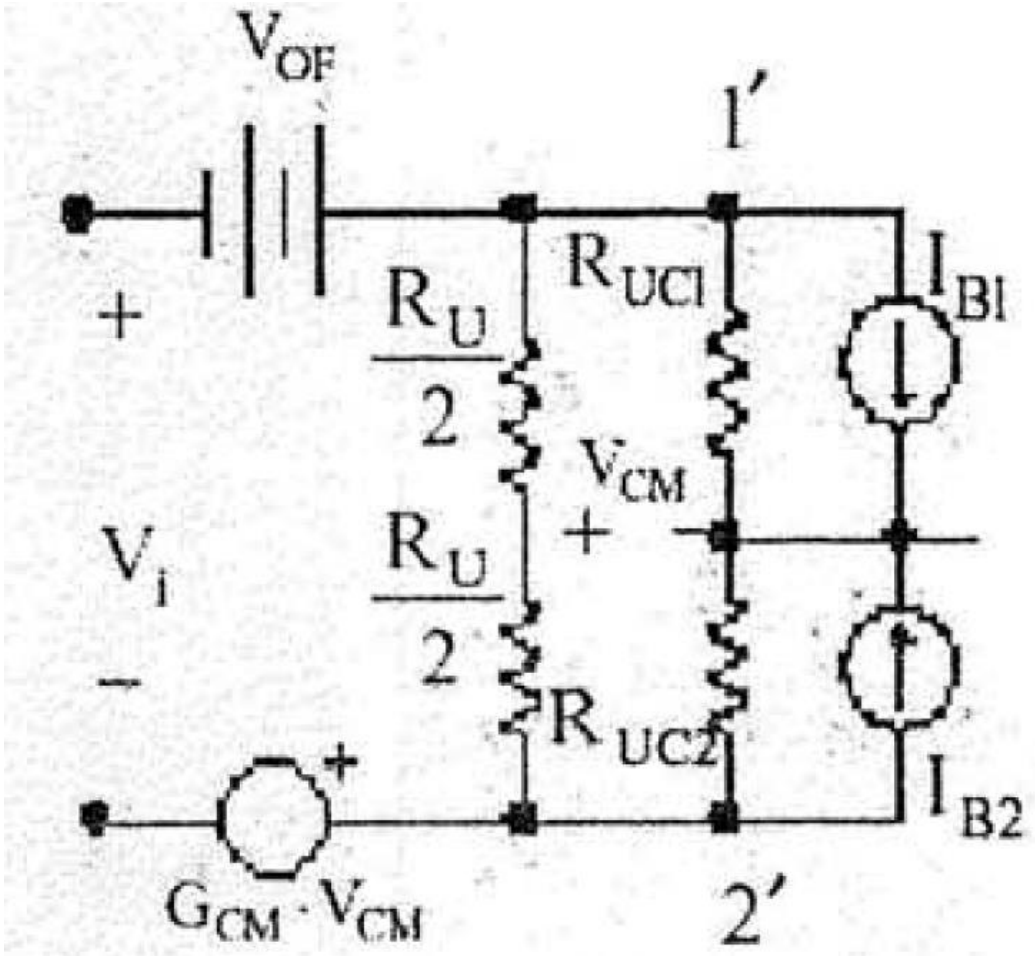
PEIC Macromodel

Macromodels for Operational Amplifiers



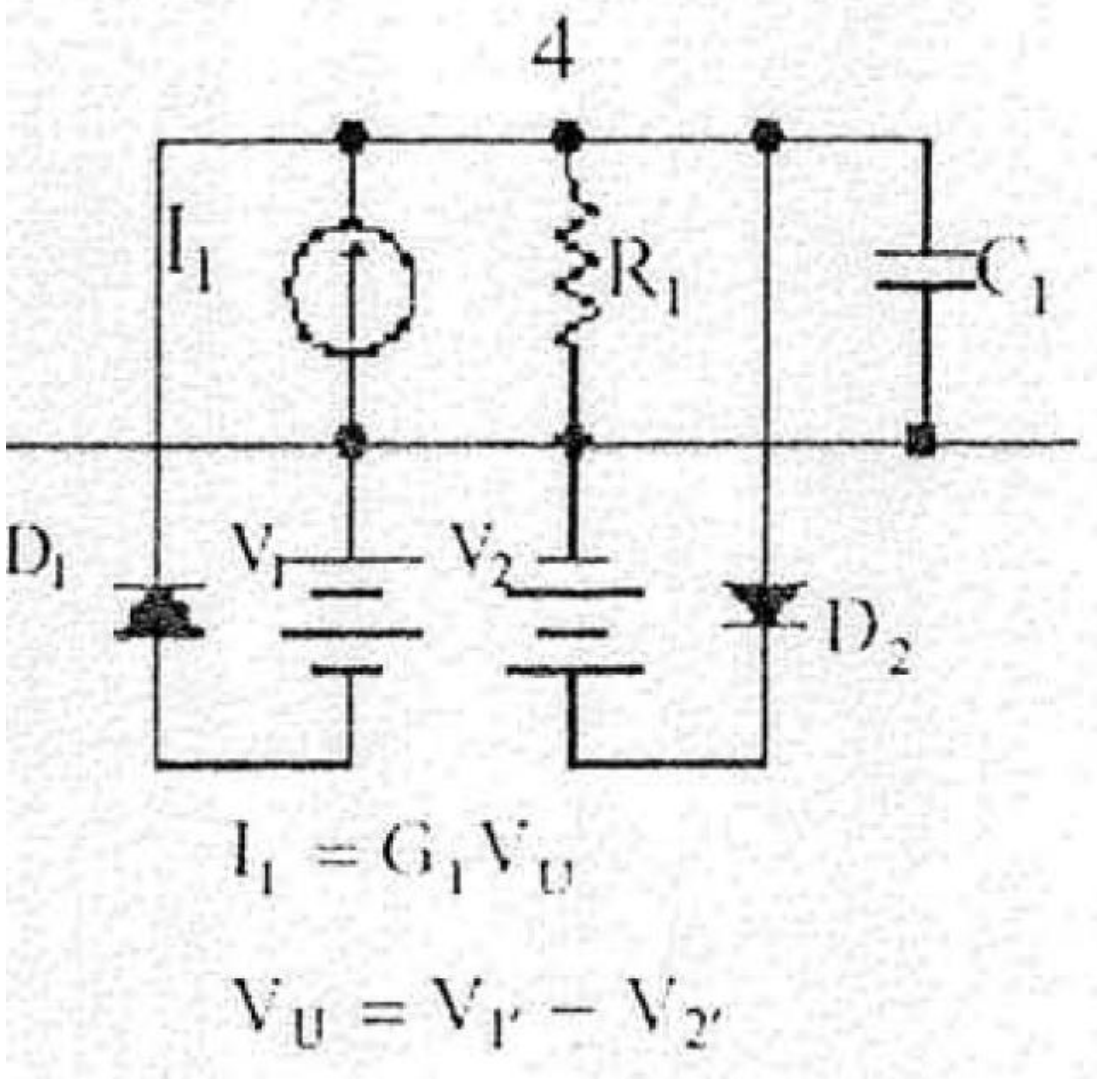
Macromodels for Operational Amplifiers

The input stage can simulate the bias current IB1, the difference-mode and the common-mode input resistances RI, RICMl, RiCM2, the offset voltage VOF and current IOF, and finally the common-mode voltage gain.



Macromodels for Operational Amplifiers

The first interstage simulates two slew rates using two diodes limiters V1-D1, and V2-D2, that define the maximum and minimum voltages at node 4



Macromodels for Operational Amplifiers

the two extreme quantities of voltage-dependent current sources G2*V4, that generate rising and falling voltages on the capacitor C2, or generate two slew rates + SR and – SR.

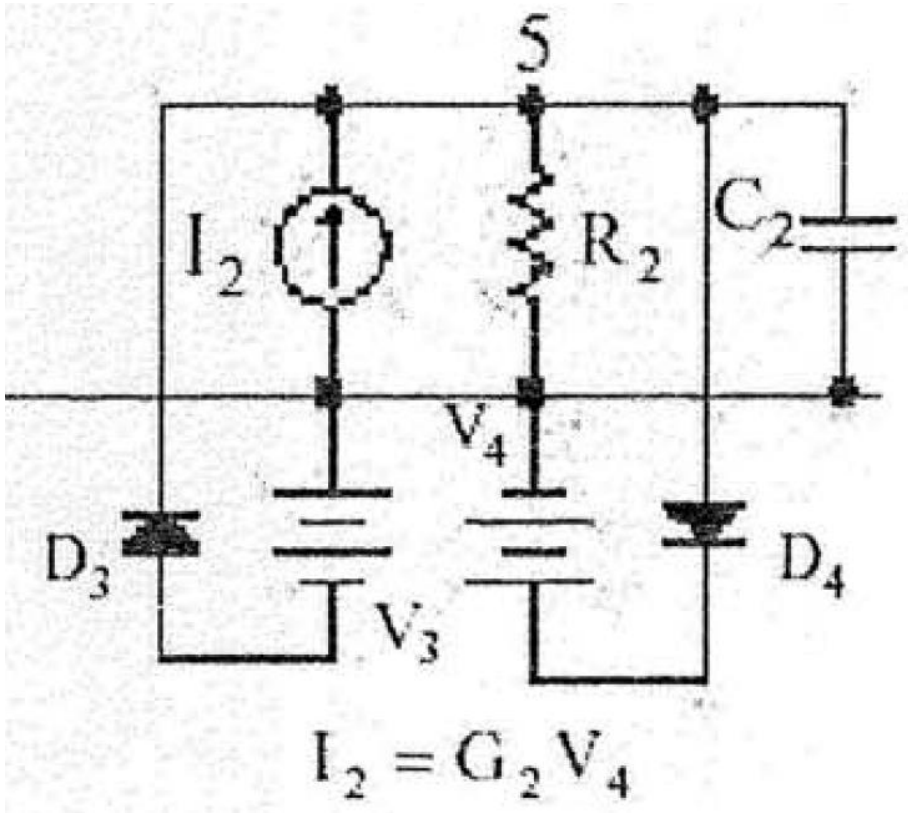
Macromodels for Operational Amplifiers

the first interstage produces the second pole f2 using the capacitor C, in parallel with R1.

Macromodels for Operational Amplifiers

The second interstage includes the capacitor C2, which in parallel with R2 forms the dominant pole f1,

Together with the first interstage defines the open-loop voltage gain Hvo.



Macromodels for Operational Amplifiers

Two diode limiters D3-V3 and D4-V4 define the maximum and minimum voltages at node 5.

Output swing.

Macromodels for Operational Amplifiers

$$C_2 = 1/2\pi \cdot R \cdot f_1$$

$$C_1 = 1/2\pi \cdot R \cdot f_2$$

$$G_1 = G_2 = \sqrt{H_{V0}} / R$$

$$V_2 = \frac{C_2 \cdot SR^+}{G_2} = \frac{SR^+}{2\pi \cdot f_1 \cdot \sqrt{H_{V0}}}$$

$$V_1 = \frac{C_2 \cdot SR^-}{G_2} = \frac{SR^-}{2\pi \cdot f_1 \cdot \sqrt{H_{V0}}}$$

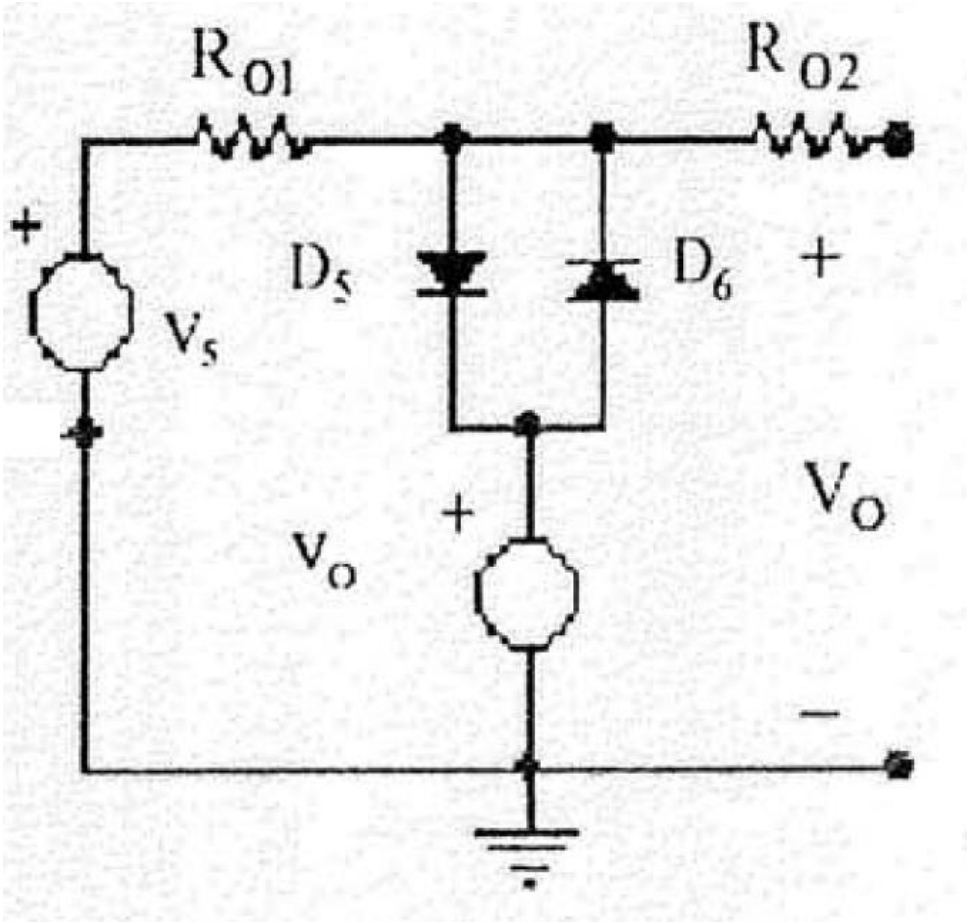
$$V_3 = V_{O\,\min}$$

$$V_4 = V_{O\,\max}$$

$$G_{\mathrm{CM}} = \frac{V_{1'} - V_{2'}}{(V_{1'} + V_{2'})/2} = \frac{1}{\mathrm{CMRR}}$$

$$I_{B2} = I_{B1} + I_{OF}.$$

Macromodels for Operational Amplifiers



Current limits are specified by the diodes D5 and D6

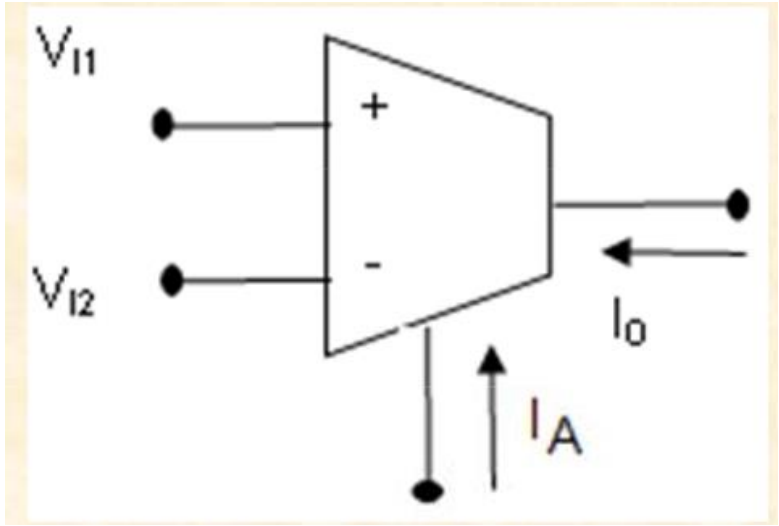
Macromodels for Operational Transconductance Amplifiers

Simple and accurate nonlinear OTA macromodel for simulation of CMOS OTA-C active filters

HAKAN KUNTMAN·

INT. J. ELECTRONICS, 1994, VOL. 77, NO. 6, 993–1006

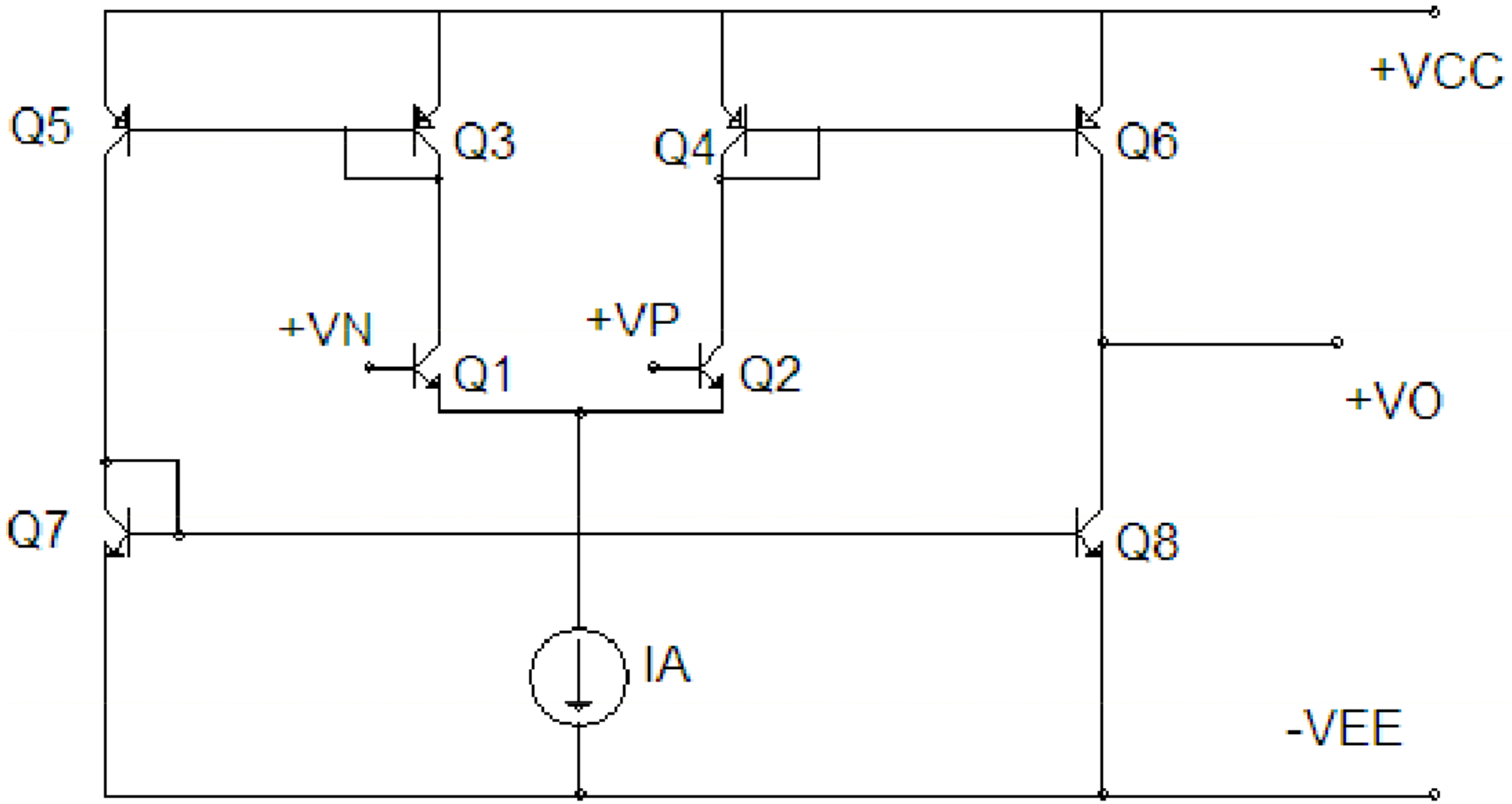
Macromodels for Operational Transconductance Amplifiers



Voltage Controlled Current Source

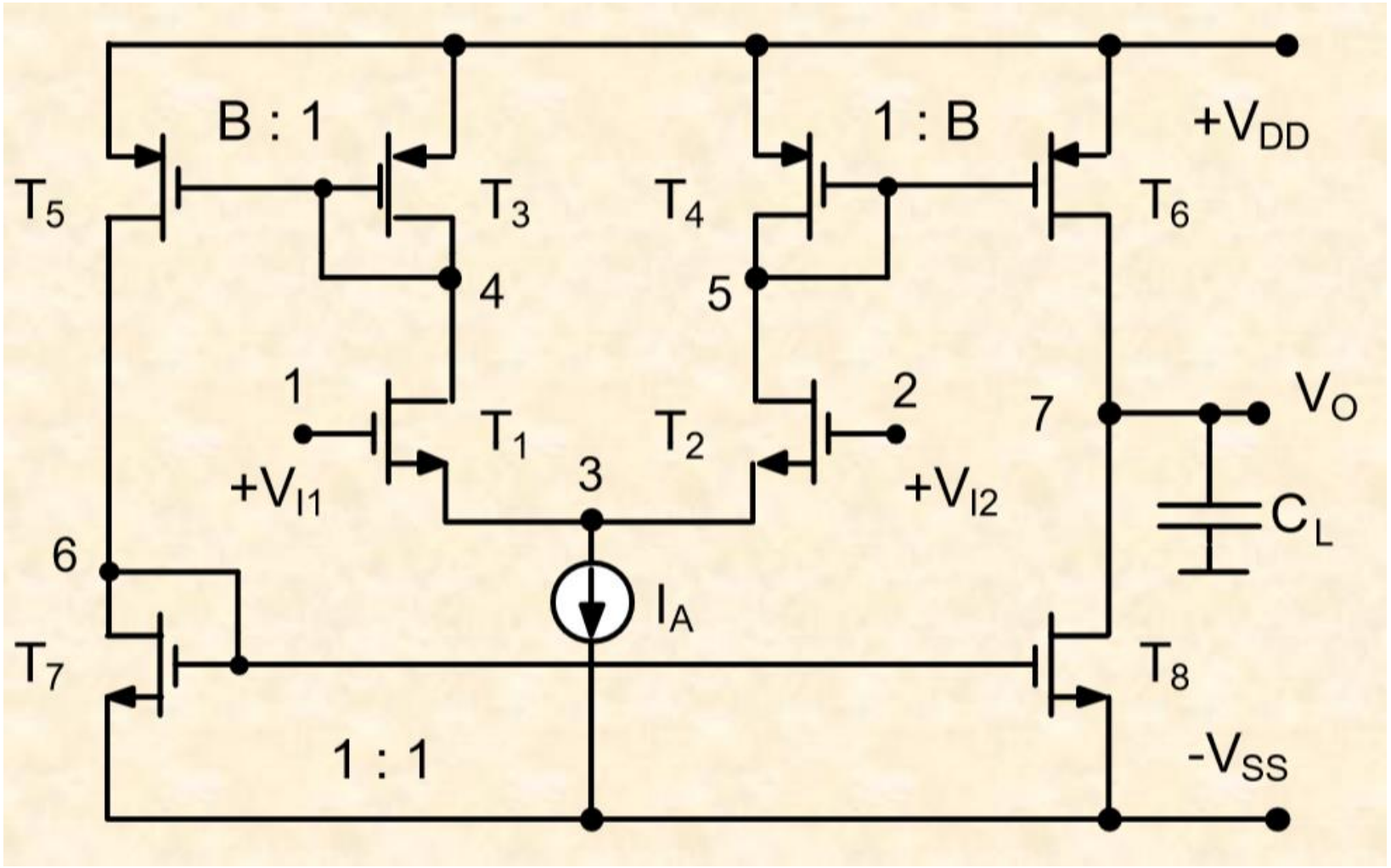
$$G_m = \frac{I_O}{V_{I1} - V_{I2}}, \qquad G_m = f(I_A)$$

Macromodels for Operational Transconductance Amplifiers



BJT OTA

Macromodels for Operational Transconductance Amplifiers



CMOS OTA

Macromodels for Operational Transconductance Amplifiers

$$G_m = B.\sqrt{K_n.I_A.(W/L)_1}$$

$$I_{Omaks} = -I_{Omin} = -B.I_A$$

$$K_V = G_m.R_O$$

$$f_d = \frac{1}{2.\pi.R_O.(C_{n7}+C_L)}$$

CMOS OTA Equations

Macromodels for Operational Transconductance Amplifiers

$$f_{nd1} = \frac{g_{m4}}{2.\pi.C_{n5}}$$

$$YE = \frac{B.I_A}{C_L + C_{n7}}$$

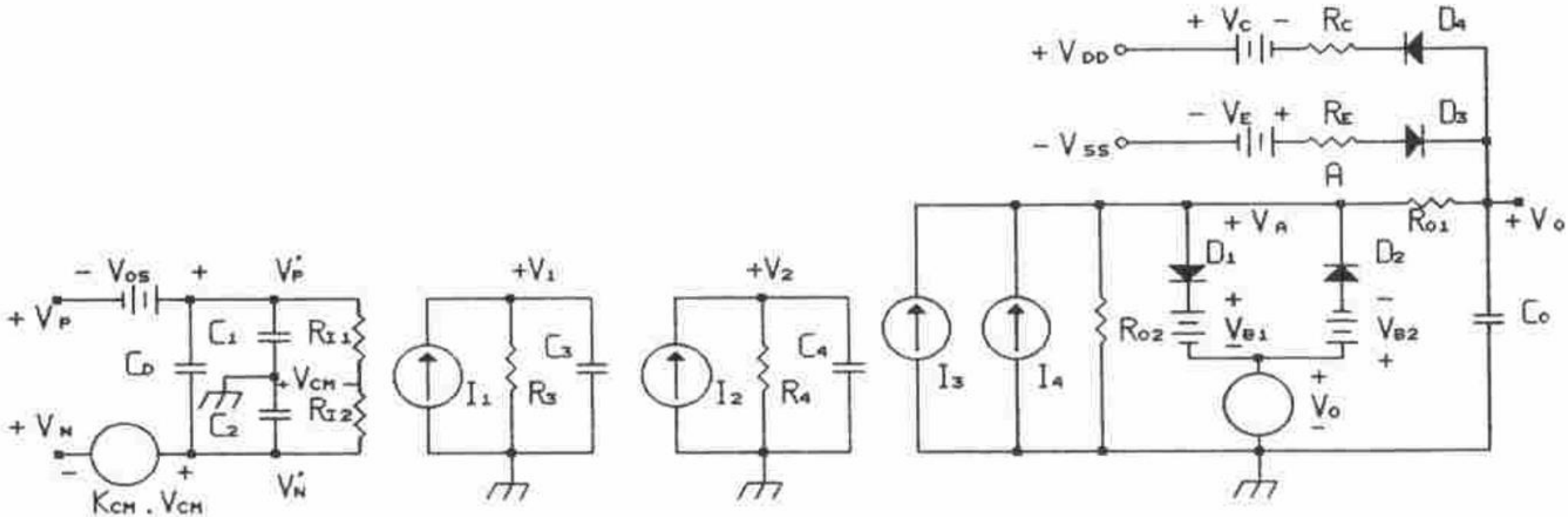
$$f_{nd2} = \frac{g_{m7}}{2.\pi.C_{n6}} \qquad f_z = 2.f_{nd2}$$

$$B = \frac{(W/L)_6}{(W/L)_4} = \frac{(W/L)_5}{(W/L)_3}$$

$$GBW = K_V.f_d$$

CMOS OTA Equations

Macromodels for Operational Transconductance Amplifiers



$I_1 = g_{m1} \cdot V_{ID}$ $I_2 = g_{m5} \cdot V_1$ $I_3 = g_{m7} \cdot V_2$

$V_{ID} = V'_P - V'_N$ $I_4 = G \cdot (V_A - V_O)$ $R_3 = 1 / g_{m4}$

$R_4 = 1 / g_{m7}$ $C_3 = C_{n5}$ $C_4 = C_{n6} / 2$

Macromodels for Operational Transconductance Amplifiers

The input stage produces the necessary linear and nonlinear differential and common-mode input characteristics capacitors C_1, C_2, C_D, resistors R_{I1}, R_{I2}, independent voltage source V_{OS} controlled voltage source $K_{CM} \cdot V_{CM}$

Macromodels for Operational Transconductance Amplifiers

The first interstage represents the behaviour of the differential input pair,

the first non-dominant pole f_{nd1}, caused by the total resistance and capacitnce at node 5.

$R_3 = 1/g_{m4}$, $C_3 = C_{n5}$ the total capacitance at node 5

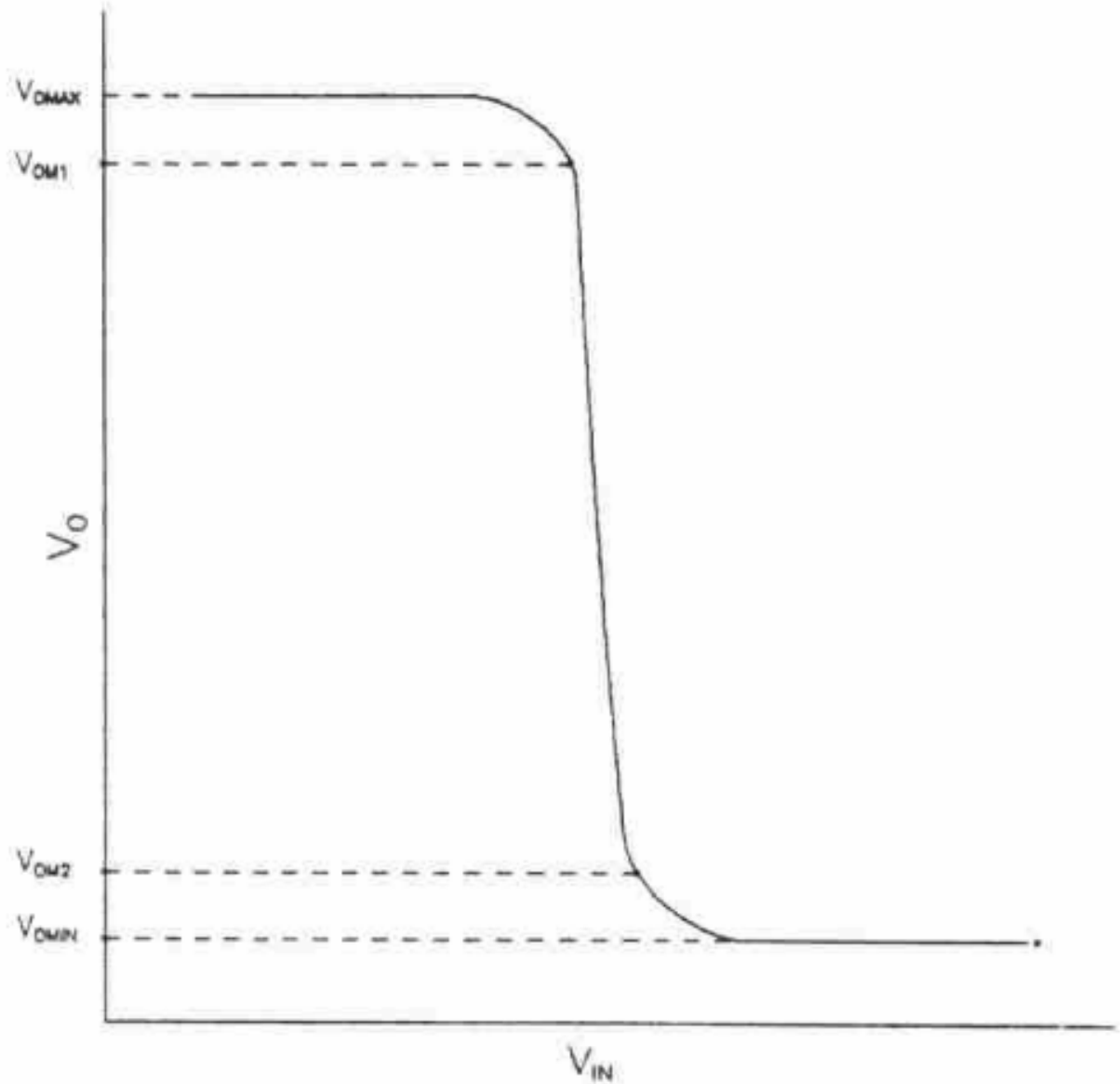
$A_{v1} = g_{m1}/g_{m4}$ gain of differential pair

Macromodels for Operational Transconductance Amplifiers

The second interstage models the behaviour of the current mirrors T4-T6, T3-T5 and T7-T8.

The resistor $R_4=1/g_{m7}$ and the capacitor C_4 produce the second non-dominant pole.

$I_2=g_{m5}.V_1$ represents the multiplication by the factor B



Boundaries of linear operating region.

$$V_{B1} = -I_{Omax} R_{01} - V_D$$

$$I_{S1} = -I_{Omax} \exp\left[-\frac{V_D}{V_T}\right]$$

$$V_{B2} = I_{Omin} R_{01} - V_D$$

$$I_{S2} = I_{Omin} \exp\left[-\frac{V_D}{V_T}\right]$$

$$R_C = \frac{V_{Omax} - V_{OM1}}{-I_{Omax}}$$

$$V_C = V_{DD} - V_{OM1} - V_\gamma$$

$$R_E = \frac{|V_{Omin}| - |V_{OM2}|}{I_{Omin}}$$

$$V_E = V_{EE} - |V_{OM2}| + V_\gamma$$

$$R_{02} = \frac{A_V}{G_m}$$

$$R_{01} = R_0 - R_{02}$$

$$G = \frac{-G_m(V_P - V_N)_{amax} + |I_{Omax}|}{|I_{Omax}| R_{01}}$$

Macromodels for Operational Transconductance Amplifiers

	$W(\mu m)$	$L[\mu m)$
T1	100	5
T2	100	5
T3	25	5
T4	25	5
T5	75	5
T6	75	5
T7	20	5
T8	20	5

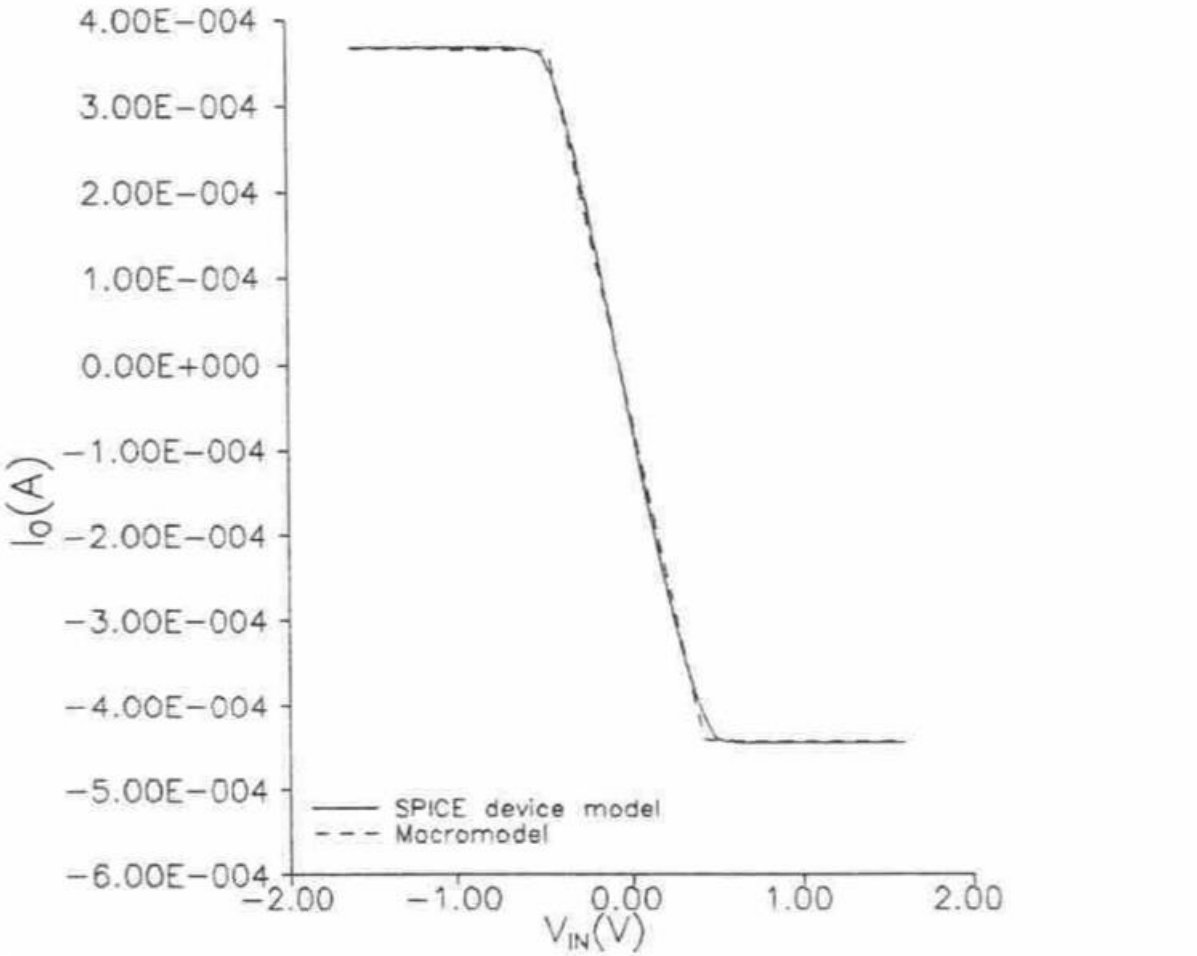
Dimensions of MOS transistors in CMOS OTA structure.

Macromodels for Operational Transconductance Amplifiers

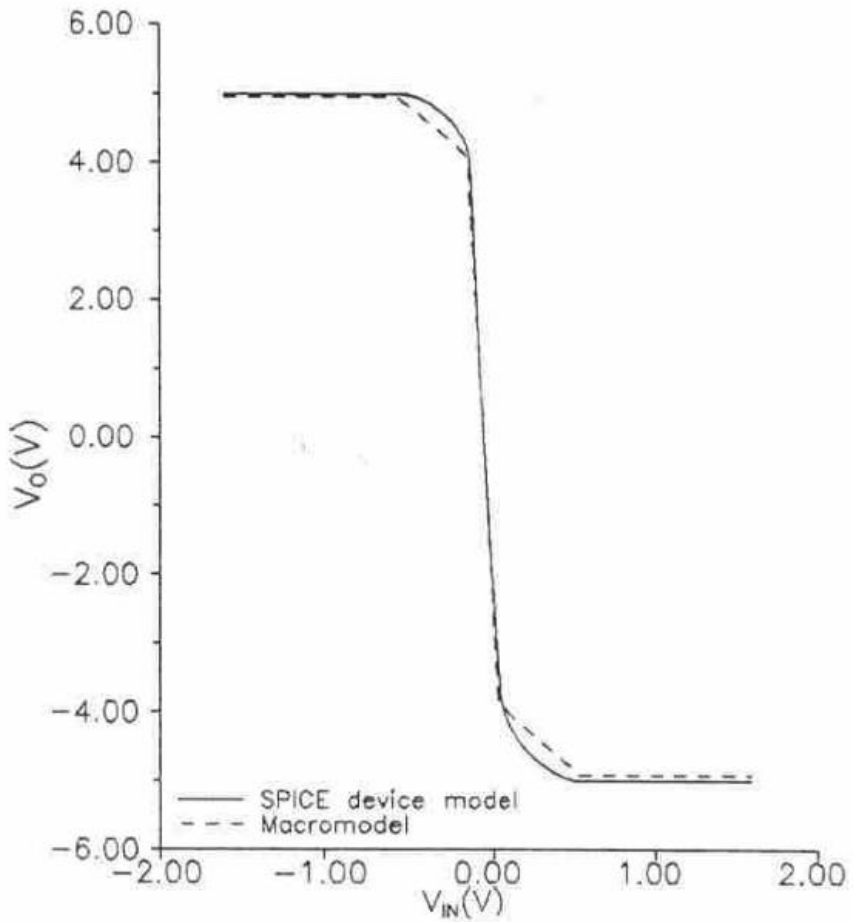
V_{OS}	59E−3	V	R_4	4·132	kΩ
V_{B1}	10·7	V	C_4	0·06018	pF
V_{B2}	13·11	V	R_5	42	kΩ
V_C	1·46	V	R_6	31	kΩ
V_E	1·673	V	C_0	0·15	pF
R_1	12·0E+12	Ω	R_C	2·2	kΩ
R_2	12·0E+12	Ω	R_E	2·2	kΩ
C_1	0·028	pF	g_{m1}	2·72E−4	AV^{-1}
C_2	0·028	pF	g_{m5}	3·04E−4	AV^{-1}
C_D	0·153P	pF	g_{m7}	2·42E−4	AV^{-1}
R_3	12·626	kΩ	G	2·25E−5	AV^{-1}
C_3	0·338	pF	K_{CM}	1E−3	—

Model parameters of derived OTA macromodel for $I_A = 100\,\mu A$.

Macromodels for Operational Transconductance Amplifiers

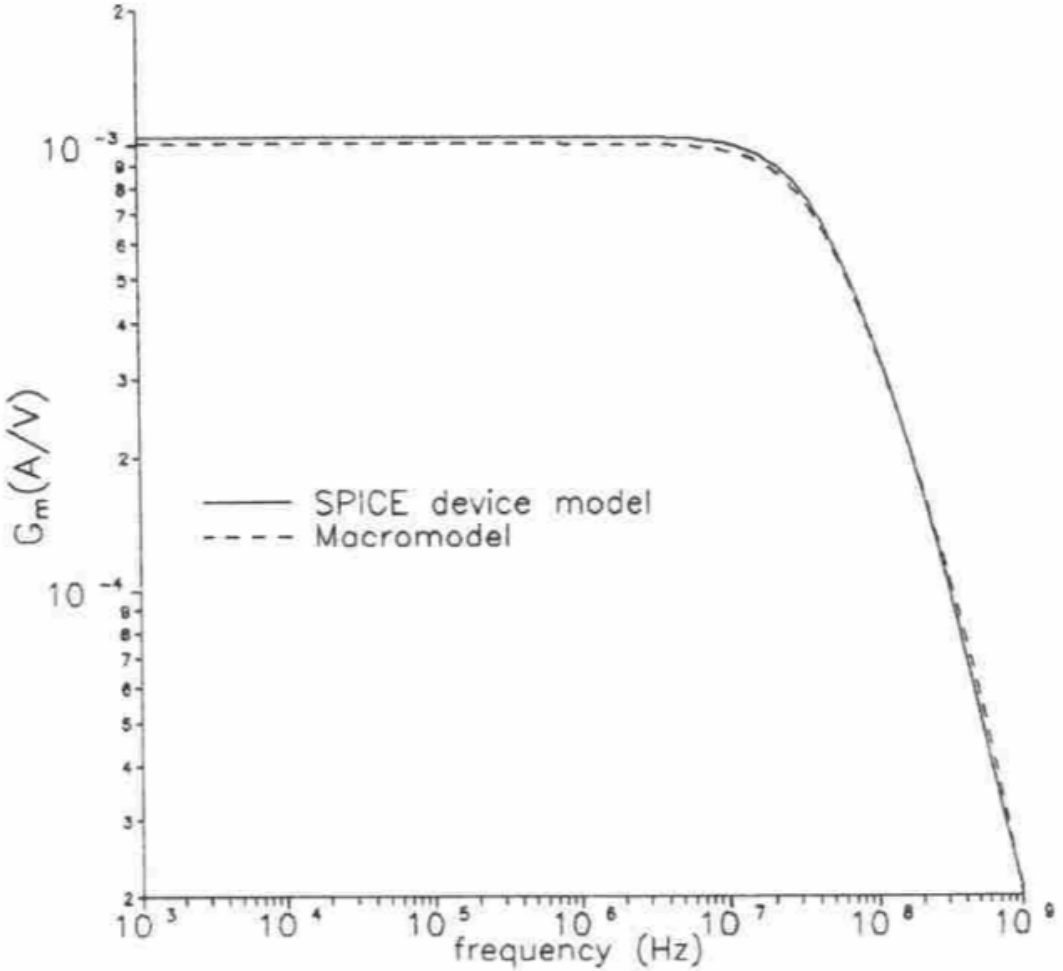


Simulated plots of I_O against $(V_P - V_N)$ for grounded non-inverting input.

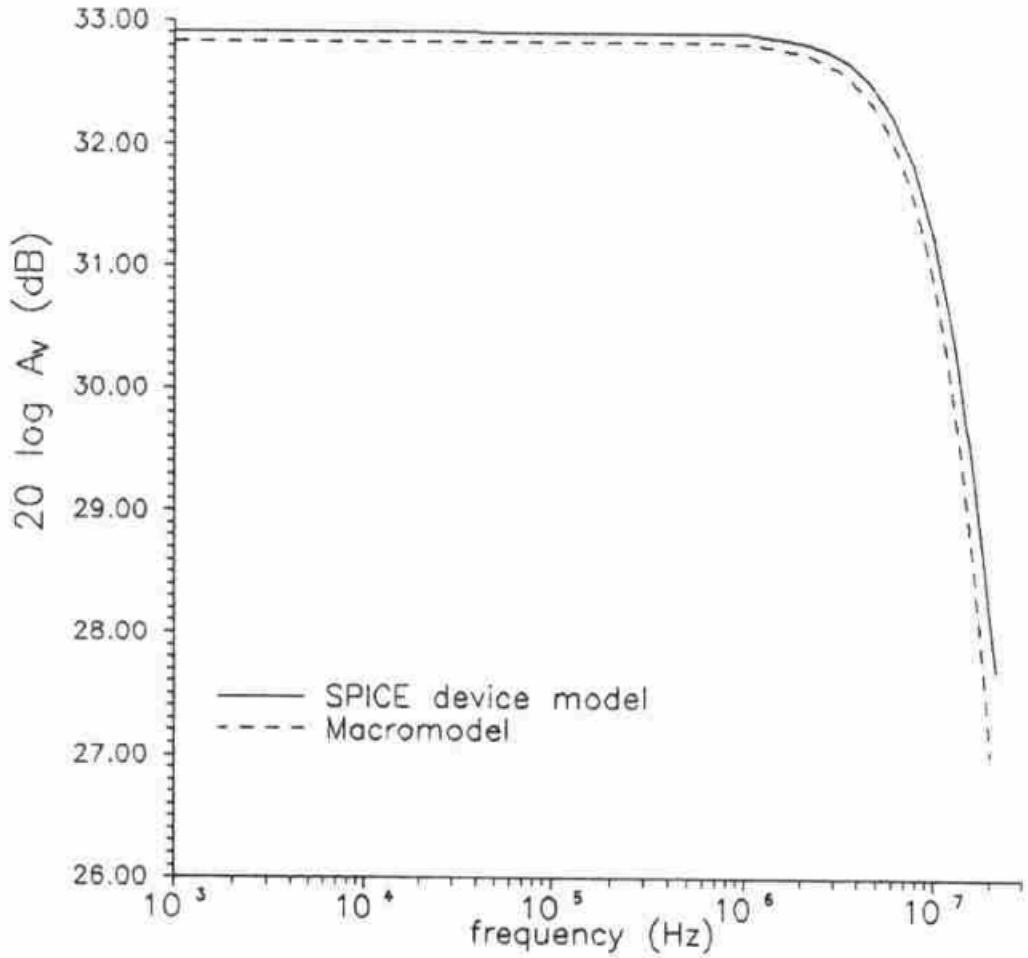


Simulated plots of V_O against $(V_P - V_N)$ for grounded non-inverting input.

Macromodels for Operational Transconductance Amplifiers

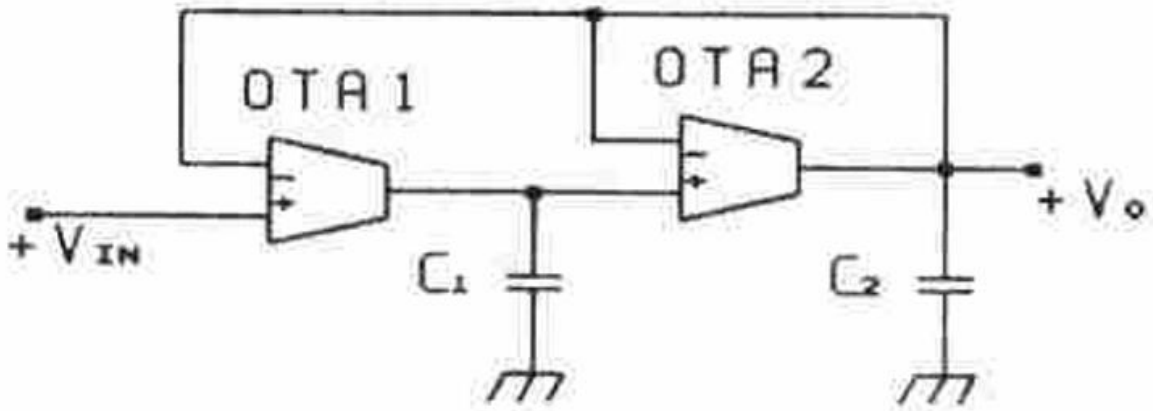


Simulated plots of OTA transconductance G_m against frequency for $I_A = 100\,\mu A$.

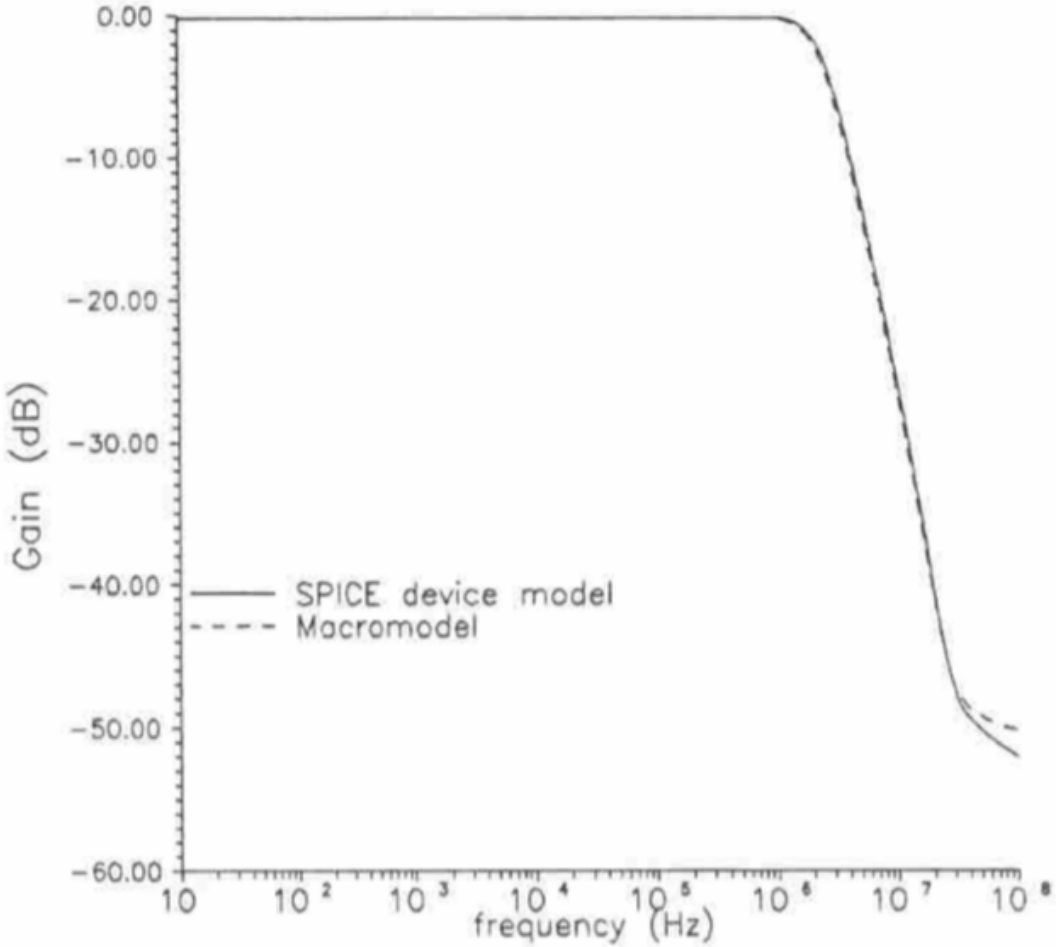


Simulated plots of voltage gain A_V against frequency for $I_A = 100\,\mu A$.

Macromodels for Operational Transconductance Amplifiers

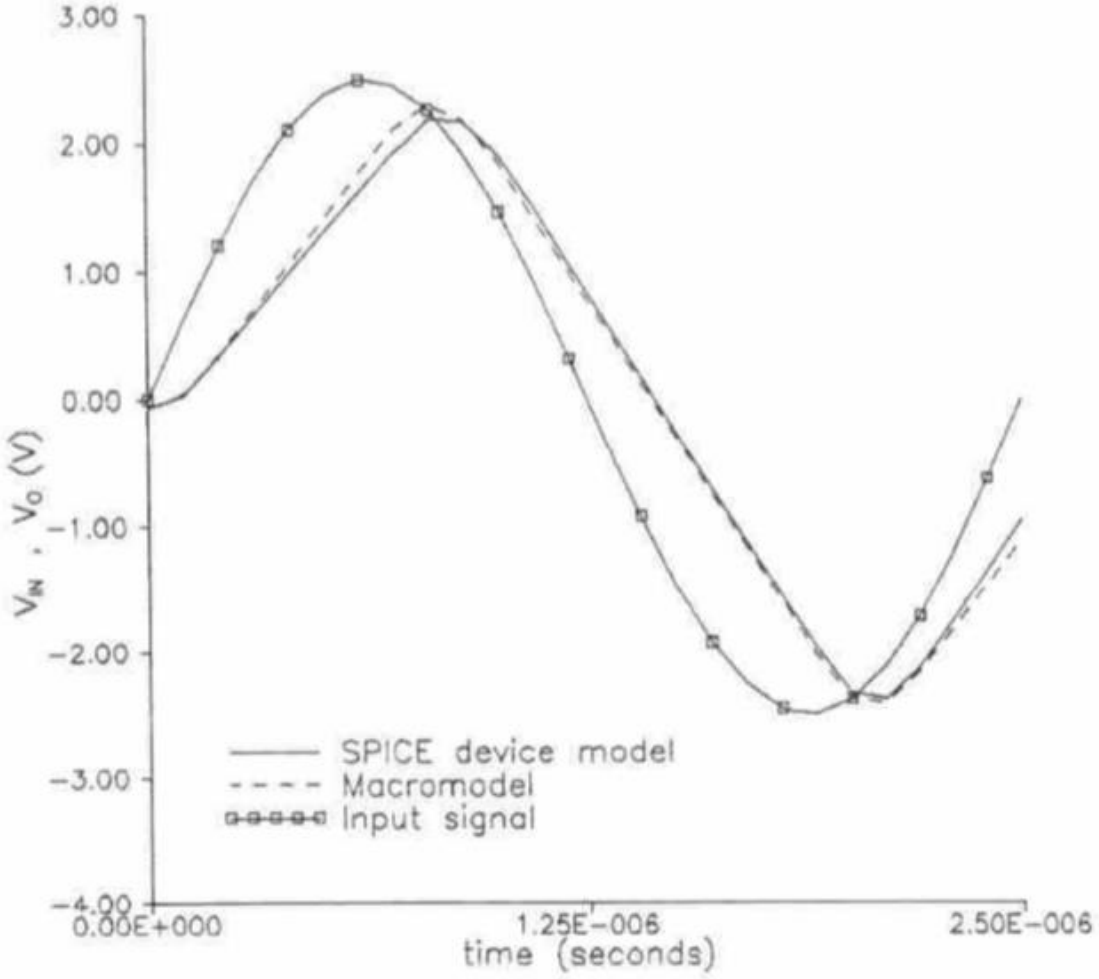


Second-order OTA-C filter.



Frequency response of OTA-C filter.

Macromodels for Operational Transconductance Amplifiers



Transient analysis results of OTA-C filter shown in Fig. 8 for a 400 kHz sinusoidal voltage with an amplitude of $V_{OP} = 2{\cdot}5$ V.

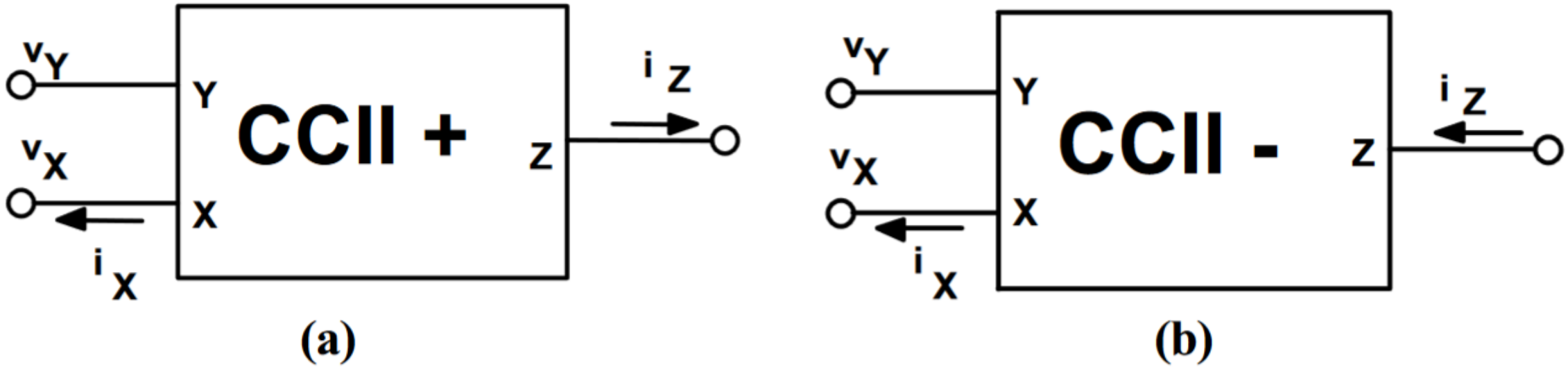
Macromodels for Current Conveyors

SIMPLE AND ACCURATE NON-LINEAR CURRENT CONVEYOR MACROMODEL SUITABLE FOR SIMULATION OF ACTIVE FILTERS USING CCIIs

NIL TARIM, BERNA YENEN AND HAKAN KUNTMAN

INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS Int. J. Circ. Theor. Appl., 26, 27—38 (1998)

Macromodels for Current Conveyors



Circuit symbol of the second generation current conveyor CCII
a) non-inverting (positive) CCII+ b) inverting (negative) CCII-

CCII is a three port active device where the current is transferred between ports with different impedance levels.

Macromodels for Current Conveyors

The behaviour of the ideal current conveyor is characterized by

$$\begin{pmatrix} I_Y \\ V_X \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix}$$

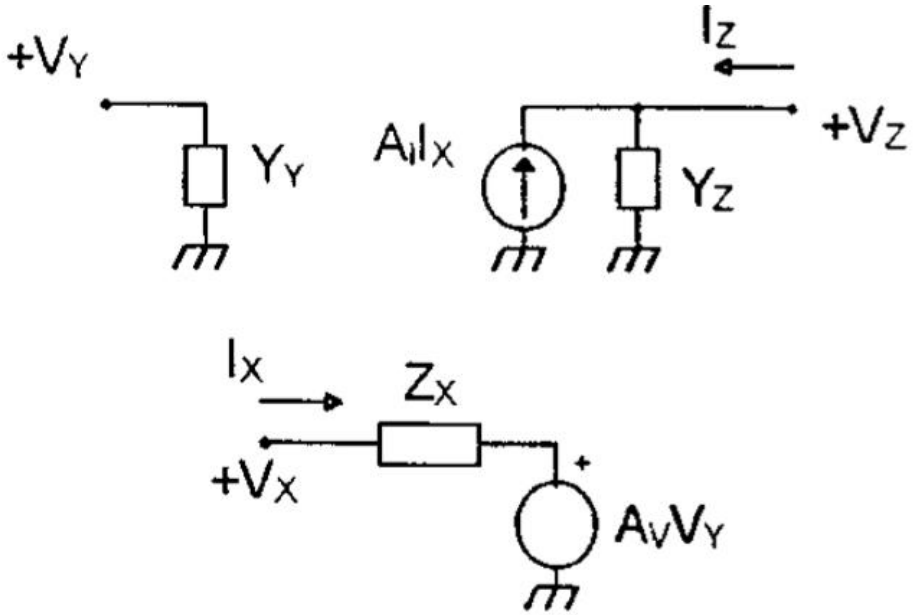
Macromodels for Current Conveyors

The behaviour of an actual current conveyor differs from the ideal current conveyor

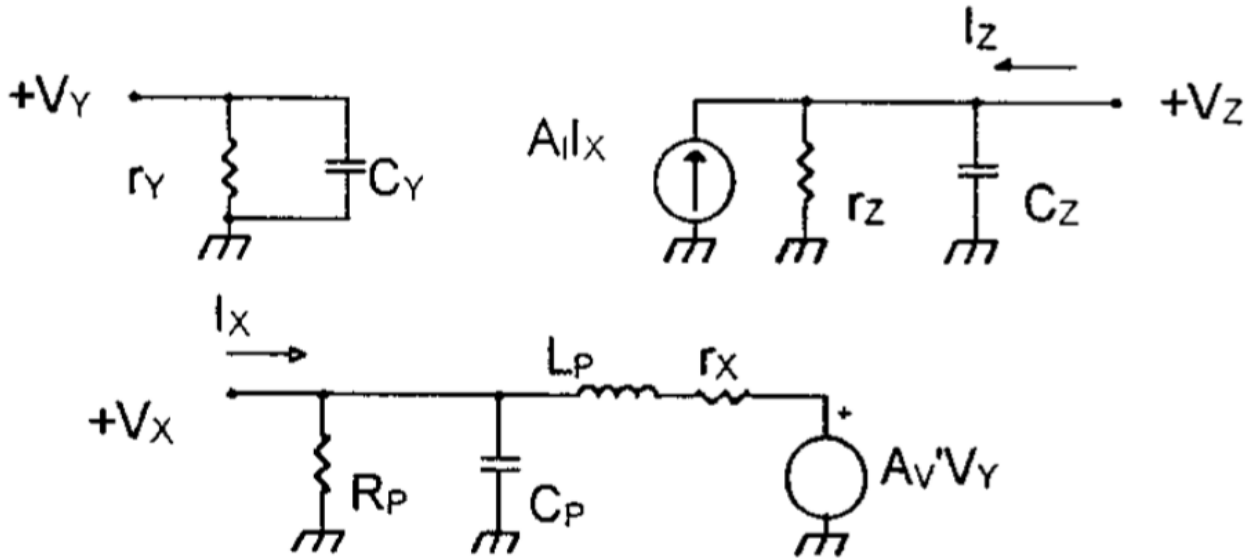
$$\begin{pmatrix} I_Y \\ V_X \\ I_Z \end{pmatrix} = \begin{pmatrix} Y_Y(s) & 0 & 0 \\ A_V(s) & Z_X(s) & 0 \\ 0 & \pm A_I(s) & Y_Z(s) \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix}$$

Macromodels for Current Conveyors

The behaviour of an actual current conveyor differs from the ideal current conveyor



(a)



(b)

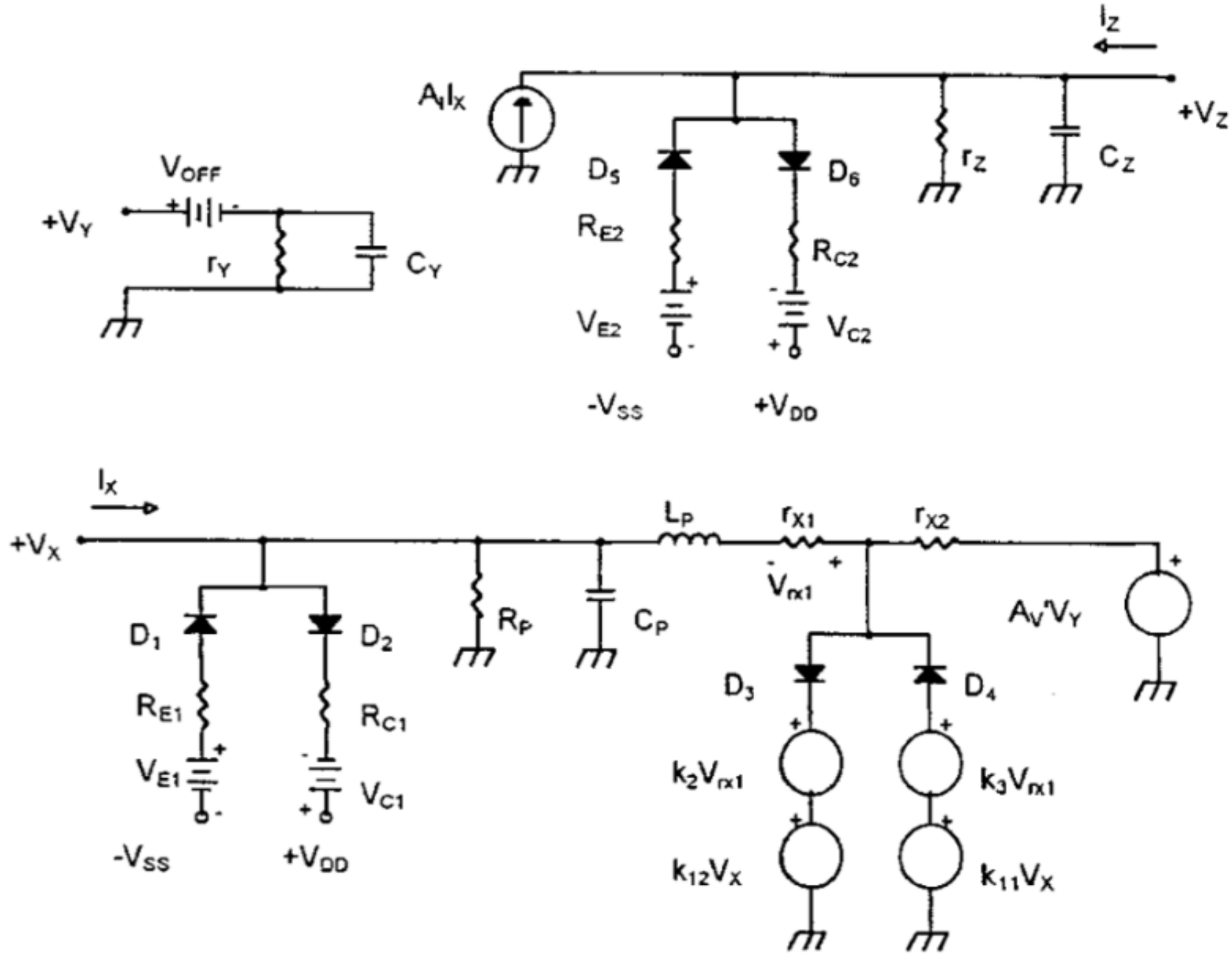
Macromodels for Current Conveyors

The limits of the characteristics

$$I_{X\min} < i_X(t) < I_{Xmaks}$$

$$V_{X\min} < v_X(t) < V_{Xmaks}$$

$$V_{Z\min} < v_Z(t) < V_{Zmaks}$$


I_Z
$A_I I_X$
$+V_Z$
V_{OFF}
$+V_Y$
r_Y
C_Y
D_5
D_6
r_Z
C_Z
R_{E2}
R_{C2}
V_{E2}
V_{C2}
$-V_{SS}$
$+V_{DD}$
I_X
$+V_X$
L_P
r_{X1}
r_{X2}
V_{rx1}
$A_V V_Y$
D_1
D_2
R_P
C_P
D_3
D_4
R_{E1}
R_{C1}
V_{E1}
V_{C1}
$k_2 V_{rx1}$
$k_3 V_{rx1}$
$k_{12} V_X$
$k_{11} V_X$
$-V_{SS}$
$+V_{DD}$

(c)

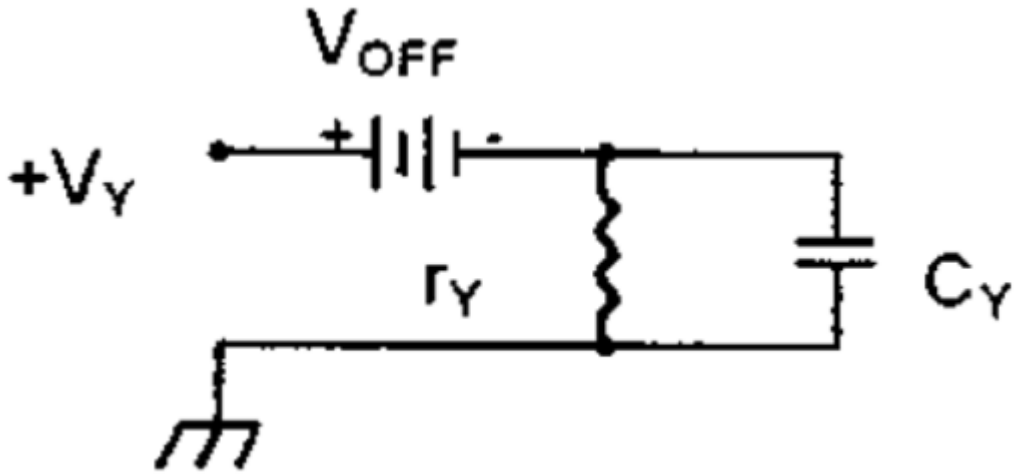
Macromodels for Current Conveyors

The derived macromodel is subdivided into three sections,

- the input stage (terminal Y),
- the intermediate stage (terminal X)
- the output stage (terminal Z).

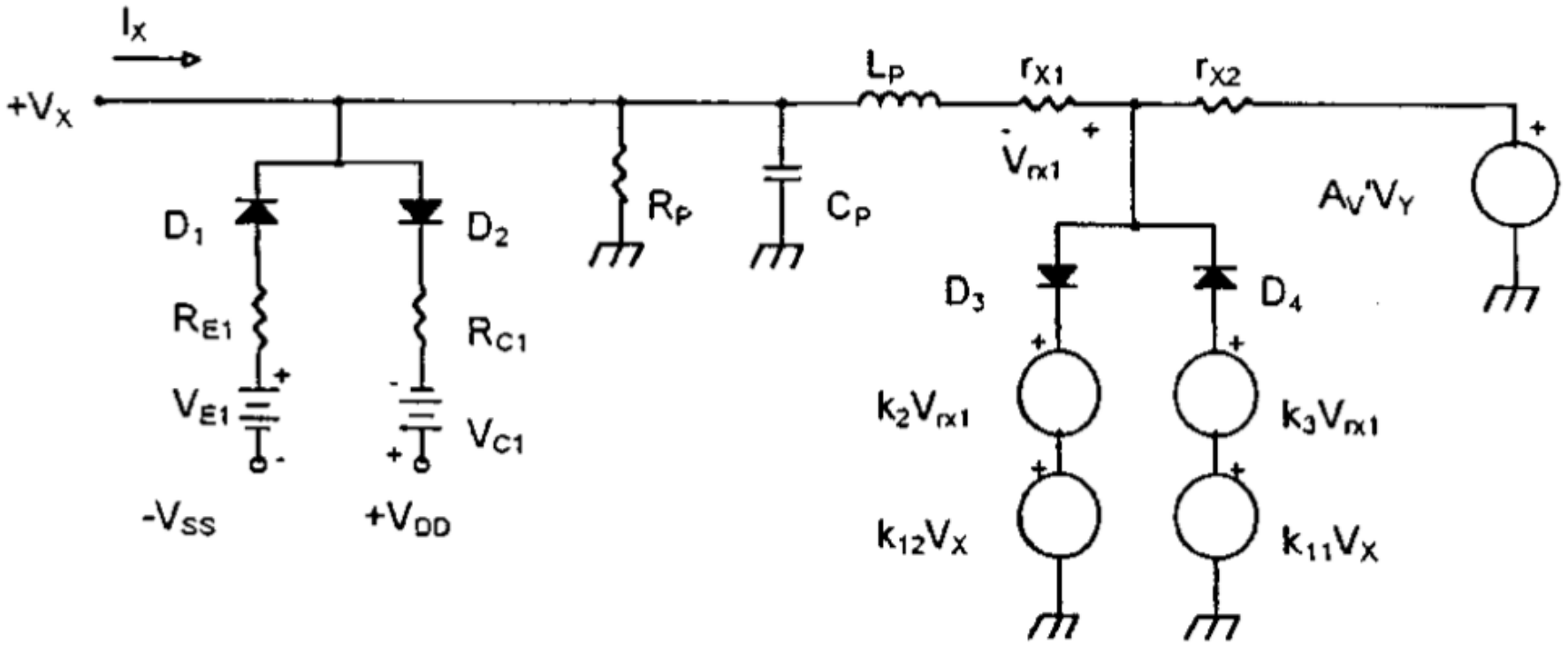
Macromodels for Current Conveyors

- The input impedance atY is represented by the resistor rY , the capacitor CY.
- The independent voltage source VOFF is for modelling of the offset voltage.



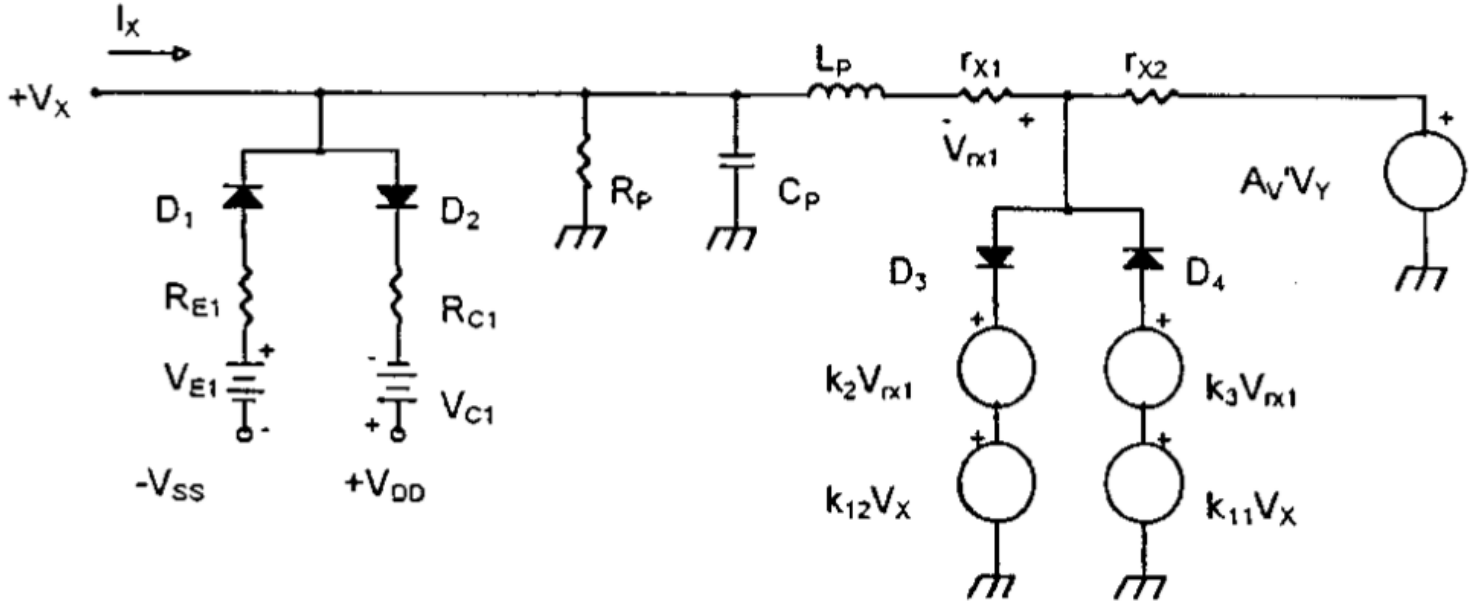
Macromodels for Current Conveyors

- The input impedance at X is represented by theresistors
- rX1, rX2, RP, the inductor LP and the capacitor CP



Macromodels for Current Conveyors

- The behaviour of an actual current conveyor shows a
- second-order character.
- An accurate representation of this second-order character is very important, it is the primary factor which determines the frequency response of the current conveyor.



Macromodels for Current Conveyors

$$Z_X(s) = \frac{1}{C_P} \frac{s + \dfrac{r_X}{L_P}}{s^2 + s\left(\dfrac{C_P R_P r_X}{C_P L_P R_P} + \dfrac{L_P}{C_P L_P R_P}\right) + \dfrac{r_X + R_P}{C_P L_P R_P}}$$

$$Z_X(s) = \frac{1}{C_P} \frac{s + \omega_Z}{s^2 + s\dfrac{\omega_P}{Q_P} + \omega_P^2}$$

Macromodels for Current Conveyors

The transfer function $H(s) = V_X/V_Y$ is given by

$$H(s) = H(0)\frac{\dfrac{R_E + r_x}{C_P L_P R_E}}{s^2 + s\left(\dfrac{C_P R_E r_X}{C_P L_P R_E} + \dfrac{L_P}{C_P L_P R_E}\right) + \dfrac{R_E + r_x}{C_P L_P R_E}}$$

$$H(0) = A_V'[R_E/(R_E + r_x)]$$

R_E is the parallel equivalent of the model parameter R_P with the external resistor R_X.

Macromodels for Current Conveyors

The transfer function $H(s) = V_X/V_Y$ is given by

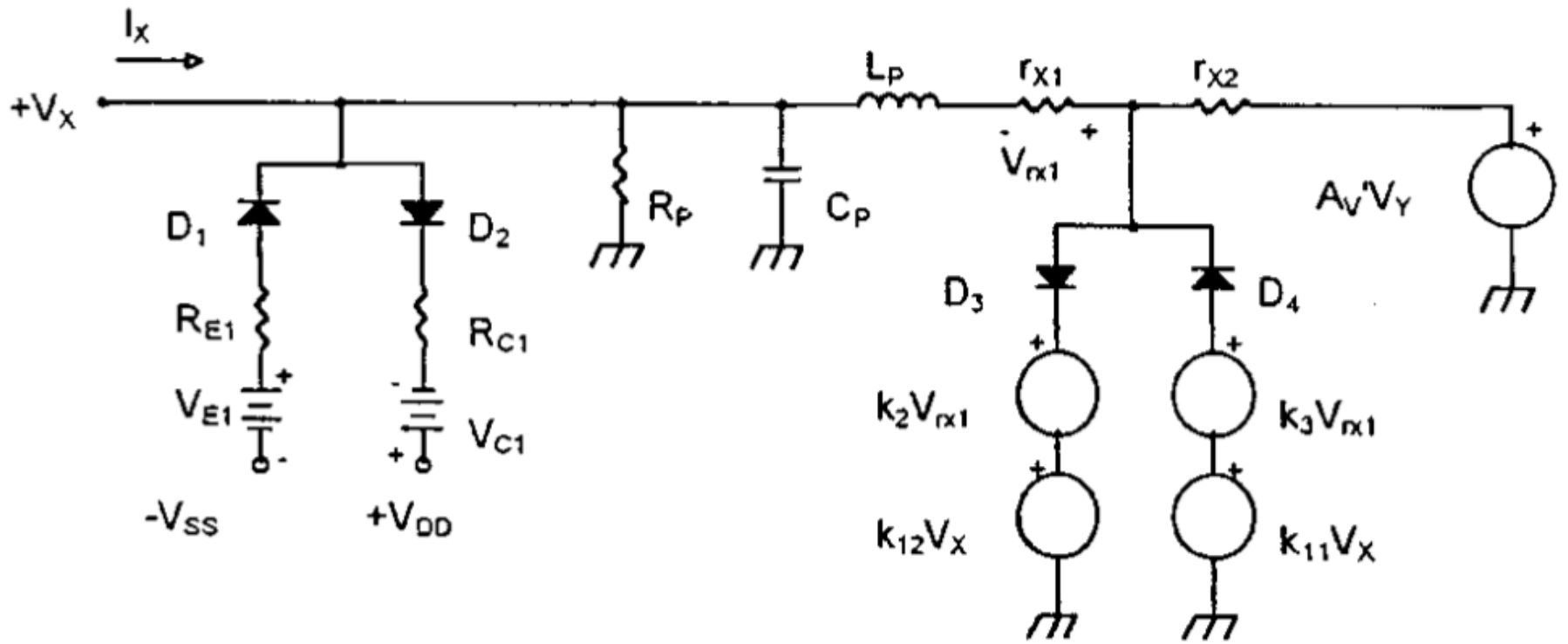
$$H(s) = H(0)\frac{\dfrac{R_E + r_x}{C_P L_P R_E}}{s^2 + s\left(\dfrac{C_P R_E r_X}{C_P L_P R_E} + \dfrac{L_P}{C_P L_P R_E}\right) + \dfrac{R_E + r_x}{C_P L_P R_E}}$$

$$H(0) = A_V'[R_E/(R_E + r_x)]$$

R_E is the parallel equivalent of the model parameter R_P with the external resistor R_X.

Macromodels for Current Conveyors

The voltage swing is limited by the voltage source-resistor-diode combinations VC1, D2, RC1, and VE1, D1, RE1.

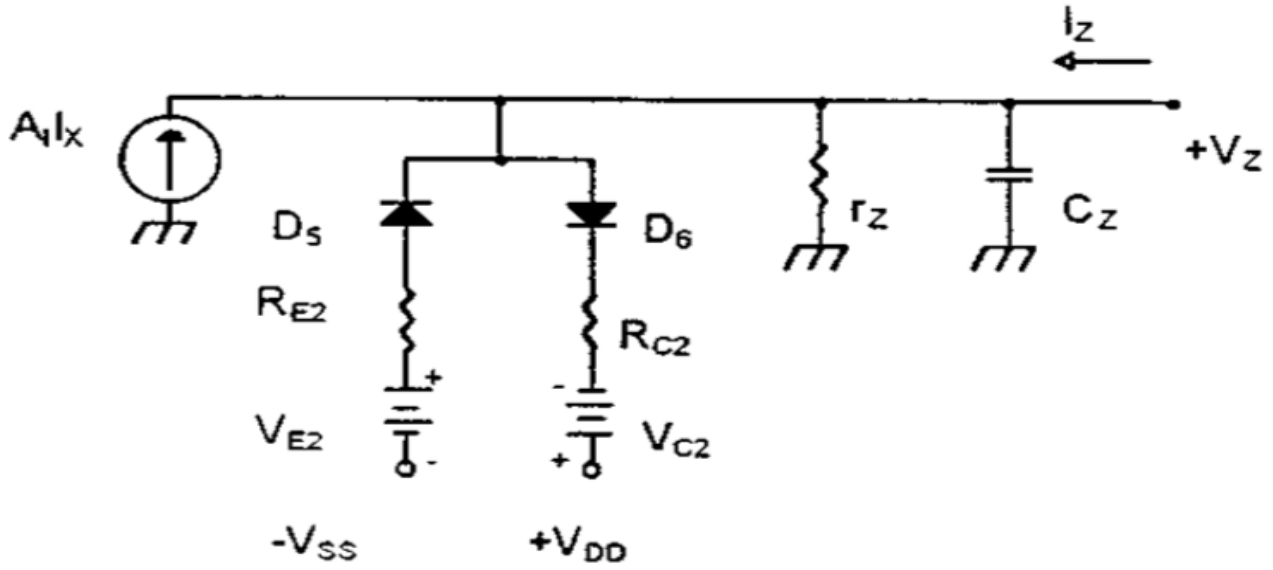


Macromodels for Current Conveyors

The output impedance at Z is modelled by the resistor rZ and the capacitor CZ.

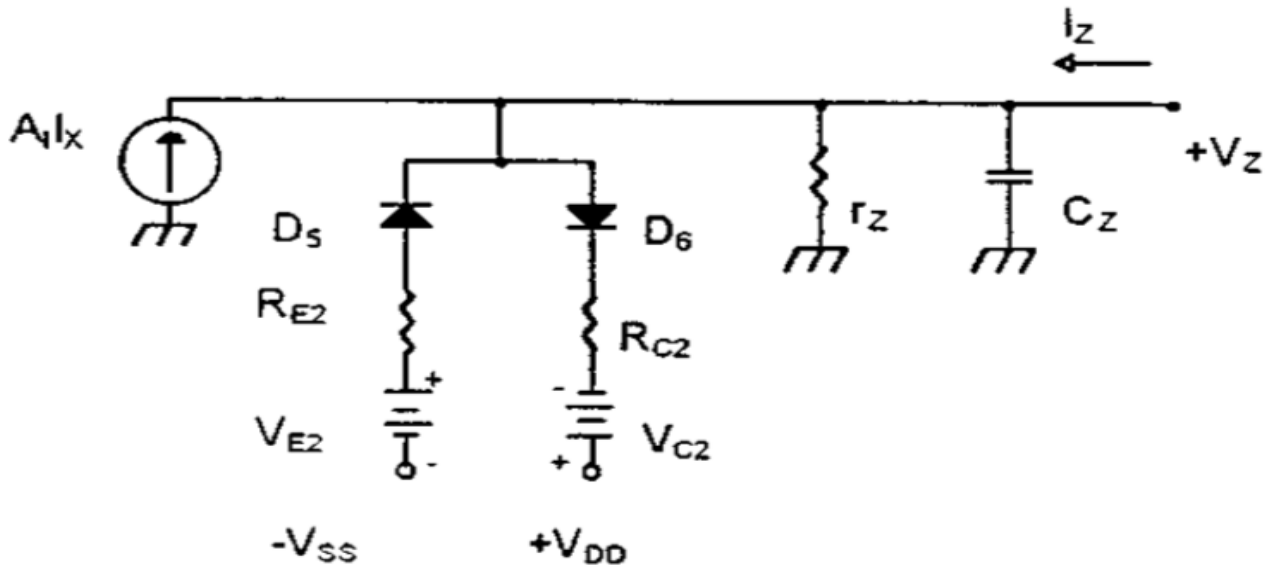
The current controlled current source I1=AI(s)*IX produces a current output at Z proportional to the current IX.

The output voltage excursion is limited by the voltage source-resistor-diode combinations VC2, D6, RC2 and VE2, D 5, RE2.



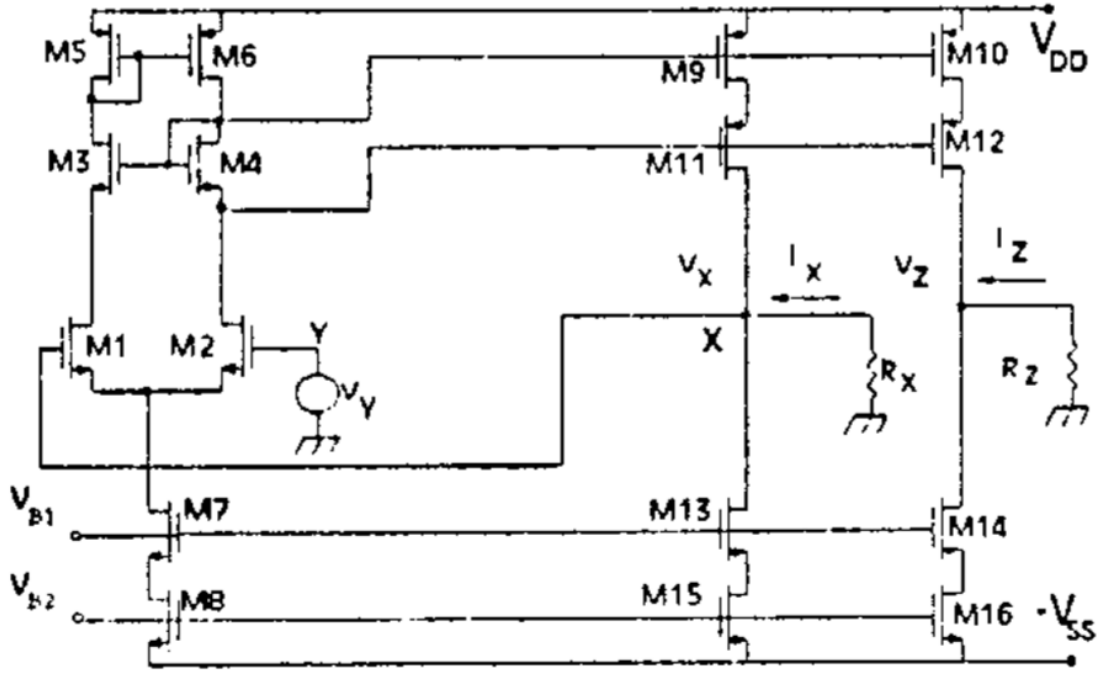
Macromodels for Current Conveyors

The resistors RC1, RE1, RC2 and RE2 are newly introduced resistive elements to the circuit model which adjust the slope of the DC voltage transfer by using a piecewise linear approximation which are not represented in the conventional macromodels for operational amplifiers.

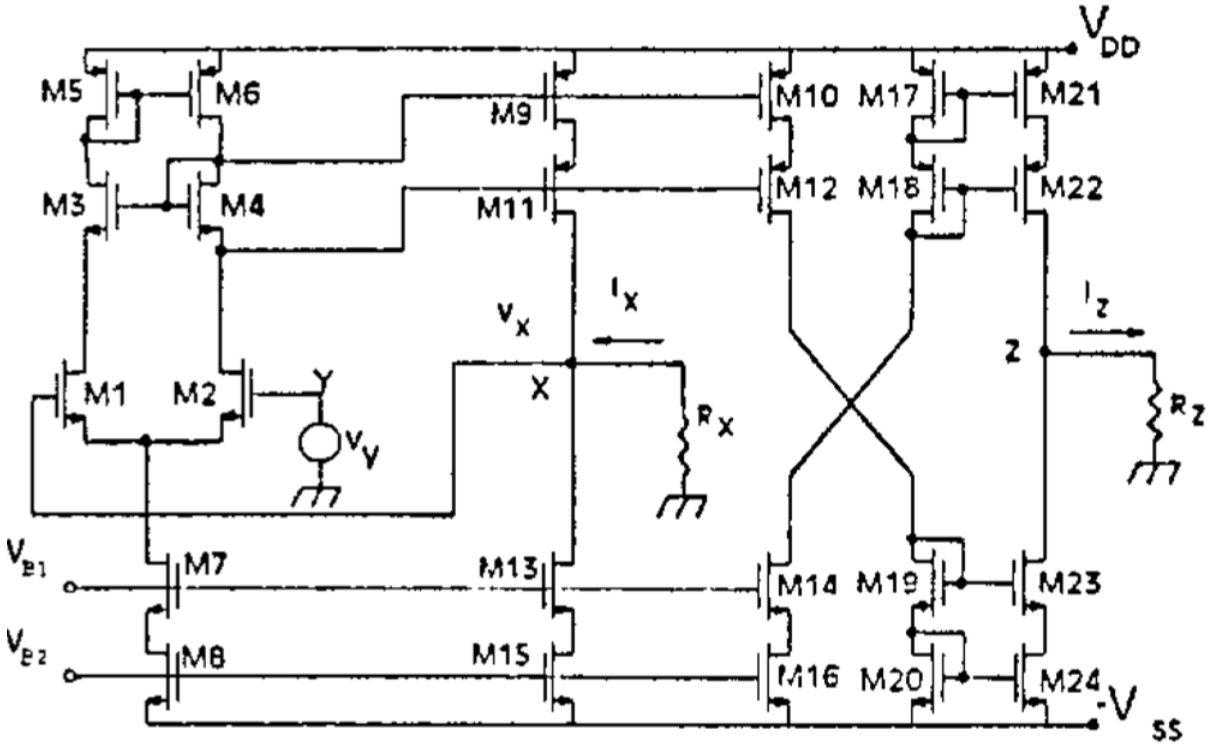


Macromodels for Current Conveyors

The accuracy of the current conveyor macromodel is demonstrated by comparing the simulated current conveyor characteristics with simulation results obtained from semiconductor device model.



CCII+



CCII-

Macromodels for Current Conveyors

Table I. Dimensions of the MOS transistors

Device	CCII $W(\mu)/L(\mu)$	CCII $W(\mu)/L(\mu)$	Device	CCII+ $W(\mu)/L(\mu)$	CCII− $W(\mu)/L(\mu)$
M1	17/10	17/10	M13	23/5	23/5
M2	17/10	17/10	M14	23/5	23/5
M3	17/10	17/10	M15	23/5	23/5
M4	17/10	17/10	M16	23/5	23/5
M5	24/5	24/5	M17	—	24/5
M6	24/5	24/5	M18	—	24/5
M7	23/5	23/5	M19	—	23/5
M8	23/5	23/5	M20	—	23/5
M9	24/5	24/4	M21	—	24/5
M10	24/5	24/5	M22	—	24/5
M11	24/5	24/5	M23	—	23/5
M12	24/5	24/5	M24	—	23/5

Macromodels for Current Conveyors

Parameter	NMOS	PMOS	Parameter	NMOS	PMOS
LD	0·414747U	0·580687U	TOX	505·0E-10	432·0E-10
VTO	0·864893	−0·944048	KP	44·9E-6	18·5E-6
GAMMA	0·981	0·435	PHI	0·6	0·6
UO	656	271	UEXP	0·211012	0·242315
UCRIT	106703	20581·4	DELTA	3·53172	4·3209E-5
VMAX	100000	33274·4	XJ	0·4U	0·4U
LAMBDA	0·0107351	0·0620118	NFS	1E11	1E11
NEFF	1·001	1·001	NSS	1E12	1E12
TPG	1	−1	RSH	9·925	10·25
CGDO	2·835E-10	4·831E-10	CGSO	2·835E-10	4·831-10
CGBO	7·968E-10	1·293E-9	CJ	0·0003924	0·0001307
MJ	0·456300	0·4247	CJSW	5·284E-10	4·613E-10
MJSW	0·3199	0·2185	PB	0·7	0·75
XQC	1	1	NSUB	1·3563E16	1E16

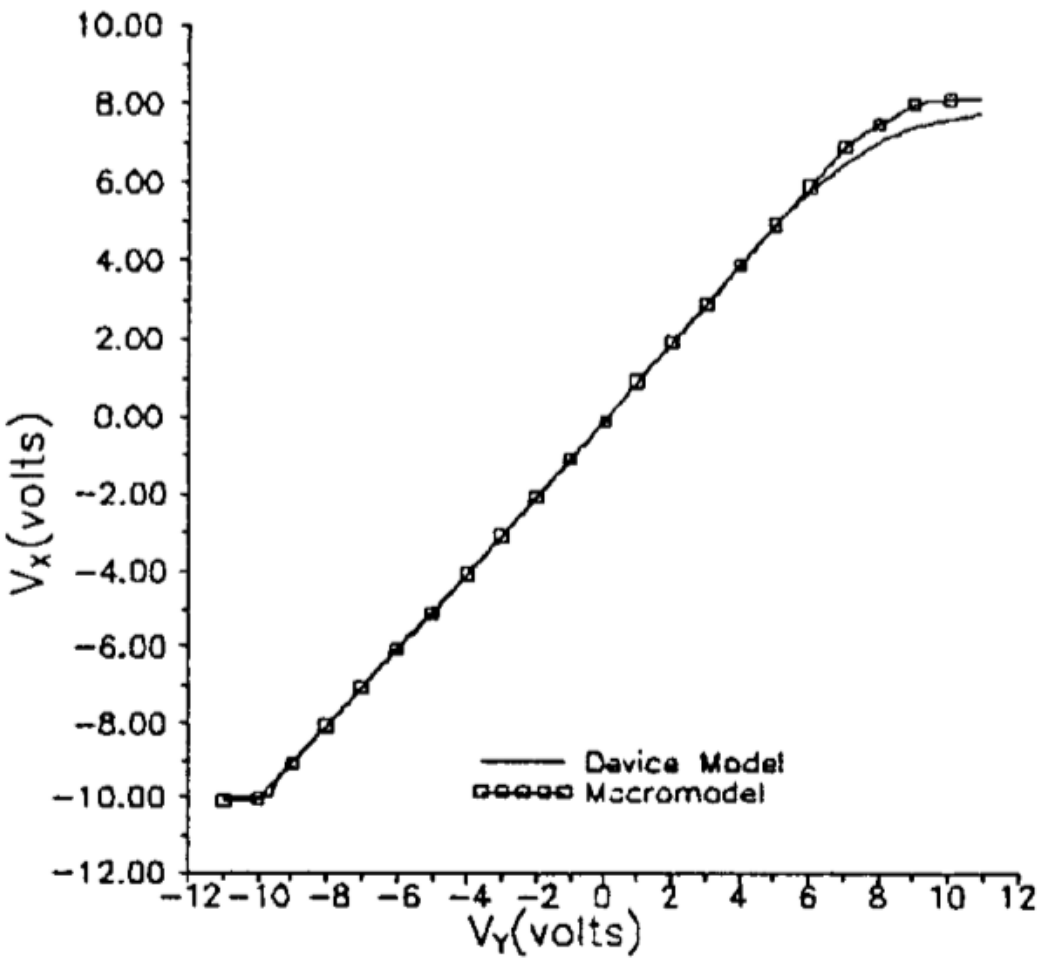
Macromodels for Current Conveyors

Table III. Macromodel parameters

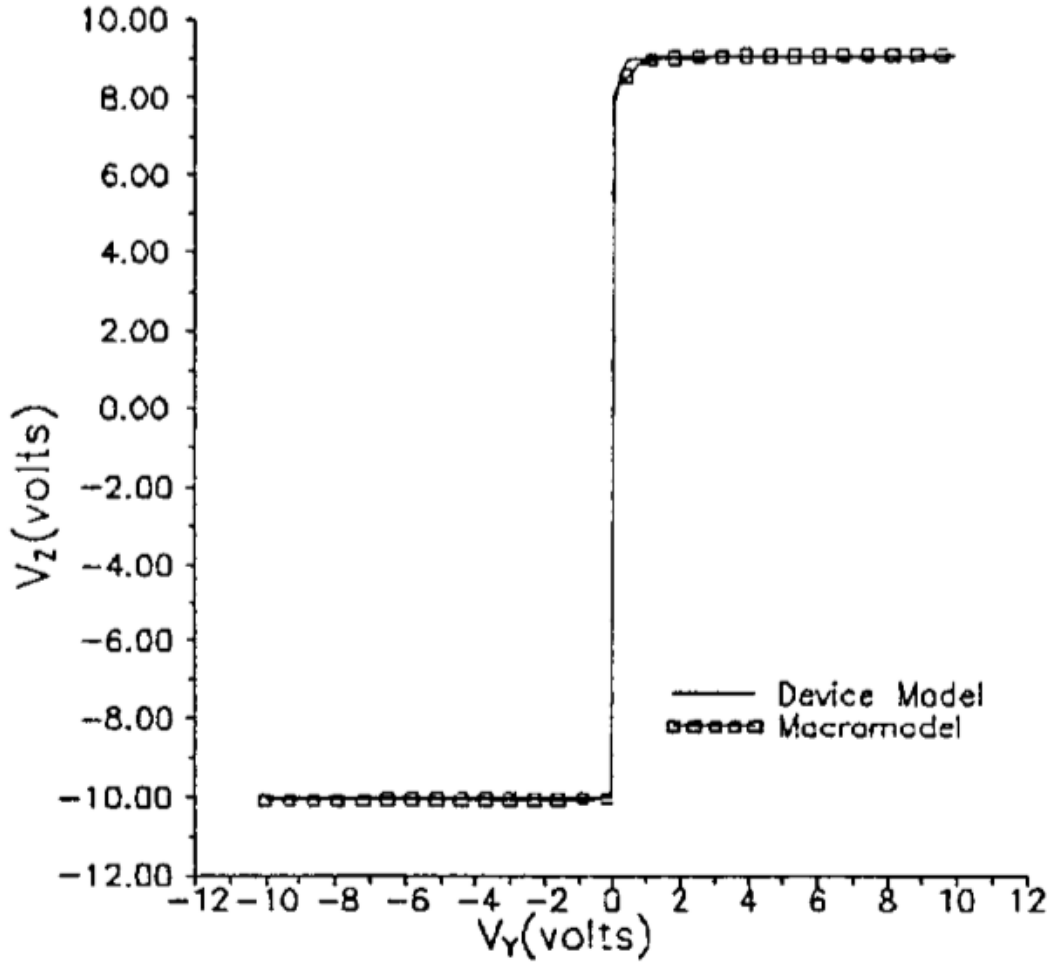
Parameter	Value	Parameter	Value
r_Y	1E12 Ω	k_2	−9
C_Y	0·0489 pF	k_3	−0·45
r_{X1}	327 Ω	I_{S1}	2E-14 A
r_{X2}	400 Ω	I_{S2}	10E-14 A
C_P	0·1 pF	I_{S3}	2E-14 A
L_P	31·2 μH	I_{S4}	10E-14 A
R_P	26 kΩ	I_{S5}	2E-14 A
A_V	1	I_{S6}	2E-14 A
k_{11}	1	A_I	1*
k_{12}	1	V_{OFF}	−63 mV
r_Z	805 kΩ	C_Z	0·16 pF
R_{C1}	833 Ω	V_{C2}	2·45 V
V_{C1}	3·5 V	R_{E2}	1750 Ω
R_{E1}	1 Ω	V_{E2}	0·9 V
V_{E1}	0·5 V	—	—
R_{C2}	640 Ω	—	—

* For inverting current conveyor $A_I = -1$.

Macromodels for Current Conveyors



(a)



(b)

Voltage transfer characteristics obtained from SPICE simulations: (a) plots of V_X against V_Y for $R_X = \infty$ and (b) plots of V_Z against V_Y for $R_Z = \infty$

Macromodels for Current Conveyors

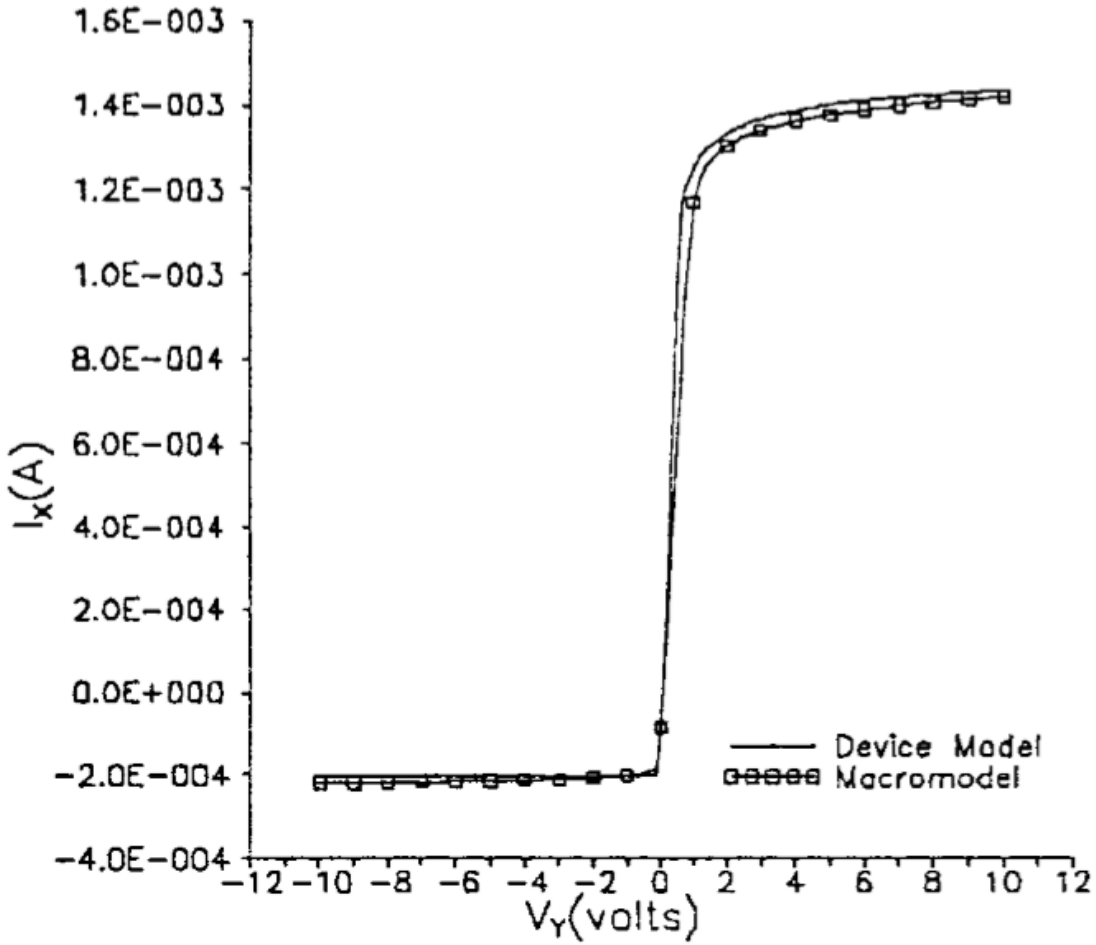
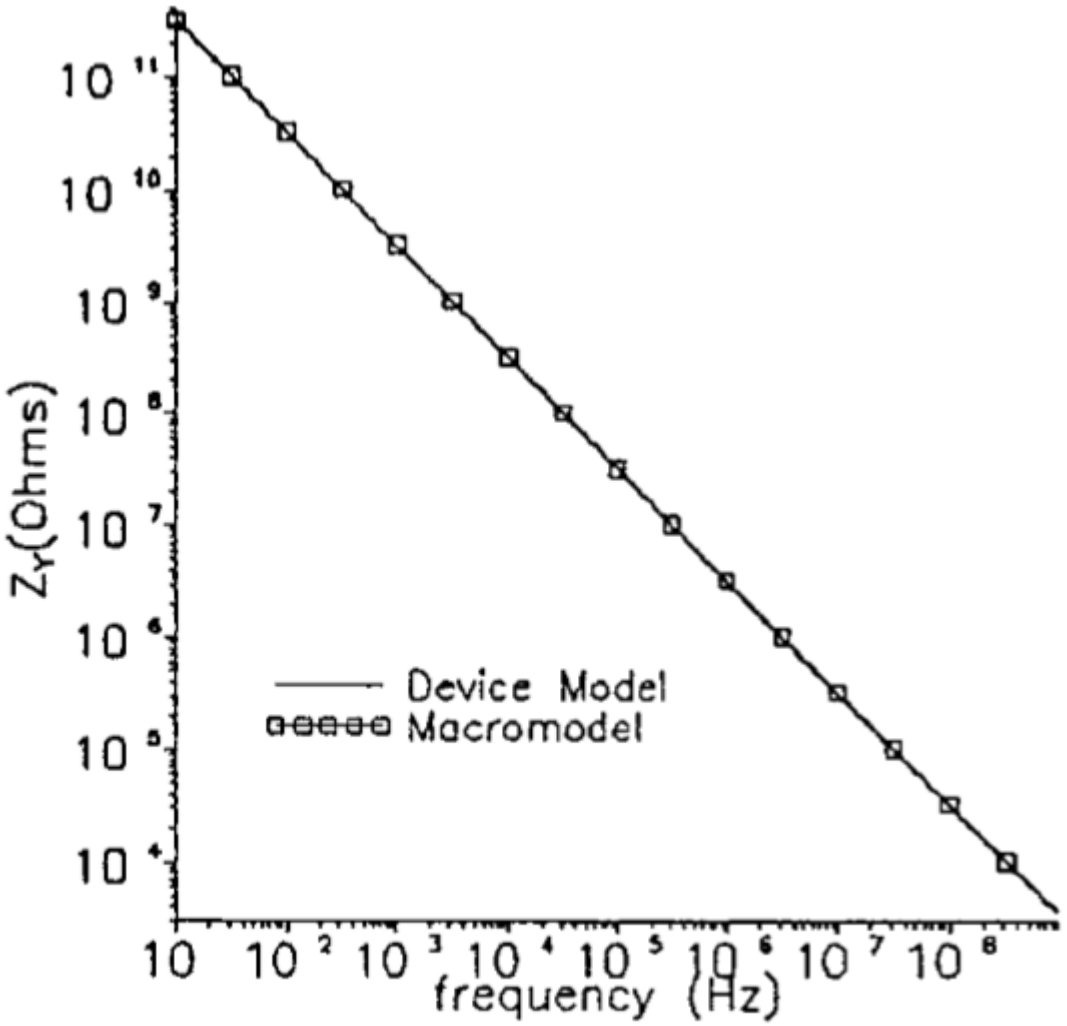
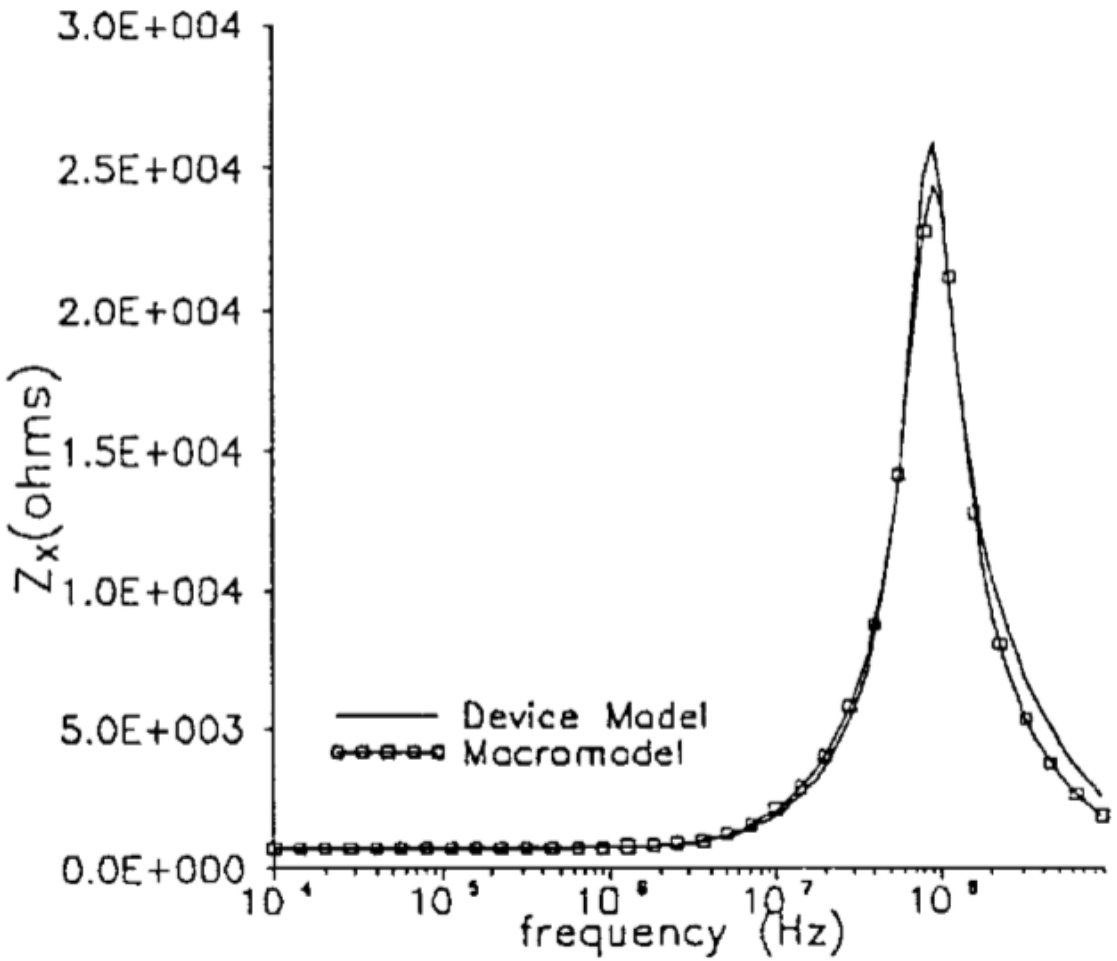


Figure 4. Simulated plots of I_X against V_Y

Macromodels for Current Conveyors

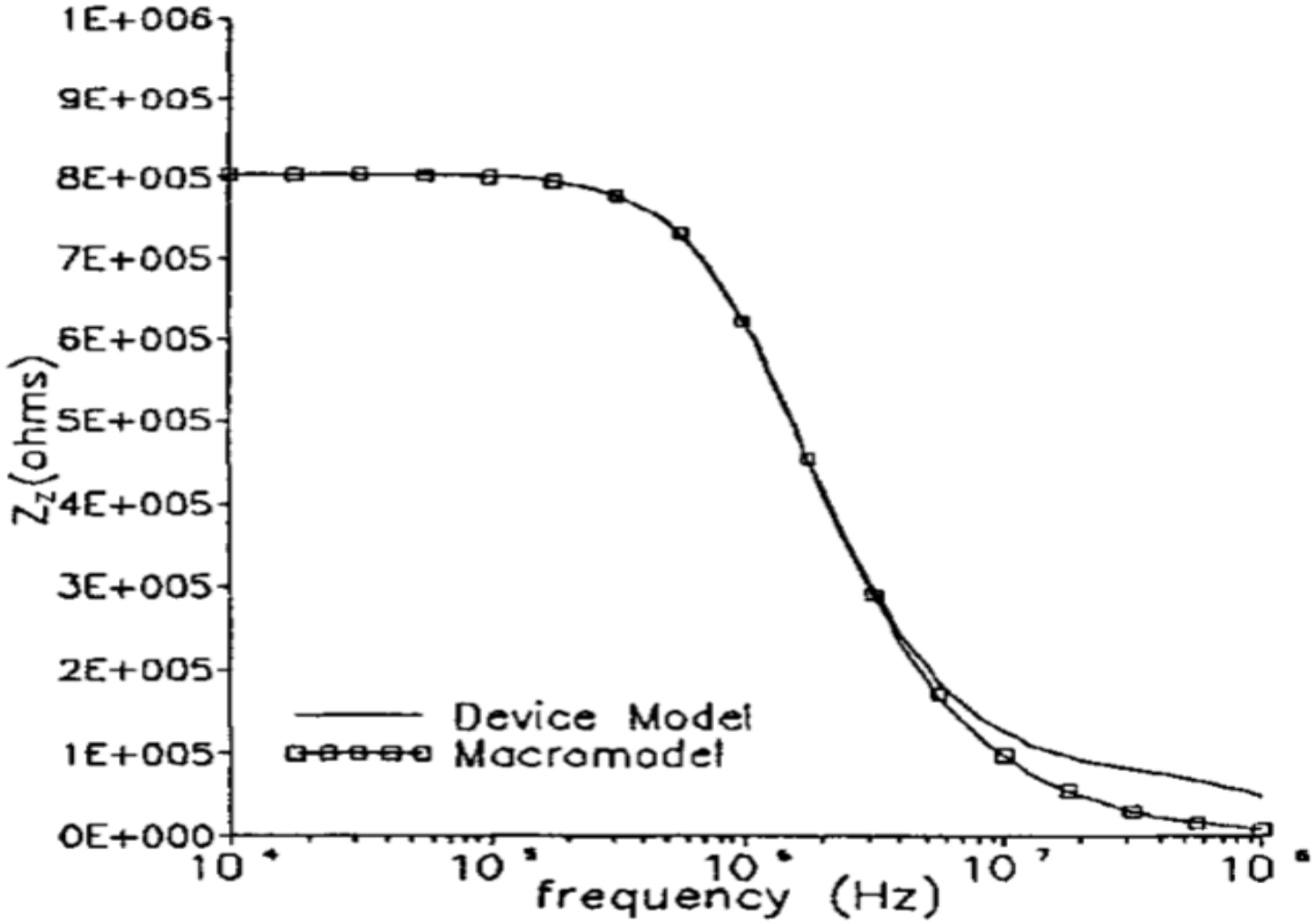


Frequency response of Z_Y



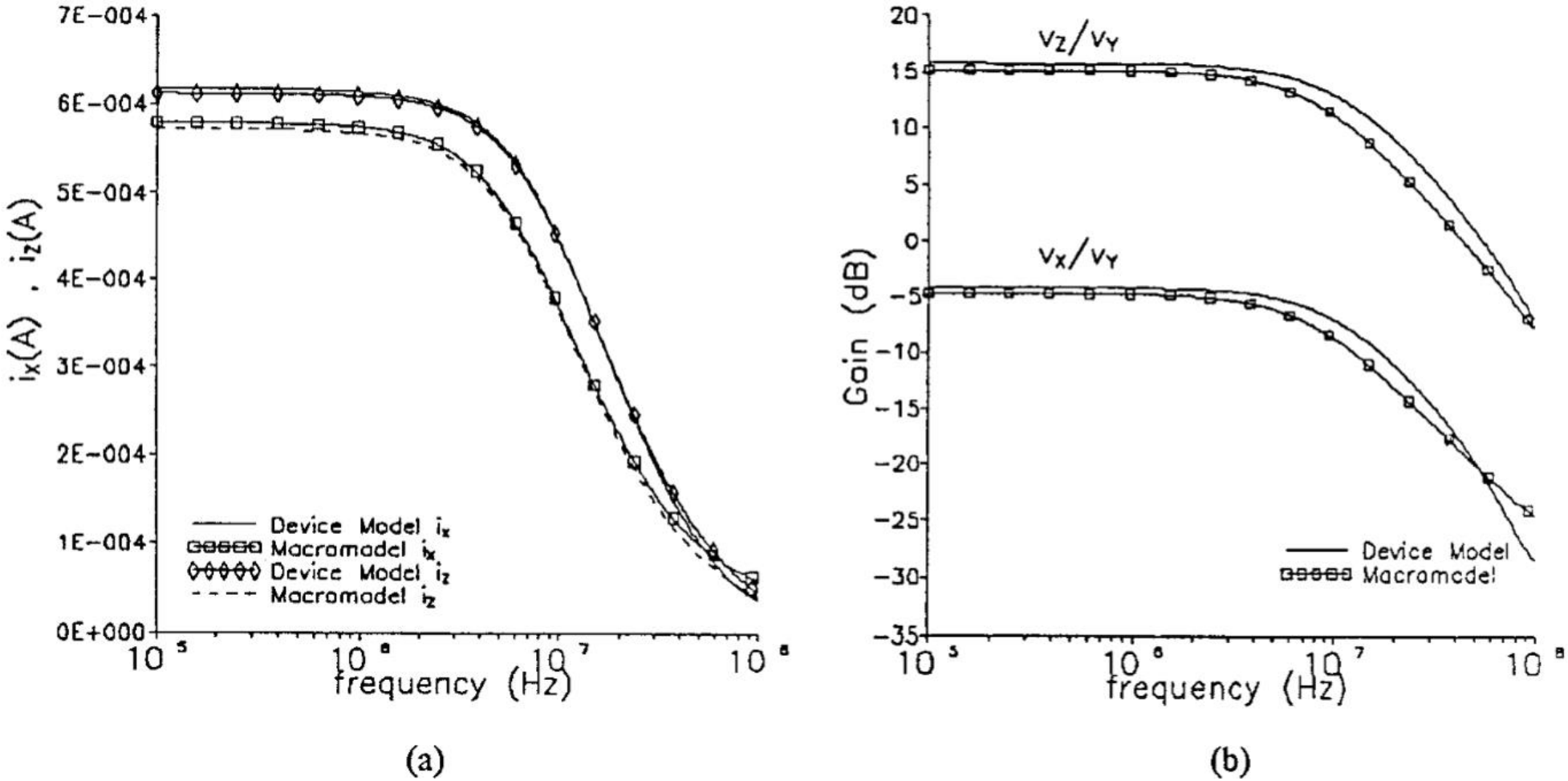
Frequency response of Z_X

Macromodels for Current Conveyors



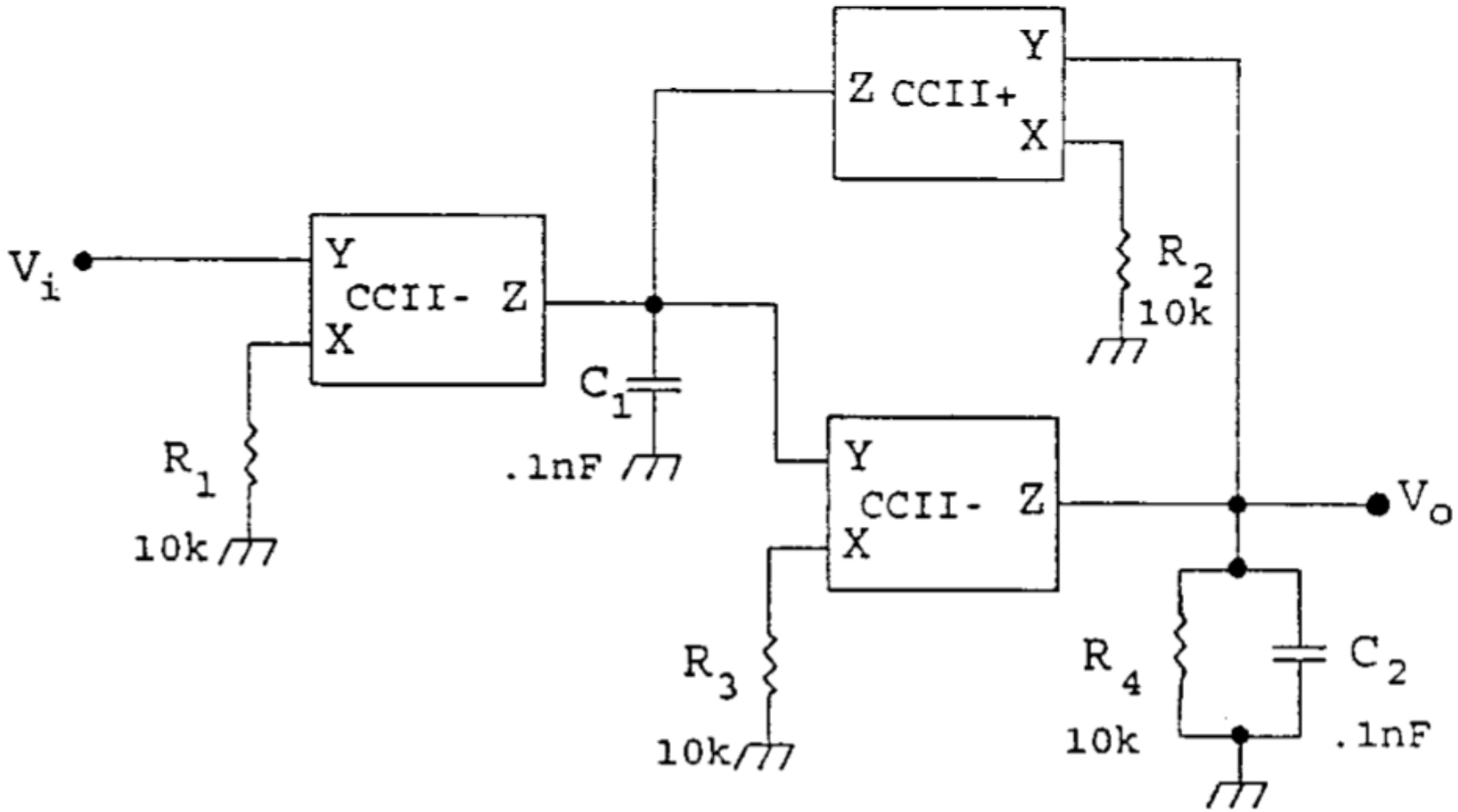
Frequency response of Z_Z

Macromodels for Current Conveyors



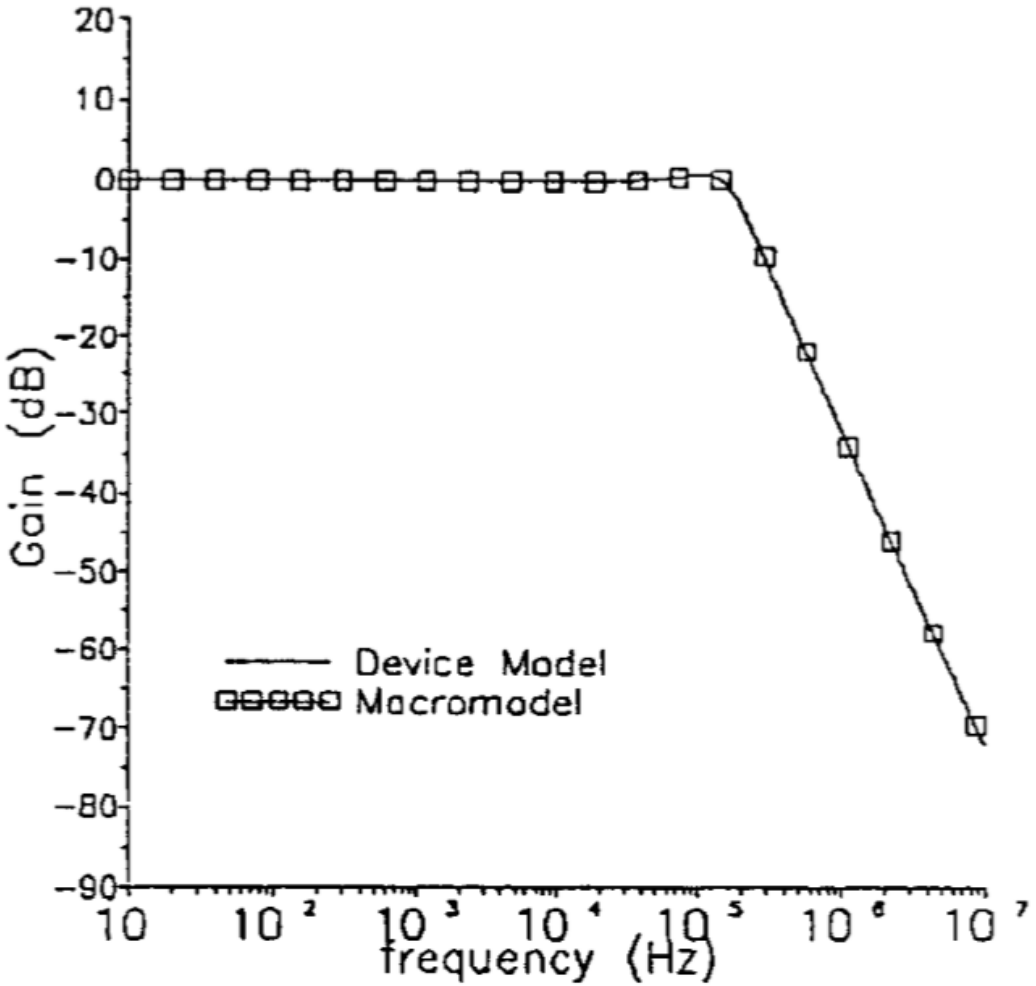
Frequency response of current and voltage gains

Macromodels for Current Conveyors

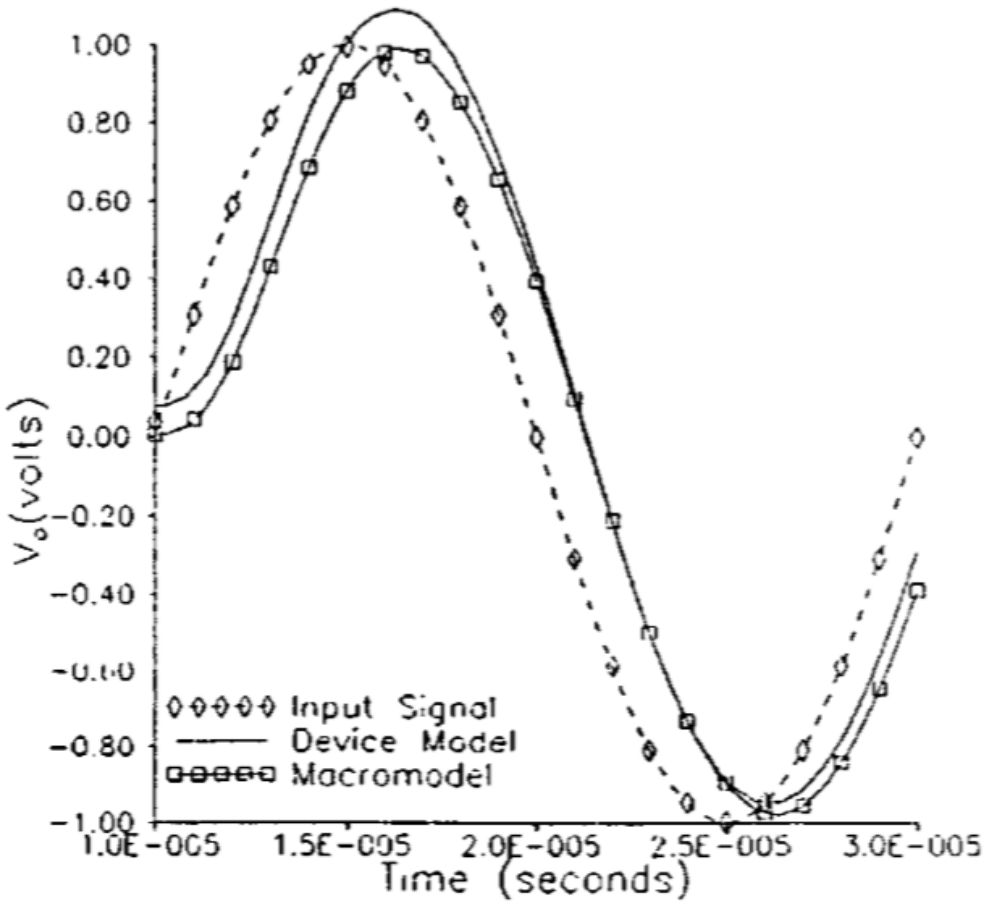


An example of a second-order low-pass active filter

Macromodels for Current Conveyors



(a)



(b)

(a) Simulated frequency response of the filter and (b) transient analysis results of the filter

Macromodels for Current Conveyors

Table IV. Computer times in seconds needed for SPICE simulations

Type of analysis	AC	TRANSIENT
Current Conveyor-1 (Device Model)	20·70	34·99
Current Conveyor-1 (Macromodel)	1·92	6·59
Current Conveyor-2 (Device Model)	60·25	72·18
Current Conveyor-2 (Macromodel)	2·03	6·32

Table V. Equations to calculate the macromodel parameters

$$R_{C1} = \frac{V_{\mathrm{Xmax}} - V_{XM1}}{|I_{\mathrm{Xmax}}|}$$

$$V_{C1} = V_{DD} - V_{XM1} + V_\gamma$$

$$I_{S1} = -I_{\mathrm{Xmax}} \exp(-V_D/V_T)$$

$$R_{E1} = \frac{|V_{\mathrm{Xmin}}| - |V_{XM2}|}{I_{\mathrm{Xmin}}}$$

$$V_{E1} = V_{SS} - |V_{ZM2}| + V_\gamma$$

$$I_{S2} = I_{X\mathrm{min}} \exp(-V_D/V_T)$$

$$R_{C2} = \frac{V_{\mathrm{Zmax}} - V_{ZM1}}{|I_{\mathrm{Zmax}}|}$$

$$V_{C2} = V_{DD} - V_{ZM1} + V_\gamma$$

$$R_{E2} = \frac{|V_{\mathrm{Zmax}}| - |V_{ZM2}|}{|I_{\mathrm{Zmin}}|}$$

$$V_{E2} = V_{SS} - |V_{ZM2}| + V_\gamma$$

$$k_2 = 1 - \frac{V_D}{r_{X1}|I_{\mathrm{Xmax}}|}$$

$$k_3 = 1 - \frac{V_D}{r_{X1} I_{\mathrm{Xmax}}}$$

$$C_Z = \frac{1}{2\pi f_{Z3dB} r_Z}$$

$$L_P = \frac{R_P}{2\pi f_P Q_P}$$

$$Q_P = \frac{f_P}{B}$$

$$C_P = \frac{Q_P}{2\pi f_P R_P}$$

$$C_Y = \frac{1}{2\pi f_{Z3dB} r_Y}$$

Macromodels for Current Conveyors

Basic static model parameters representing the non-linear current conveyor behaviour can be easily determined from dc transfer characteristics $V_X = V_X(V_Y)$, $V_Z = V_Z(V_Y)$, $I_X = I_X(V_Y)$

The model parameters I_{S1}, I_{S2}, k_{11}, k_{12}, k_2, k_3 represent the current limiting behaviour at the X terminal of the current conveyor and can be determined from the measured or simulated $I_X = I_X(V_Y)$ characteristic. The maximum and minimum values of the current I_X are specified as I_{Xmax} and I_{Xmin}. The forward-biasing voltage of the diodes is fixed at a value of $V_D = 0{\cdot}62$ V; the diode currents are assumed to be equal to I_{Xmax} and I_{Xmin}, respectively.

Model parameters V_{C1}, R_{C1}, V_{E1} and R_{E1} are introduced to represent the boundaries of the voltage swing region at the terminal X and can be obtained from the $V_X = V_X(V_Y)$ characteristic. The two boundaries of linear operation are denoted as V_{XM1} and V_{XM2}, while the maximum and minimum values of the voltage V_X are specified as V_{Xmax} and V_{Xmin}.

Macromodels for Current Conveyors

Similarly, model parameters V_{C2}, R_{C2}, V_{E2} and R_{E2} are introduced to represent the boundaries of the voltage swing region at the terminal Z and can be obtained from the $V_Z = V_Z(V_Y)$ characteristic. The boundaries of linear operating region are denoted as V_{ZM1} and V_{ZM2}, while the maximum and minimum values are specified as V_{Zmax} and V_{Zmin}.

The model parameters r_Y, C_Y, r_Z and C_Z represent the input and output impedances of the current conveyor and can be specified from measured or simulated plots of input and output impedances against frequency (Figures 5 and 7). f_{Y3dB} and f_{Z3dB} are cut-off frequencies.

The model parameters r_{X1}, r_{X2}, R_P, L_P and the capacitor C_P can be extracted from measured and simulated plots of the input impedance at the X terminal against frequency. The resonant frequency is denoted by f_P and B represents the 3 dB bandwidth of the frequency response. As shown in Figure 6, at low frequencies the impedance is resistive and has a value of $R_P//r_X$ where $r_X = r_{X1} + r_{X2}$. At resonant frequency the impedance becomes $Z_X = r_X + R_P = \omega_P Q_P L_P$. The fraction ratio of r_{X1}/r_{X2} has no physical meaning and can be taken as $r_{X1}/r_{X2} = 1$ for simplicity, though it is a well known technique in the modelling of current limiting.[1–3]

Macromodel for four-terminal floating nullors (FTFNs)

Simple and accurate nonlinear macromodel for four-terminal floating nullors (FTFNs)

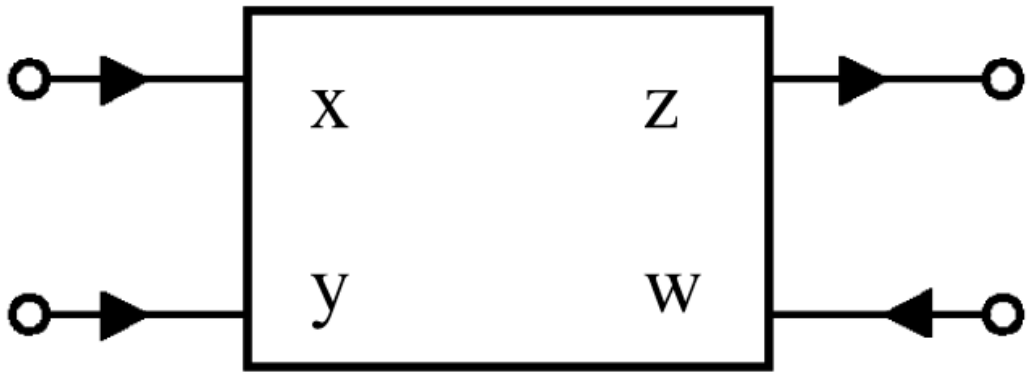
Ugur Çam & Hakan Kuntman

INT. J. ELECTRONICS, 2001, VOL. 88, NO. 4, 435- 447

Macromodel for four-terminal floating nullors (FTFNs)

- The four-terminal foating nullor (FTFN) has also been receiving considerable attention recently
- A very flexible and versatile building block in active network synthesis.
- The FTFN contains both a floating voltage follower and a current follower without having any common node,
- makes it easy to synthesize current and voltage-mode analogue signal processing circuits

Macromodel for four-terminal floating nullors (FTFNs)



Circuit symbol of the FTFN.

Macromodel for four-terminal floating nullors (FTFNs)

ideal FTFN is characterized by the following port relations

$$\left.\begin{aligned} V_x &= V_y \\ I_x &= I_y = 0 \\ I_z &= I_w \end{aligned}\right\} \tag{1}$$

Taking into consideration the FTFN non-idealities, the port relations in equation (1) can be expressed as follows

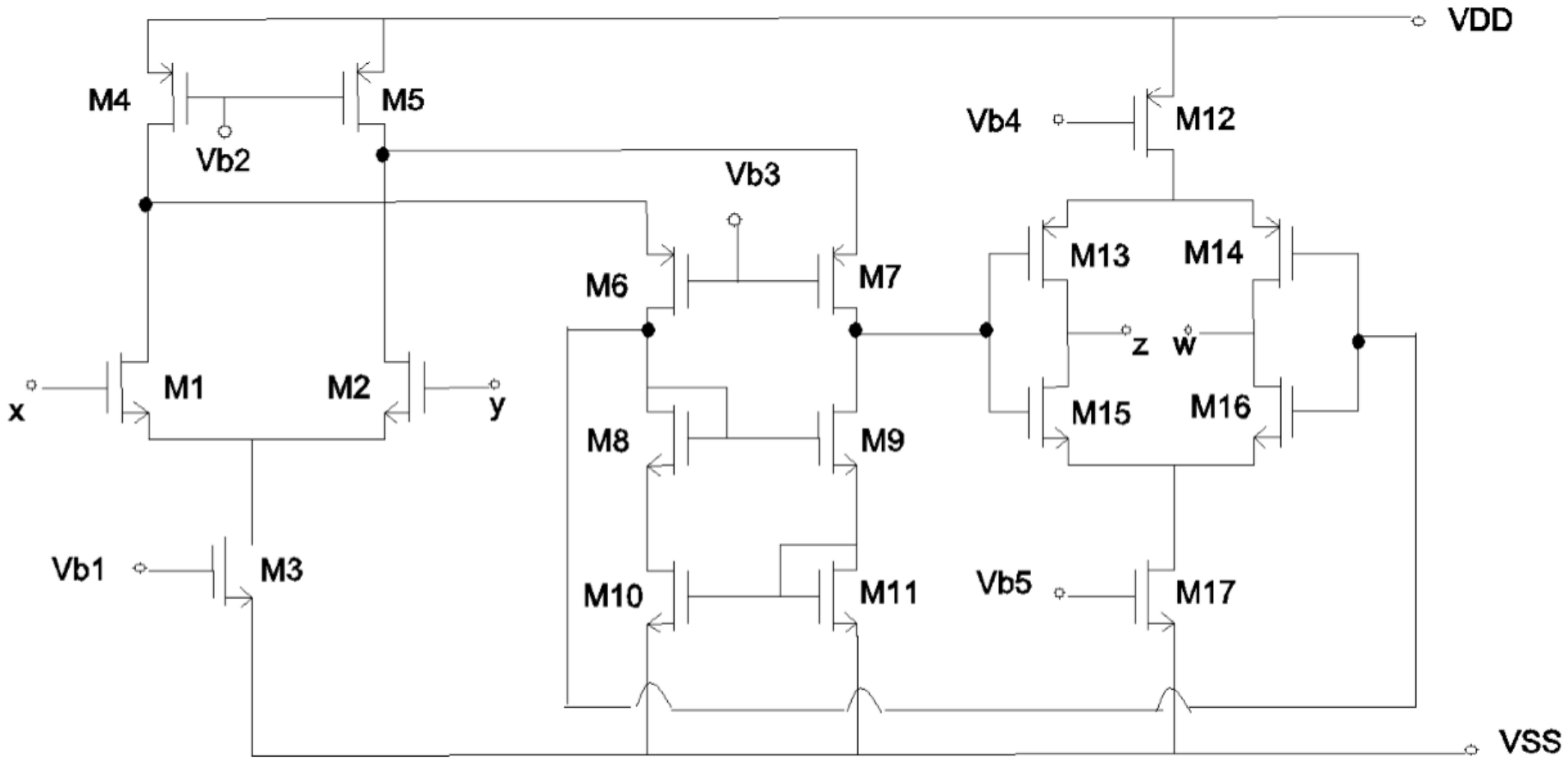
$$\left.\begin{aligned} V_x &= \beta V_y \\ I_z &= \alpha I_w \end{aligned}\right\} \tag{2}$$

where $\beta = 1 - \varepsilon_v$, where ε_v denotes voltage tracking error, and $\alpha = 1 - \varepsilon_i$, where ε_i denotes current tracking error of the FTFN.

Macromodel for four-terminal floating nullors (FTFNs)

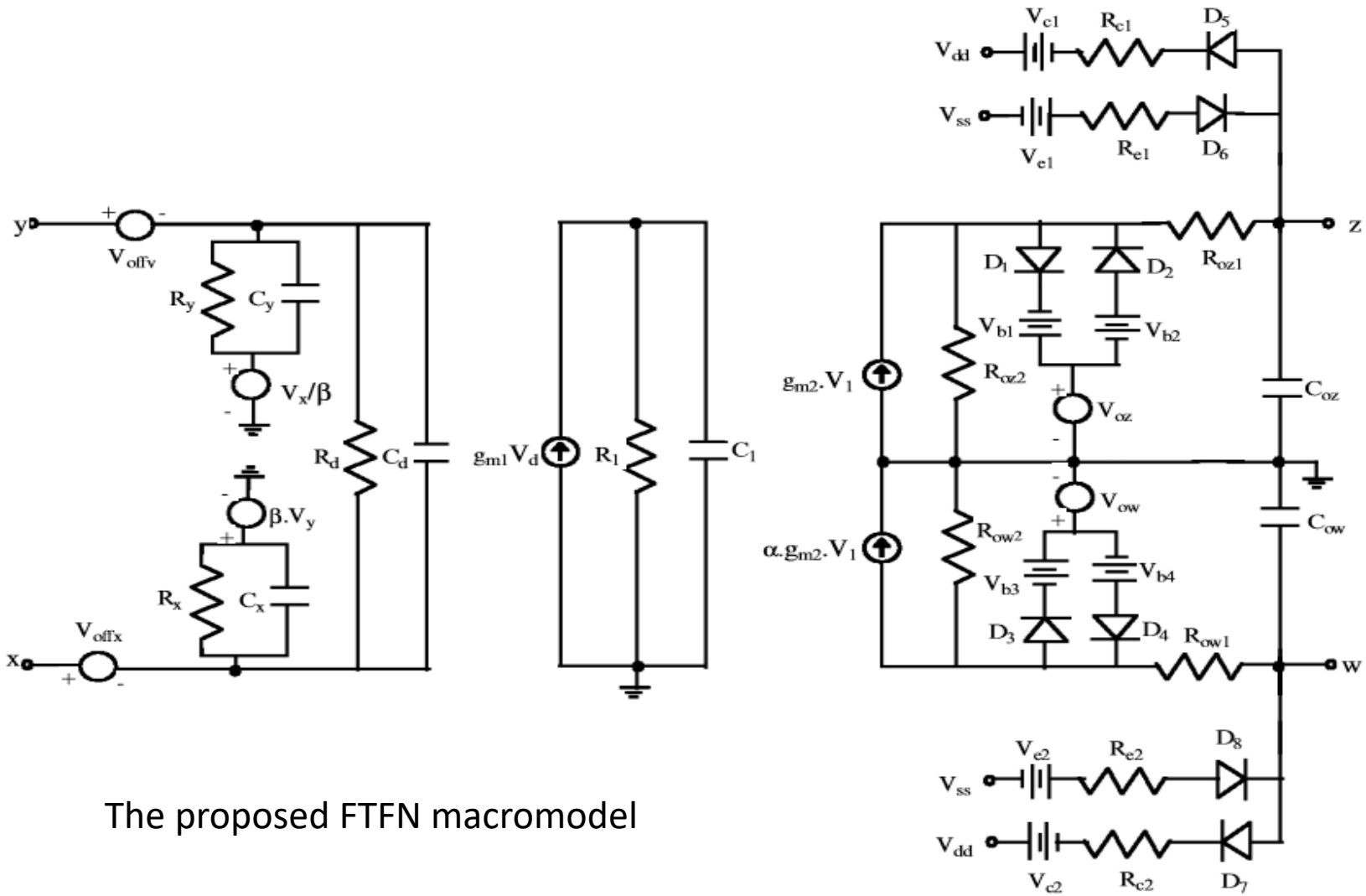
The FTFN is ideally a transconductance amplifier featuring infinite gain and two output currents. The basic equation describing its operation $I_w = I_z = G_m (V_x - V_y)$. For a finite open-loop transconductance gain G_m, the difference between two differential voltages increases as G_m decreases. Therefore the open-loop transconductance gain should be as large as possible to achieve high performance operation.

Macromodel for four-terminal floating nullors (FTFNs)



Circuit schematic diagram of the CMOS FTFN.

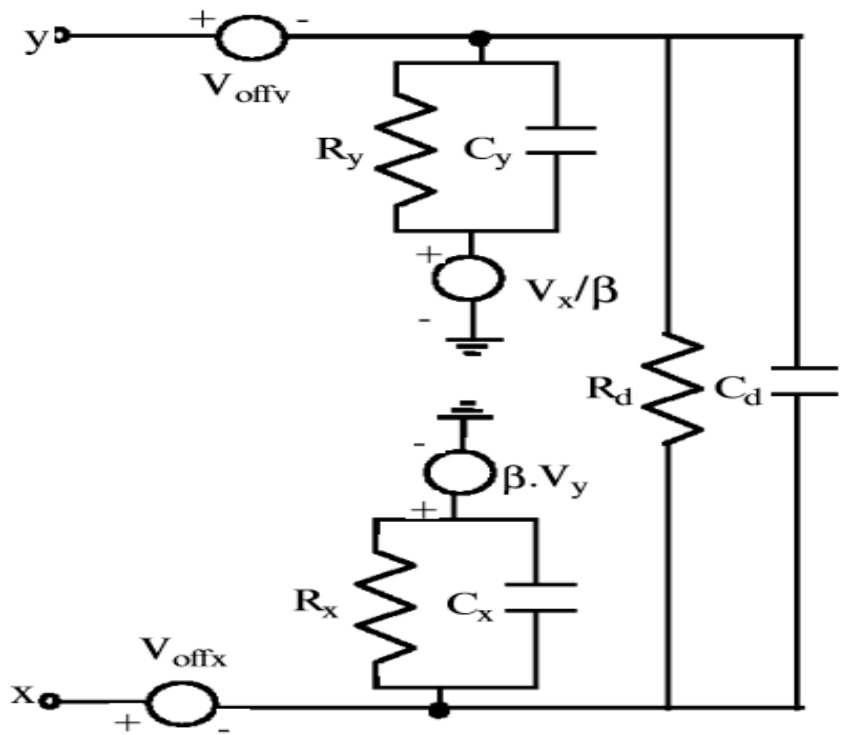
Macromodel for four-terminal floating nullors (FTFNs)



The proposed FTFN macromodel

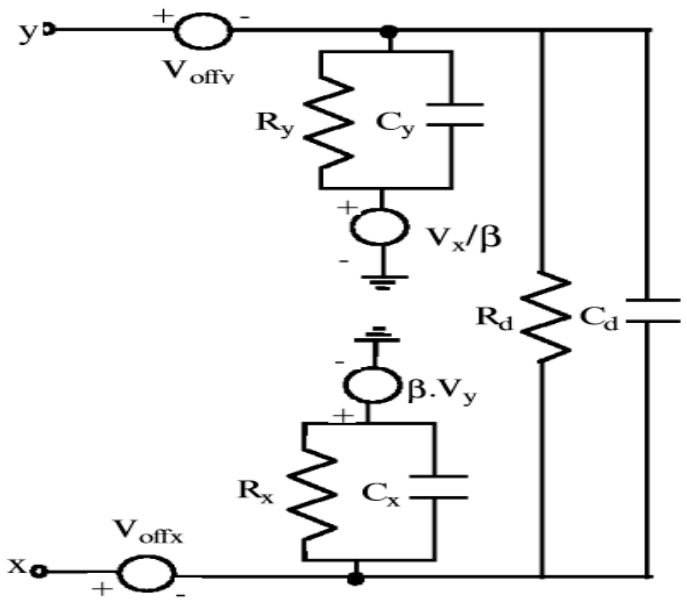
Macromodel for four-terminal floating nullors (FTFNs)

The input stage produces the necessary linear and nonlinear differential mode input characteristics and consists of capacitors C_x, C_y, C_d, resistors R_x, R_y, R_d, independent voltage source V_{os} and voltage-controlled voltage sources V_x, V_y.



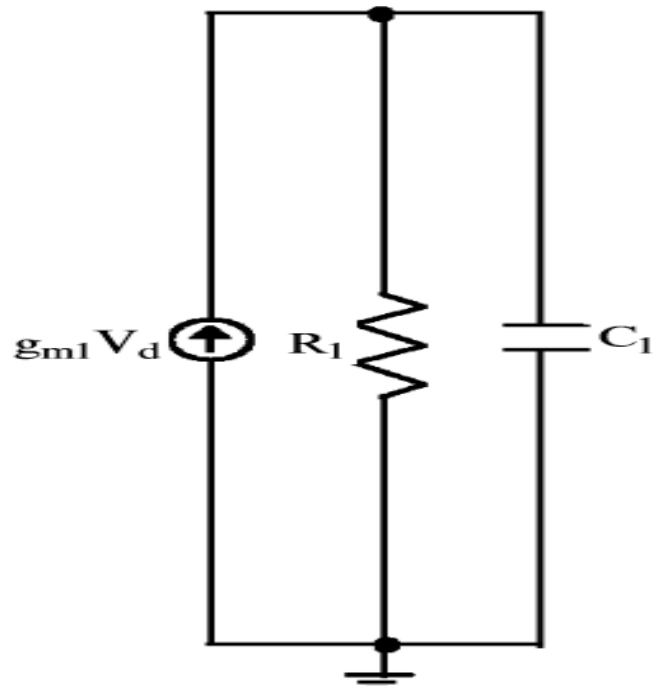
Macromodel for four-terminal floating nullors (FTFNs)

voltage source V_{os} is introduced to model the input voltage offset voltage. V_x and V_y are dependent voltage sources which represent voltage tracking error of the FTFN. C_x, C_y, C_d and R_x, R_y, R_d represent input capacitances and resistances of the FTFN respectively. Since the input resistance of the FTFN can be assumed practically infinite, R_x, R_y and R_d are fixed at $10^{12}\,\Omega$ to prevent numerical problems



Macromodel for four-terminal floating nullors (FTFNs)

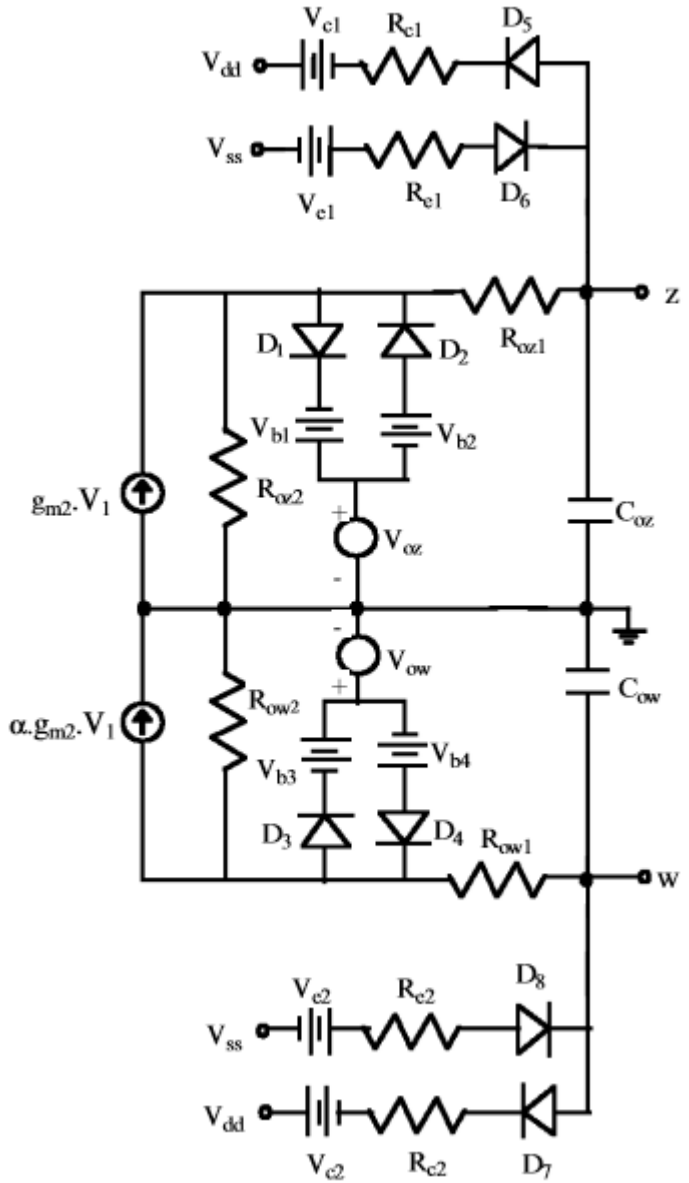
The inter-stage contains a unity gain connection and is introduced to provide a high-frequency dominant pole. To introduce this pole into the frequency response the resistance R_1 is chosen as $1/g_{m1}$.



Macromodel for four-terminal floating nullors (FTFNs)

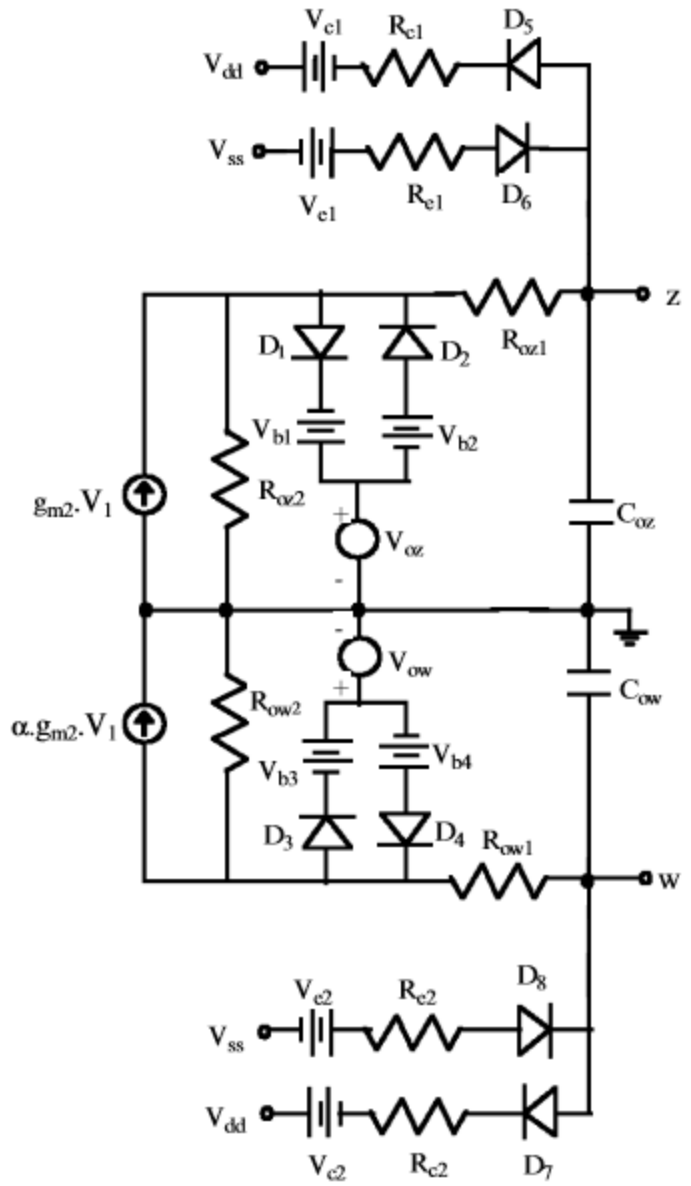
The output stage consists of two current controlled current sources, output capacitances and output resistances.

The transconductance ratio of the current-controlled current source represents the current tracking error of the FTFN.



Macromodel for four-terminal floating nullors (FTFNs)

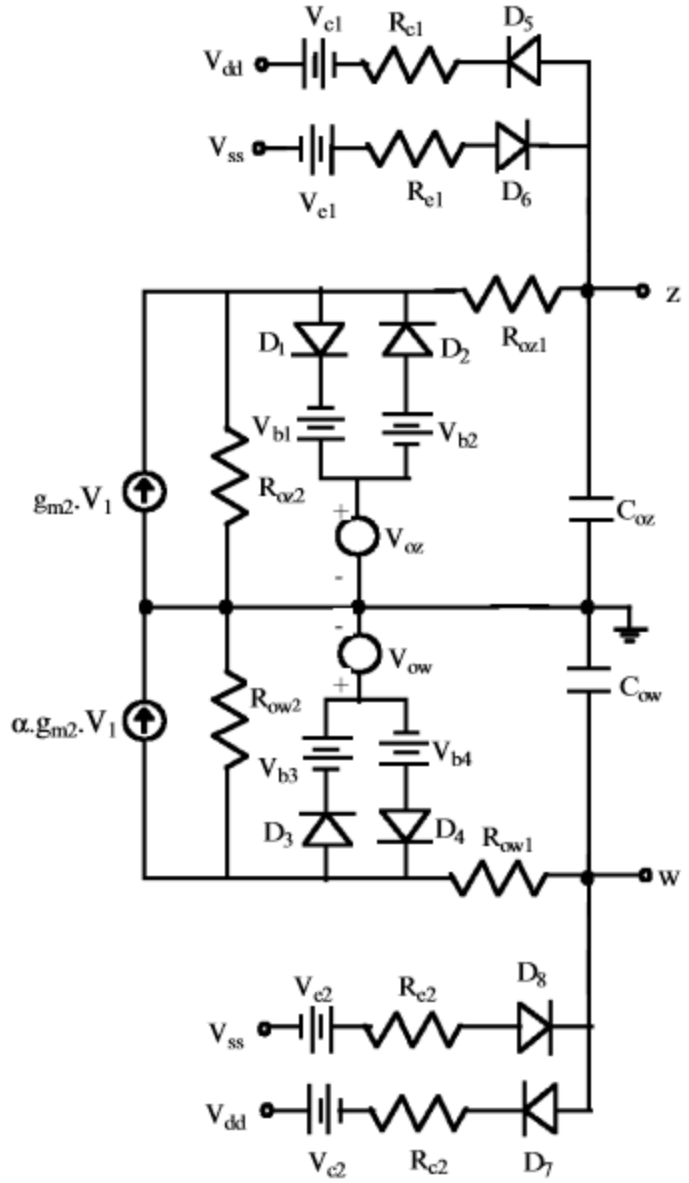
The nonlinearity of the FTFN caused by voltage and current limiting at the z and w terminals modelled a well-known modelling technique, namely piecewise linear approximation, by introducing additional elements.



Macromodel for four-terminal floating nullors (FTFNs)

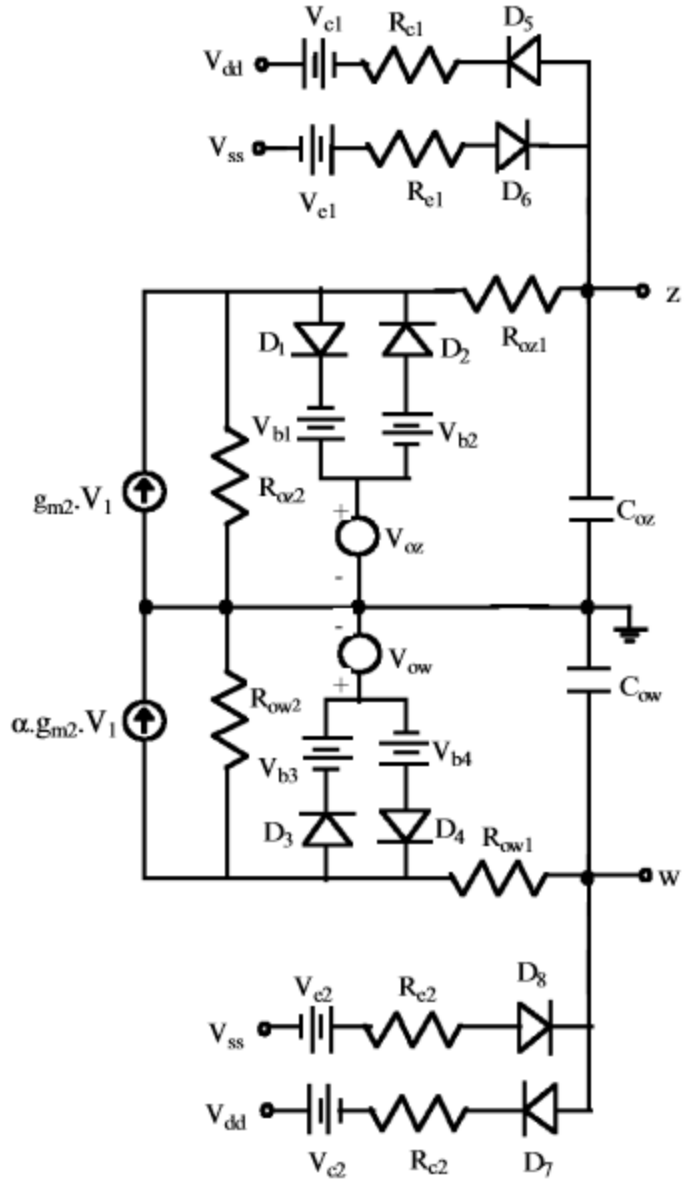
The voltage swings at the z and w terminals are limited by voltage source-resistor-diode combinations Vc1, D5, Rc1 Ve1, D6, Re1 and Vc2, D7, Rc2, Ve2, D8, Re2.

To represent current-limiting voltage-dependent voltage source-diode-voltage source combinations Vz, Vb1, Vb2, D1, D2 and Vw, Vb3, Vb4, D3, D4 are incorporated into the circuit.



Macromodel for four-terminal floating nullors (FTFNs)

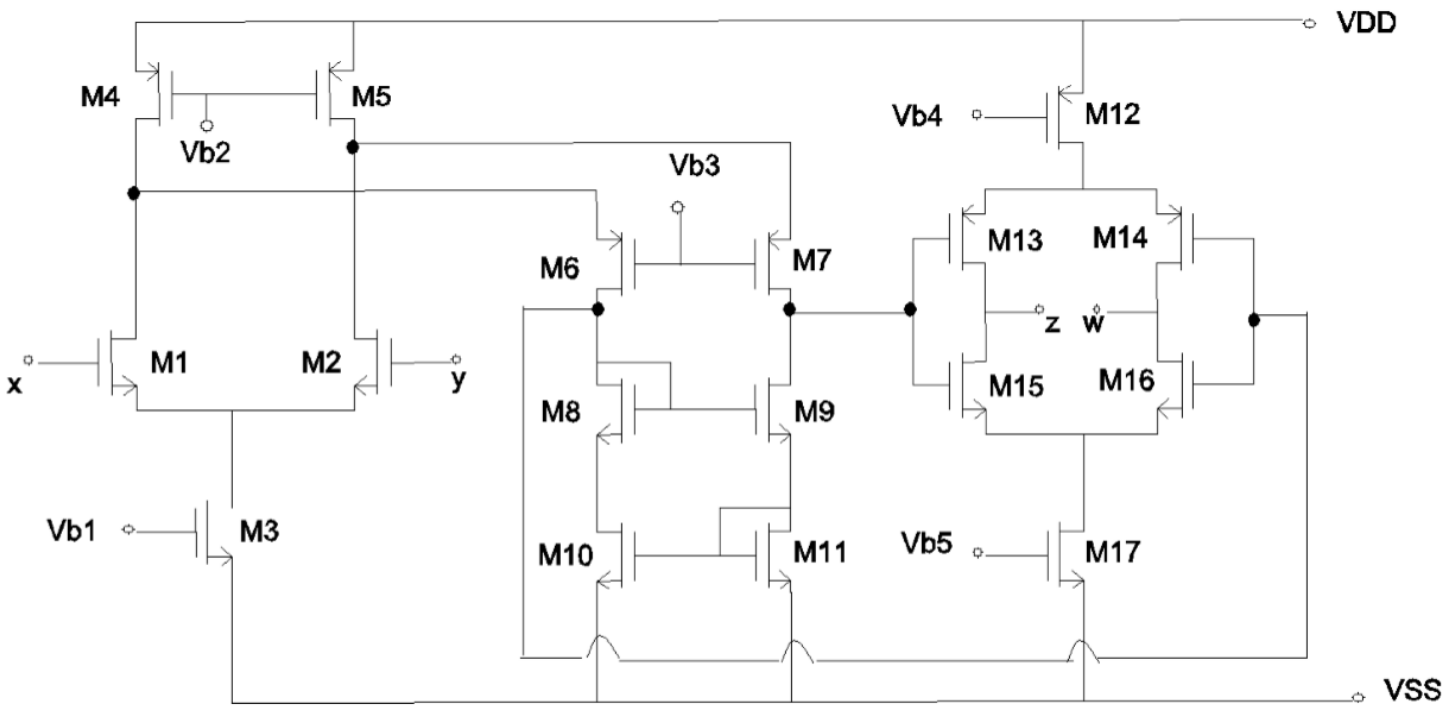
The resistors Rc1, Re1, Rc2 and Re2 are resistive elements introduced into the circuit model which adjust the slope of the dc voltage transfer characteristic at the boundaries of the linear operation region.



Macromodel for four-terminal floating nullors (FTFNs)

Comparison with semiconductor device models

Transistor	W (μm)	L (μm)
M1	24	3
M2	24	3
M3	100	3
M4	100	3
M5	100	3
M6	100	3
M7	100	3
M8	100	3
M9	100	3
M10	100	3
M11	100	3
M12	300	3
M13	100	3
M14	100	3
M15	100	3
M16	100	3
M17	300	3



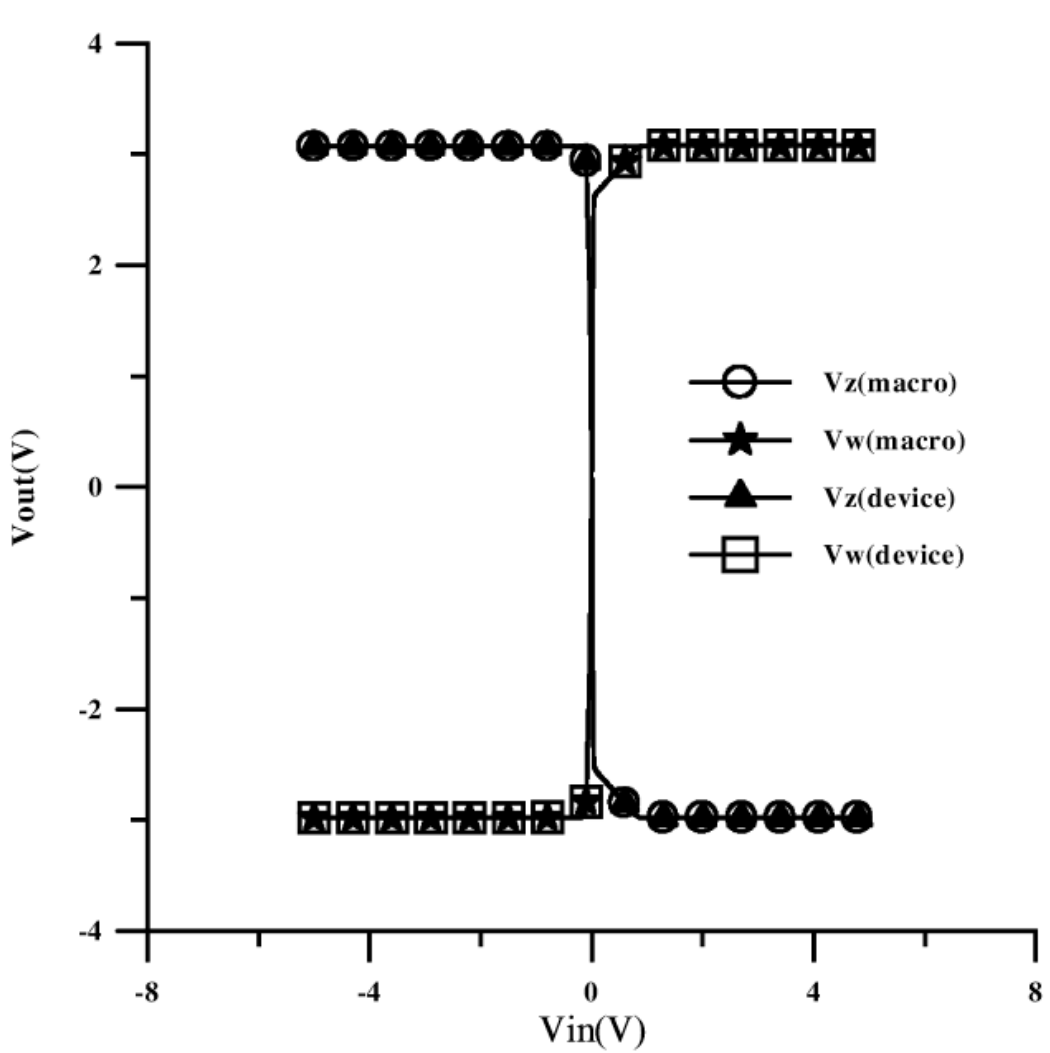
Macromodel for four-terminal floating nullors (FTFNs)

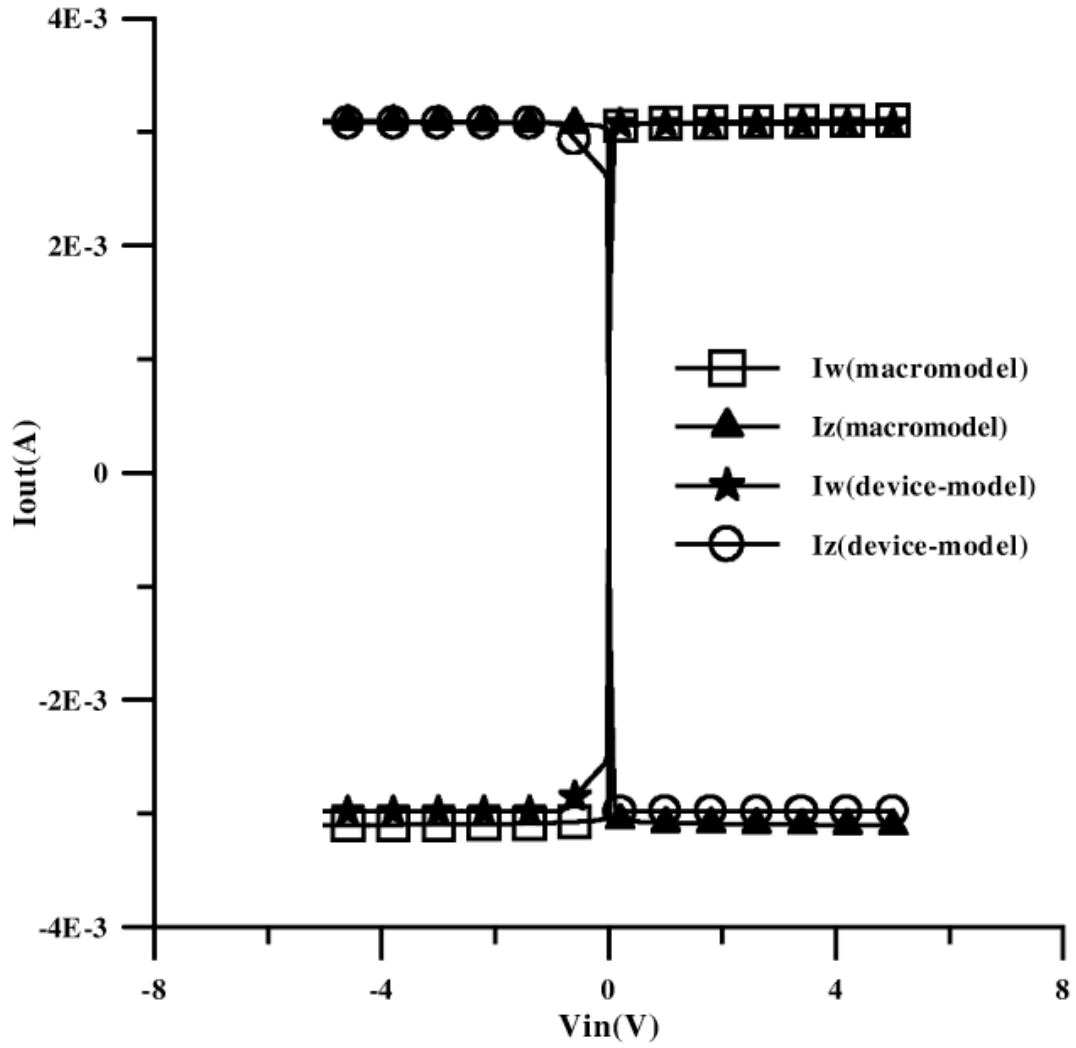
Comparison with semiconductor device models

Parameter	Value	Parameter	Value	Parameter	Value
V_{offx}	1 mV	β	1	R_{c1}	1 kΩ
V_{offy}	1 mV	R_1	1 Ω	R_{c2}	1 kΩ
V_{b1}	5.6 V	C_1	100 pF	R_{e1}	1 kΩ
V_{b2}	5.6 V	R_d	10^{12}Ω	R_{e2}	1 kΩ
V_{b3}	5.6 V	C_d	1 pF	g_{m1}	1 A V^{-1}
V_{b4}	5.6 V	R_x	10^{12}Ω	g_{m2}	180 mA V^{-1}
V_{c1}	1.2 V	C_x	1 pF	R_{oz1}	18 kΩ
V_{c2}	1.2 V	R_y	10^{12}Ω	R_{oz2}	2 kΩ
V_{e1}	1.6 V	C_y	1 pF	R_{ow1}	18 kΩ
V_{e2}	1.6 V	C_{oz}	0.1 pF	R_{ow2}	2 kΩ
α	1	C_{ow}	0.1 pF		

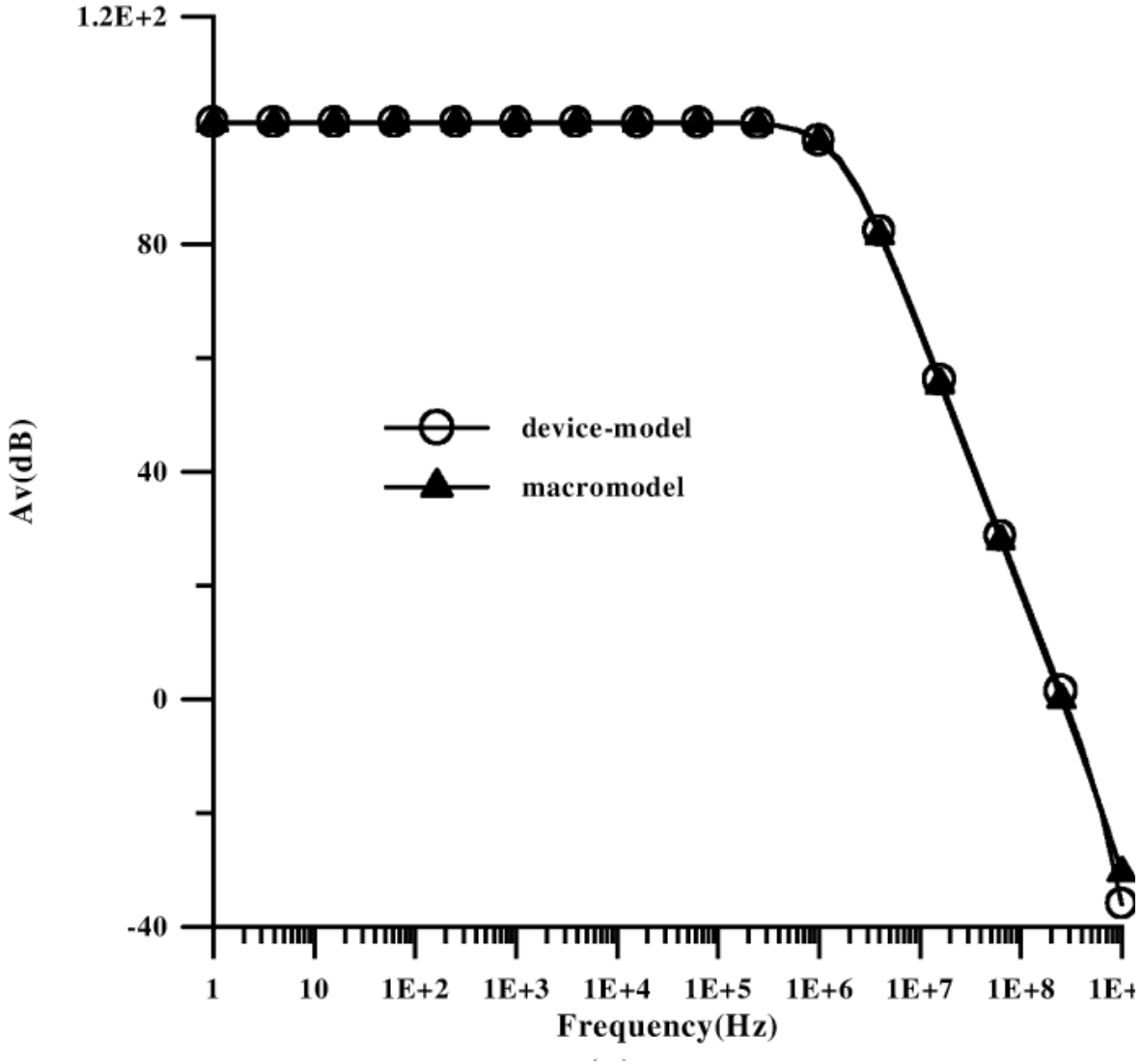
Model parameters of the derived FTFN macromodel.

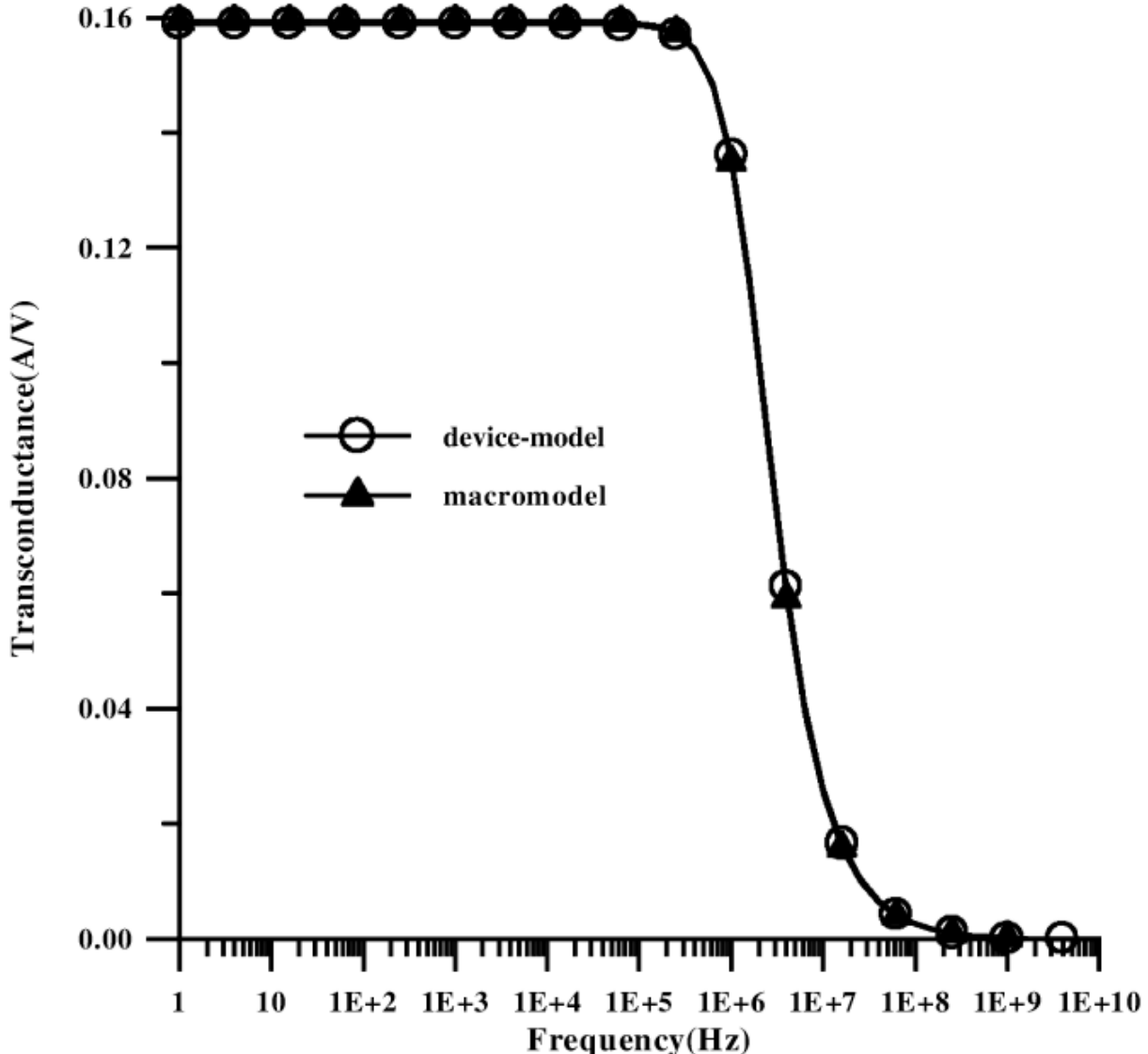
Macromodel for four-terminal floating nullors (FTFNs)





Macromodel for four-terminal floating nullors (FTFNs)





Macromodel for four-terminal floating nullors (FTFNs)

Comparison with semiconductor device models

	Relative error (% ε)
dc current curves	2.2
dc voltage cuves	2.4
Gain–frequency curve	1.01
Transconductance–frequency curve	0.5
Filter ac response	1.4

Relative errors between device model and macro-model for SPICE simulations.

Macromodel for four-terminal floating nullors (FTFNs)

Parameter Extraction

Macromodel for four-terminal floating nullors (FTFNs)

$$V_{b1} = -I_{oz\,max}R_{Oz1} - V_D$$

$$V_{b2} = -I_{oz\,min}R_{oz1} - V_D$$

$$V_{b3} = -I_{ow\,max}R_{ow1} - V_D$$

$$V_{b4} = -I_{ow\,min}R_{ow1} - V_D$$

$$I_{s1} = I_{oz\,max}\exp\left[-\frac{V_D}{V_T}\right]$$

$$I_{s2} = I_{oz\,min}\exp\left[-\frac{V_D}{V_T}\right]$$

$$I_{s3} = I_{ow\,max}\exp\left[-\frac{V_D}{V_T}\right]$$

$$I_{s4} = I_{ow\,min}\exp\left[-\frac{V_D}{V_T}\right]$$

$$R_{c1} = \frac{V_{oz\,max} - V_{om1}}{I_{oz\,max}}$$

$$R_{e1} = \frac{V_{oz\,min} - |V_{om2}|}{I_{oz\,min}}$$

$$R_{c2} = \frac{V_{ow\,max} - V_{om3}}{I_{ow\,max}}$$

$$R_{e2} = \frac{V_{ow\,min} - |V_{om1}|}{I_{ow\,min}}$$

$$V_{c1} = V_{dd} - V_{om1} - V_\gamma$$

$$V_{e1} = V_{ss} - |V_{om2}| + V_\gamma$$

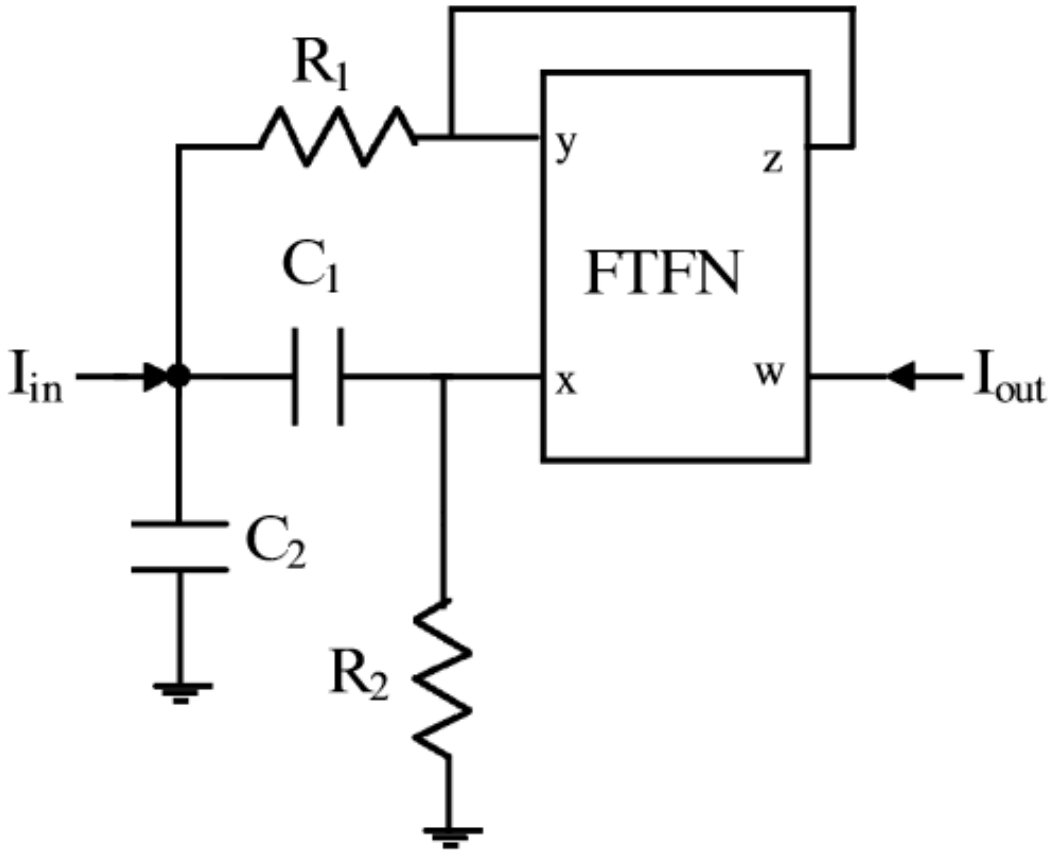
$$V_{c2} = V_{dd} - V_{om3} - V_\gamma$$

$$V_{e2} = V_{ss} - |V_{om4}| + V_\gamma$$

Equations to calculate the model parameters.

Macromodel for four-terminal floating nullors (FTFNs)

Application Example:
Second-order current-mode low-pass filter prototype for constructing a sixth-order current-mode low-pass filter.



Macromodel for four-terminal floating nullors (FTFNs)

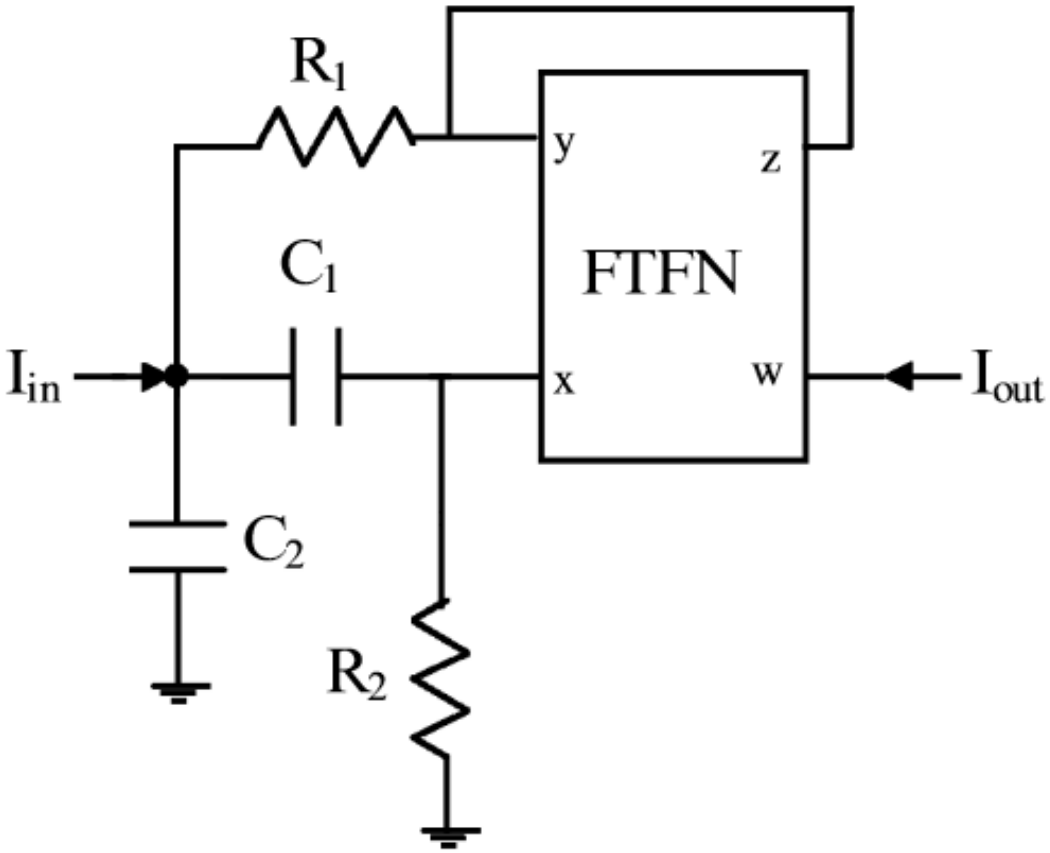
The filter topology was constructed by cascading three second-order current-mode lowpass filters

The normalized transfer function of the Butterworth filter is given as

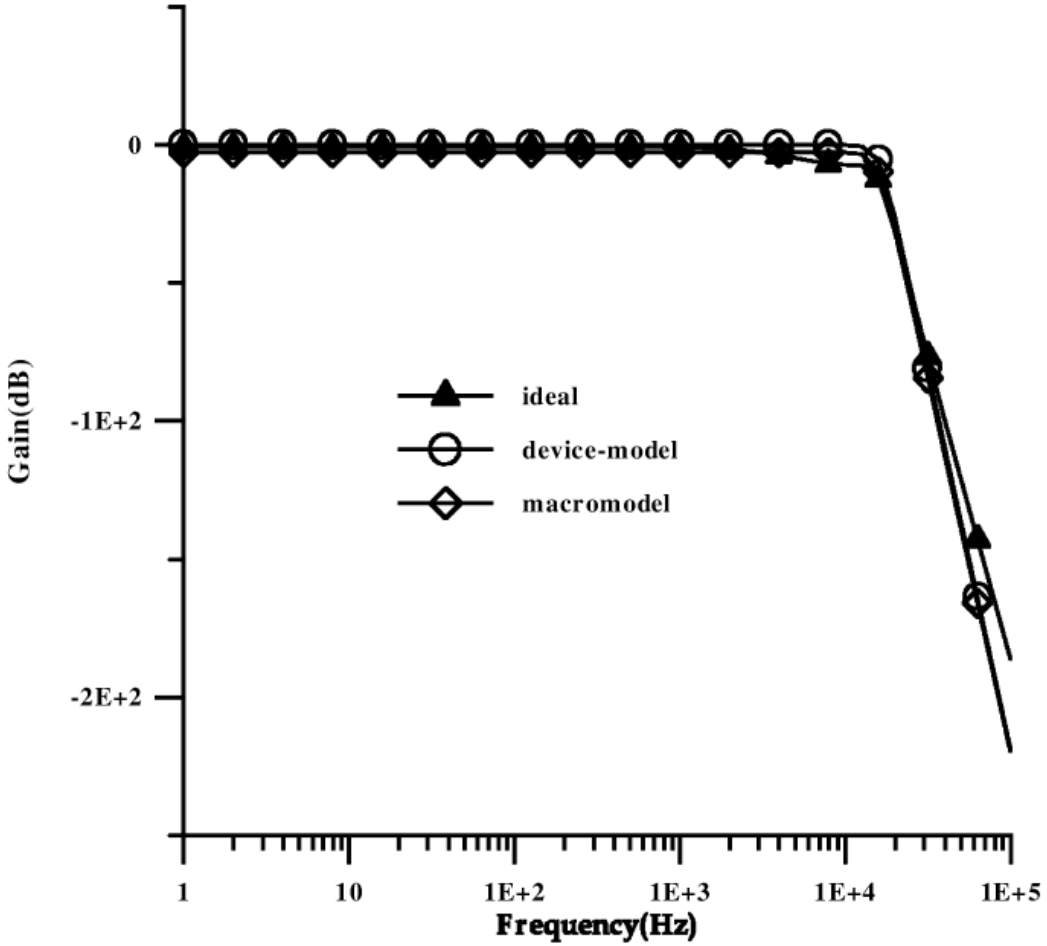
$$\frac{I_{out}}{I_{in}} = \frac{1}{(s^2 + 0.518s + 1)} \frac{1}{(s^2 + \sqrt{2}s + 1)} \frac{1}{(s^2 + 1.932s + 1)}$$

Macromodel for four-terminal floating nullors (FTFNs)

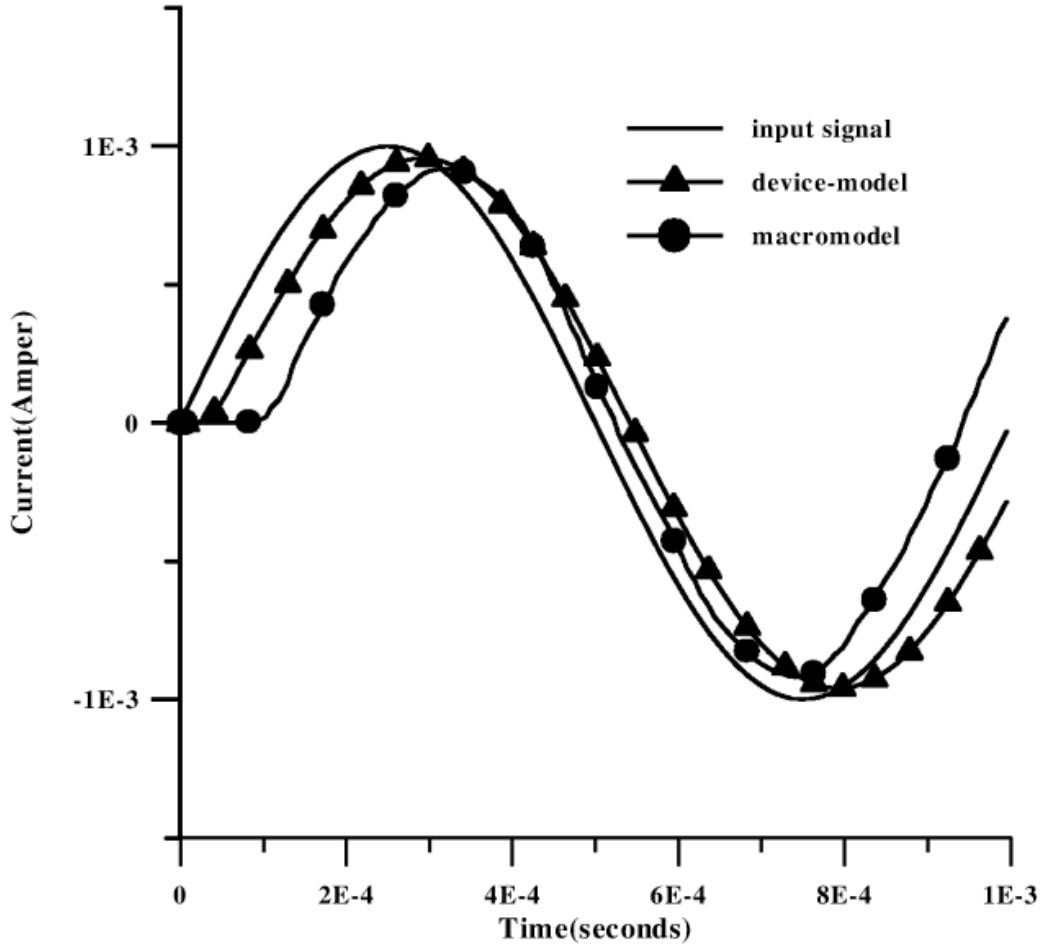
Passive components were chosen as C1 = C2 = 10nF, R1 = 0,259kΩ, R2 = 3,861 kΩ for the ® first stage, C1= C2 = 10nF, R1 = 0,709 k Ω, R2 = 1:41 Ω for the second stage and C1 = C2 = 10nF, R1 = 0:966 k Ω, R2 = 1:037k Ω for the third stage, which result in 15.9kHz cut-off frequency.



Macromodel for four-terminal floating nullors (FTFNs)



Frequency response of the sixth-order low-pass Butterworth filter.



Transient analysis result of the filter with 1kHz sine-wave input voltage.

Macromodel for four-terminal floating nullors (FTFNs)

Analysis type	ac (s)	Transient (s)
Macromodel	2.69	2.75
Device model	10.32	16.42

Computer times needed for SPICE simulations.

Macromodel for four-terminal floating nullors (FTFNs)

- The most important result obtained in the context of this work is the combination of accurate modelling with reduced computer time,
- providing the IC designer with the possibility of speeding up the simulation of large electronic systems in VLSI systems that contain circuits such as active filters and oscillators constructed with FTFNs.

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