isoelectric segments, modified signal averaging performs better than classical averaging, but it compromises the MSE in the VLP segment, due to an additional lowpass filtering effect and smearing in the time domain. Results would be better if no beat-to-beat VLP variability were present. In this case, the MSE in VLP segments would be drastically reduced by more than 20 times with respect to that of **y**.

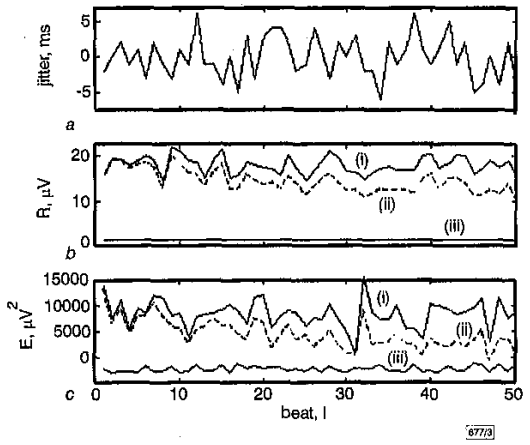

Fig. 3 *VLP jitter, RMS noise and MSE computed for* **y**, **a** *and* **e** *signals*

a VLP jitter
b RMS noise
c MSE
(i) **y** signal
(ii) **a** signal
(iii) **e** signal

This system performs well with only 1 min of HR-ECG signals. Standards for the analysis of VLP [1, 6] can be applied to a single beat from **e** and the results coincide with those using ideal signal **x**.

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A. Taboada-Crispi and J.V. Lorenzo-Ginori (*Electrical Engineering Faculty, Universidad de Las Villas, 54830 Santa Clara, Villa Clara, Cuba*)

D.F. Lovely (*Institute of Biomedical Engineering, University of New Brunswick, PO Box 4400, Dineen Drive, Fredericton, NB, E3B 5A3, Canada*)

D.F. Lovely: Corresponding author

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High-output-impedance CMOS dual-output OTA suitable for wide-range continuous-time filtering applications

A. Zeki and H. Kuntman

A high-output-impedance precision current mirror is implemented in a CMOS dual-output OTA (DOTA) structure by means of an efficient implementation method, which is also applicable to other current-output-based active devices. The new DOTA, when used in a DOTA-C integrator, enables integration at very low frequencies, with a capacitor on the order of several picofarads.

Introduction: The use of current-output-based active devices (COBADs), such as OTAs, current conveyors, etc. in continuous-time filter design, has been attracting a large amount of interest, especially because of their wider bandwidths with respect to those of equivalent opamps. An important drawback of COBAD-based continuous-time filters is the finite output resistance (R_{out}) of a COBAD, which, in a basic integrator structure, is in parallel with the load capacitor C_L, causing a lossy integration, thus generating filtering errors [1]. Classical cascode current output stages cannot handle a load capacitor of the order of several picofarads at low frequencies (e.g. for $f < 1$kHz); therefore integration cannot be performed beyond this limit [2]. Choosing large C_L values (e.g. several nanofarads) is not a reasonable solution, since this requires very large areas on a chip. Therefore, very high output impedance current output stages are required, both to enable filtering at low frequencies and to reduce filtering errors.

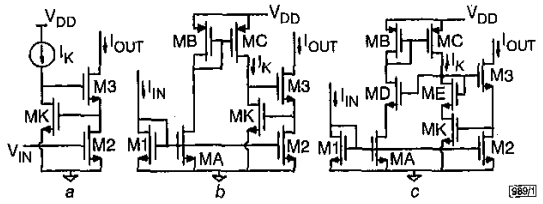

Fig. 1 *Active-feedback cascode structures*

a RGC stage
b Active-feedback cascode CM
c Improved active-feedback cascode CM

Precision current mirrors with very high R_{out}: The regulated cascode (RGC) stage [3] (Fig. 1*a*) achieves a very high output impedance with the aid of active negative feedback through amplifier MK-I_K and source follower M3. The current mirror (CM) in Fig. 1*b* employs the RGC stage to achieve a very large R_{out} [4]. Precision is maintained by making I_K dependent on I_{IN}, to achieve $V_{GSK} = V_{GS1}$ equality (thus, $V_{DS2} = V_{DS1}$ equality), for any input current level. To save power and area, MA and MK can be relatively smaller than M1, i.e. $(W/L)_A = (W/L)_K = (W/L)_1/\kappa$, where $\kappa > 1$ [4]. Then, matching MB and MC will be sufficient to achieve the $I_K = I_{IN}/\kappa$ equality satisfactorily. Further precision improvements can be maintained by choosing long channel lengths for MB and MC; and, as in the CM of Fig. 1*c*, by using additional devices (MD and ME) to maintain $V_{DSA} = V_{DSK} = V_{DS1}$ [5].

Proposed DOTA structure: In fully-differential structures, better PSRR, CMRR, distortion and input/output swing performances are achieved with respect to those of single-ended structures [6]. Also fewer active devices are required in a filter or oscillator. It is possible to efficiently implement the active-feedback CMs of Fig. 1 into a differential-output COBAD (e.g. a DOTA or a dual-output current conveyor), enabling further reduction of excess power and area consumption. The incorporation of the CM of Fig. 1*b* into a DOTA structure is described below. The method is also valid for the CM of Fig. 1*c* and can be applied to other differential-output COBADs.

Since inverted and non-inverted copies of output-stage currents are conveyed both by PMOS and NMOS CMs in a DOTA (or in a differential-output COBAD) the dependent I_K current of each active-feedback CM can be obtained easily, simply by connecting a single transistor (MC) in parallel, to copy this current. Thus, MA and MB are eliminated, reducing the consumed power and

chip area, as well as parasitics. The resulting circuit is given in Fig. 2. It is worth mentioning that the new circuit does not need any additional biasing for the cascode stages. Actually, an 'adaptive biasing' is performed by the active feedback within each RGC stage.

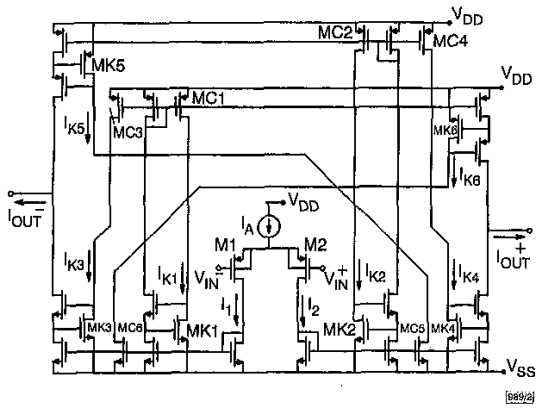

Fig. 2 *Proposed CMOS DOTA structure*

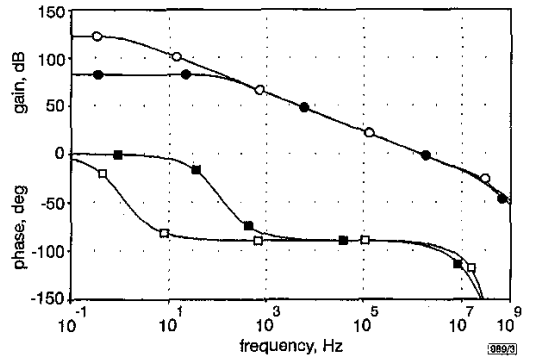

Fig. 3 *Gain and phase responses of simulated DOTA-C integrators*

● classical cascode DOTA-C integrator (gain)
■ classical cascode DOTA-C integrator (phase)
○ proposed active-feedback cascode DOTA-C integrator (gain)
□ proposed active-feedback cascode DOTA-C integrator (phase)

Simulation results: PSPICE simulations were performed for the proposed DOTA and an equivalent classical cascode DOTA (employing classical double-cascode CMs). MIETEC 1.2μm *n*-well CMOS technology model parameters (V_{T0n} = 0.736V, V_{T0p} = -0.751V, μ_{0n} = 515cm^{2}V^{-1}s^{-1}, μ_{0p} = 175cm^{2}V^{-1}s^{-1}, t_{ox} = 23.8nm) were used for the simulations. L = 3μm for all devices; W = 20μm for all *n*-channel devices (except that $W_{C1,C2,C3,C4,K1,K2,K3,K4}$ = 2μm to achieve κ = 10) and W = 40μm for all *p*-channel devices (except that $W_{C5,C6,K5,K6}$ = 4μm to achieve κ = 10; and $W_{1,2}$ = 10μm). V_{DD} = $-V_{SS}$ = 2.5 V and I_A = 30 μA for both simulated DOTAs, to achieve a transconductance of G_m = 45μs. It is clear from Table 1 that the proposed DOTA structure achieves a much larger R_{out} (therefore a much larger DC gain) with respect to its classical cascode counterpart, while keeping mirroring precision and GBW high (current reflection error is < 0.02% for the active-feedback CMs of the proposed DOTA, which means that device mismatches will determine the precision). The increase in consumed power is only 10%. The improvement in C_{out} (thus in GBW) is due to the fact that, in an active-feedback CM, the capacitive current through C_{GD3} (see Fig. 1*b*) simply flows to the ground through MK; however a similar capacitive current in a classical double-cascode CM flows to the input path and is mirrored back to the output, where it appears a second time. Therefore, the C_{out} value is almost doubled [3].

Fig. 3 shows the gain and phase responses of two DOTA-C integrators constructed with the proposed DOTA and the equivalent classical cascode DOTA, with C_L = 5pF. AC plots prove that the proposed structure enables integration within a much wider frequency range. The frequency range within which $\phi = -90° \pm 10°$ (phase error ≤ 10°) is 6.3Hz – 5.6MHz for the proposed DOTA-C integrator and 635Hz – 3.5MHz for the classical cascode DOTA-C integrator. The improvement is more than two decades of frequency. The very high output impedance of the proposed DOTA helps to significantly reduce the low-frequency phase errors. The use of C_L values of the order of several tens of picofarads enables filtering beyond the hertz range.

Table 1: Simulation results for proposed and equivalent classical cascode DOTAs

	Classical cascode DOTA	Proposed cascode DOTA
DC Gain (differential)	81.9dB	122dB
GBW	234MHz	392MHz
R_{out} (differential)	283MΩ	28.5GΩ
C_{out} (differential)	30fF	18fF
Power dissipation	450μW	496μW

Conclusions: Use of the proposed very high output impedance precision DOTA in a DOTA-C integrator enables integration at very low frequencies, as well as at very high frequencies, with a capacitor of the order of several picofarads. The described CM implementation method is simple, power-efficient and directly applicable to other types of differential-output COBADs, such as dual-output current conveyors and fully-differential current amplifiers.

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A. Zeki and H. Kuntman (*Istanbul Technical University, Faculty of Electrical and Electronics Engineering, 80626, Maslak, Istanbul, Turkey*)

E-mail: alizeki@ehb.itu.edu.tr

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Phase advancing for current in R-L circuits using switched capacitors

C. Suciu, M. Kansara, P.G. Holmes and W. Szabo

A periodically reversed switched capacitor is connected in series with an RL load supplied from a sinusoidal voltage source. To control the phase of the fundamental component of load current, a novel algorithm for the switching of the capacitor is derived and tested.

Introduction: Switched capacitor (SC) networks offer considerable flexibility in varying the transfer function between input and output. Switched capacitor techniques are currently applied in implementing filters in silicon integrated circuits [1]. Switched capacitor filters use periodically operated switches with capacitors and