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Accurate and high output impedance current mirror suitable for CMOS current output stages

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Indexing terms: CMOS integrated circuits, Current mirrors

An accurate, very-high-output-resistance active-feedback cascode current mirror has been proposed and compared with a previously reported accurate cascode current mirror. Comparisons have shown that, besides higher accuracy and output resistance, the proposed circuit has no residual error, but has a wider output voltage swing, a much higher PSRR, and an easier and more flexible design.

Introduction: Much work has been carried out on current-output-based active devices (COBADs), such as current conveyors and OTAs, because of their wider bandwidths with respect to voltage-mode structures, such as op-amps. Also, the availability of multiple current outputs is advantageous. A current output stage (COS) is one of the main building blocks of COBADs. Both linearity and output resistance of a COS depend on the performance of the current mirrors (CMs) used and both must be sufficiently high. The impedance of an integrator capacitor at the output of a COBAD in a continuous-time filter is too high at low frequencies to be handled even by a conventional cascode COS. Very high output resistance linear COSs are required, thus CMs are used.

Cascode current mirrors: The accuracy and output resistance of a classical cascode CM (Fig. 1*a*) are much higher than for a simple CM. However, the input voltage swing is restricted due to the doubling of input devices. The cascode CM in Fig. 1*b* is a good solution, but accuracy decreases due to a fixed V_{G23}, preventing V_{DS22} from following $V_{DS21} = V_{GS21}$. A good improvement in the accuracy was introduced by the so-called 'improved dynamic matching current mirror' (DMCM) which is shown in Fig. 1*c* [1]. V_{DS32} follows V_{DS31} dynamically via source followers M3X and M33. DC matching is improved by creating a V_{GSX} dependent on the input current I_{IN}, with the aid of simple CMs, for adjusting V_{GS33} so as to force V_{DS32} to follow V_{DS31}. However, proper care is required to adjust $(W/L)_{3X}$ for the highest accuracy level, which degrades as I_{IN} changes, due to the difference between threshold voltages of PMOS and NMOS transistors. Therefore, large signal linearity is not high enough for a COS using DMCMs. Also, owing to the body effect on M3X, a residual nonlinearity may remain [1], due to the high threshold of M3X caused by the body effect, which cannot be overcome by adjusting $(W/L)_{3X}$. The body effect on M3X also causes a supply-dependent I_{OUT}, resulting in a low PSSR. This also means that power supply flexibility is poor, i.e. the accuracy optimised for a certain V_{DD} value degrades for a different V_{DD} value.

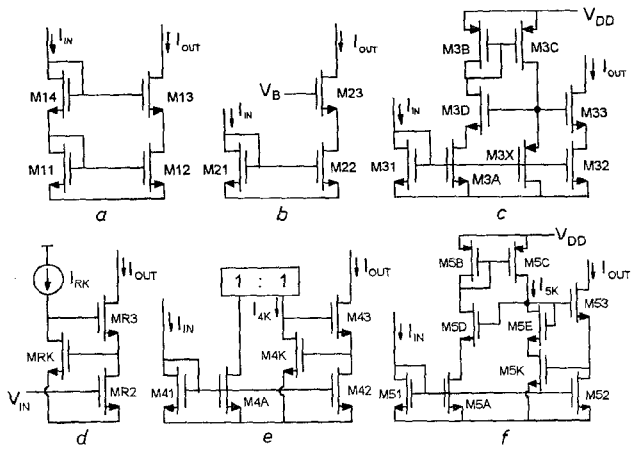

Fig. 1 *Cascode structures*
a Classical cascode CM
b Single input transistor cascode CM
c Improved DMCM
d RGC stage
e Active-feedback cascode CM
f Proposed IAFCCM

Proposed current mirror: Recently, a novel method was introduced to make use of the regulated-gate cascode (RGC) stage [2] of Fig. 1*d*, for obtaining very-high-output-impedance accurate CMs for use in a high performance OTA [3]. A similar alternative method suitable for general purposes is explained schematically in Fig. 1*e*. In the RGC stage, a high output impedance is achieved by the negative active-feedback loop along the amplifier MRK-I_{RK} and the source follower MR3. In the CM of Fig. 1*e*, I_{RK} of the RGC stage was replaced with a dependent source I_{4K}, nominally equal to I_{IN}. $(W/L)_{4K} = (W/L)_{4A}$ are chosen equal to $(W/L)_{41} = (W/L)_{42}$, to set V_{DS42} to be equal to V_{DS41}, thus achieving an accurate current reflection for any I_{IN} value. If the upper CM is a simple CM, channels of its PMOS transistors (e.g. M3B and M3C) can be set to be long enough to reduce the channel length modulation effect to achieve sufficient accuracy, since they should only match with each other i.e. $(W/L)_{3B} = (W/L)_{3C}$. However, channel lengths of M4A and M4K should remain equal to M41 and M42, otherwise precise matching with M41 and M42 cannot be achieved, even if $(W/L)_{4A,4K} = (W/L)_{41,42}$ is chosen. Therefore, these effects must be eliminated by setting V_{DS4A} and V_{DS4K} equal to V_{DS41}. In the proposed improved active-feedback cascode current mirror (IAFCCM) of Fig. 1*f*, this is performed by M5D and M5E (where $(W/L)_{5D,5E} = (W/L)_{53}$) by supplying voltage drops from the gate of M53 to drains of M5A and M5K, equal to V_{GS53}. This brings no degradation to the output resistance, since the feedback loop gain does not change, as proven below.

Assuming the gain of source followers M43 and M53 to be unity (i.e. $1/g_{m43} < r_{ds42}$ and $1/g_{m53} < r_{ds52}$), the loop gains are

$$K_{loop4} = -g_{m4K}(r_{ds4K}//r_{ds4C}) \quad (1)$$

$$K_{loop5} = \frac{-g_{m5K}r_{ds5K}r_{ds5C}}{r_{ds5K} + 1/g_{m5E} + r_{ds5C}} \simeq -g_{m5K}(r_{ds5K}//r_{ds5C}) \quad (2)$$

for the CM of Fig. 1*e* and for IAFCCM, respectively, where $1/g_{m5E} < r_{ds5K}$ is assumed and the body effect is neglected for simplicity. Output resistances for the CMs in Fig. 1*e* and *f* are somewhat higher than those of the CMs of Fig. 1*a*, *b* or *c*. Output resistances for the DMCM of Fig. 1*c* and the proposed IAFCCM of Fig. 1*f* can be expressed simply as

$$R_{O3} = g_{m33}r_{ds32}r_{ds33} \quad (3)$$

$$R_{O5} = g_{m53}g_{m5K}r_{ds52}r_{ds53}(r_{ds5K}//r_{ds5C}) \quad (4)$$

respectively. Eqn. 3 is valid for all the cascode CMs of Fig. 1. Eqns. 2, 3 and 4 imply that improvement in the output resistance of an active-feedback CM, with respect to a conventional cascode CM, is by a factor $(1 - K_{loop5}) \simeq -K_{loop5} = g_{m5K}(r_{ds5K}//r_{ds5C})$.

Simulation results: SPICE simulations have been carried out for V_{DD} = 5V, with model parameters of Tübitak-Yital's 3μm *n*-well CMOS process. L = 3μm for all devices in both DMCM and IAFCCM but L = 9μm for M3A, M3B, M5A and M5C, for accuracy of simple CMs. W = 150μm for NMOS, W = 300μm for PMOS transistors, and W = 125μm for M3X, which achieves the highest accuracy for DMCM. Fig. 2 shows the transfer error against I_{IN} curves, for 5μA < I_{IN} < 500μA range (log scale) and V_{OUT} = 5V, where the error is defined as

$$\varepsilon(\%) = 100(I_{OUT} - I_{IN})/I_{IN} \quad (5)$$

Because DMCM was designed to satisfy the best accuracy at I_{IN} = 50μA, it can achieve a low error only within that point's proximity. Conversely, IAFCCM keeps its high accuracy level within the whole I_{IN} range, because the $V_{DS2} = V_{DS1}$ equality is achieved precisely for any I_{IN} value. Although the simulated DMCM has fortunately not shown a residual error, its PMOS complement, which is needed in a COS, has been found to possess a residual error of >10% (as mentioned above and in [1]). Elimination by resizing is not possible (this might occur for the simulated DMCM for a higher V_{DD} value). Therefore, a comparison of COSs constructed with DMCMs and IAFCCMs was avoided.

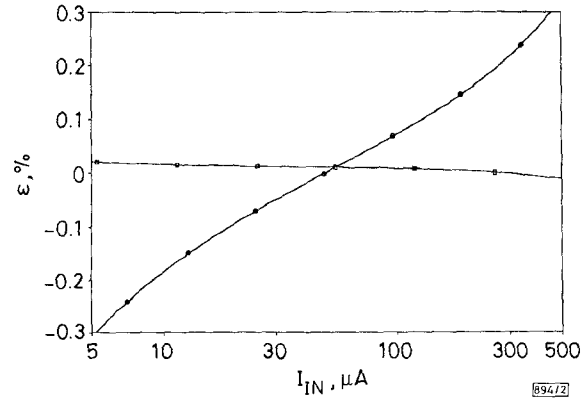

Fig. 2 *Current transfer error against I_{IN}*

I_{IN} in logarithmic scale
● DMCM
□ proposed IAFCCM

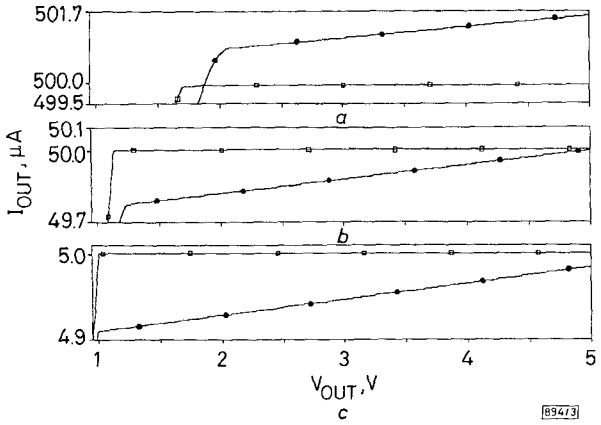

Fig. 3 *I_{OUT} against V_{OUT} curves for three I_{IN} values*

a I_{IN} = 500μA
b I_{IN} = 50μA
c I_{IN} = 5μA
● DMCM
□ proposed IAFCCM

Fig. 3 shows I_{OUT} against V_{OUT} curves for I_{IN} = 5, 50 and 500μA. It is clear that IAFCCM shows a much better output resistance and accuracy behaviour than DMCM, which can achieve a high accuracy only for I_{IN} = 50μA and V_{OUT} = 5V case. Output resistances for I_{IN} = 50μA are R_{OUT3} = 16.1MΩ for DMCM and R_{OUT5} = 18.6GΩ for IAFCCM. The improvement is by a factor of 1155, which should be equal to $(1 - K_{loop5})$, according to theory. This was verified by simulation and −1184 was found for K_{loop5}, supporting the theory. Also, the output swing for the proposed CM is wider, as a result of a high output resistance, delaying the breakpoint of the I_{OUT}-V_{OUT} curve [2].

The supply voltage dependency (SD) of I_{OUT} for DMCM was found to be 3.1, 1 and 0.4% for I_{IN} = 5, 50 and 500μA, respectively, where *SD* is defined as

$$SD = 100(dI_{OUT}/dV_{DD})/I_{IN} \quad (6)$$

These SD values for DMCM are rather high. For IAFCCM, *SD* = 0.012, 0.008 and 0.015% for I_{IN} = 5, 50 and 500μA, respectively, supplying a much higher PSRR and a wide power supply flexibility.

Bandwidths and output capacitances for DMCM and IAFCCM have been found to be BW_3 = 35MHz, C_{OUT3} = 15.6fF, and BW_5 = 52.3MHz, C_{OUT5} = 15.9fF, respectively, implying no degradation in the frequency behaviour in IAFCCM. One of the main reasons for the improvement of BW is that IAFCCM does not have an extra gate (gate of M3X in DMCM) connected to the input node.

Conclusions: The new CM shows a much better accuracy and output resistance performance than an equivalent DMCM. It needs no proper care in design, as DMCM does. No residual error exists in the proposed CM and the PSRR is much higher, the output voltage swing range is wider, with respect to an equivalent DMCM, without any bandwidth performance shift. Therefore, the proposed structure is a much more suitable CM for use in high linearity, high output impedance COSs. The design method can be applied to bipolar and MESFET structures.

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Consideration of thermal constraints during multichip module placement

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Indexing terms: Multichip modules, Circuit layout CAD

A multichip module placement algorithm which handles heat distribution as well as traditional placement objectives is presented. The algorithm uses a combined quad-partitioning genetic search, and simulated annealing technique. Experimental results show improvements in the min-cut and simulated annealing algorithms, in terms of net length, while satisfying the heat distribution constraints.

Introduction: A new multichip module (MCM) placement algorithm, MPH, is presented. Many placement algorithms for integrated circuits and printed circuit board technologies can be found in the literature. However, most are not suitable for multichip module (MCM) placement. Although some algorithms have been proposed to consider heat constraints, they are either used for resistors instead of chips, do not simultaneously consider wire length, or cannot handle fixed-area constraints. The MPH algorithm presented here takes both wire length and heat constraints into consideration concurrently.

Algorithm: Inputs to the MPH algorithm include the size of the substrate, the value of heat flux created by each chip, the netlist,