2. IDEAL OTA STRUCTURE

The circuit symbol of the DO-OTA (dual-output operational transconductance amplifier) is given in Figure 1.

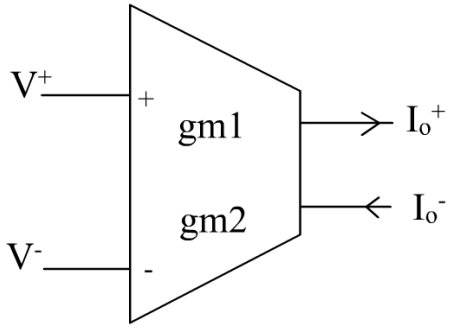


Figure 1 Ideal DO-OTA circuit

Ideally, DO-OTA is assumed as an ideal voltage controlled current source and can be described by following equations.

$$I_o^+ = g_{m1}(V^+ - V^-) \quad I_o^- = g_{m2}(V^- - V^+) \qquad (1)$$

At most of the DO-OTA circuits, it is taken as $g_{m1}=g_{m2}$. In this work all g_m values are equal. For other applications, taking different width and length values for MOS transistors at output stages could vary gm.

3 PROPOSED TOPOLOGIES

From the equation (1), on ideal case the relationship between input voltage and output current is linear. But in real world this relationship is not linear. In today's world, the linearity is an important subject at telecommunication. So circuits must be very linear to have the best performance.

Input stage: To achieve that linear relationship between input differential voltage and output current, linearization techniques for input cells are proposed. Some of these circuit topologies are given at this work.

On the other hand, another restrict for OTA circuits is output impedance. To achieve best performance circuits must have high output resistances [1].

Output stage: The output stage of the proposed DO-OTA circuit is based on a previous work by Zeki and Kuntman [1]. The output stage is realized by to use of high-output-impedance current mirrors [1,2]. Furthermore it was demonstrated that this type output stage exhibits improved output characteristics compared to the conventional circuits constructed with cascode-current mirrors. The output stage achieves a much larger R_{out} and therefore a much larger DC gain with respect to its classical cascode counterpart while keeping mirroring precision and GBW high.

3.1 INPUT STAGES

To compare DO-OTA linearised input stages, one classical input stage and four other linearised input stages are given at this work. The difference between these circuits is given by total harmonic distortion (THD) analysis[8].

3.1.1 CLASSICAL INPUT STAGE

The classical input stage for an OTA circuit is differential pair. Differential pair consists of two MOS transistors and a current mirror. In ideal case this current mirror is an ideal one. At applications MOS current mirrors realize this ideal current mirror.

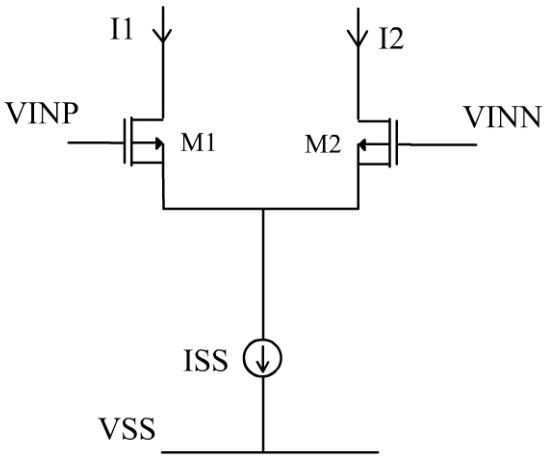


Figure 2 Differential pair

Differential pair can be seen from Figure 2. If we ignore the output resistances of MOSFETs and body effect, the current-voltage relationship is,

$$I_{D1} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 [V_{GS1} - V_{th}]^2 \quad I_{D2} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 [V_{GS2} - V_{th}]^2 \tag{2}$$

Differential input signal can be defined as,

$$\Delta V_I = V_{INP} - V_{INN} = V_{GS1} - V_{GS2} \tag{3}$$

If we combine the equations (2) and (3) we achieve,

$$\Delta I_D = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)\Delta V_I \sqrt{\frac{2I_{SS}}{\mu C_{ox}\left(\frac{W}{2L}\right)} - (\Delta V_I)^2} \tag{4}$$

The equation (4) is valid only for the signals that are,

$$\Delta V_I \le \sqrt{\frac{2I_{SS}}{\mu C_{ox}\left(\frac{W}{L}\right)}} \tag{5}$$

But if the input signal is larger than this limit, the conductivity of one of the input MOSFETs become larger than the other and current flows from this MOSFET and becomes $\Delta I_D = I_{SS}$.

The transconductance of the circuit is given by,

$$G_m = \sqrt{I_{SS}\mu C_{ox}\left(\frac{W}{L}\right)} \qquad (6)$$

3.1.2 NEDUNGADI INPUT CIRCUIT

One of the most popular linearised input circuit is Nedungadi's input circuit [3] The aim of this linearisation technique is inserting a constant voltage source between the input pairs. In ideal case system can be found at Figure 3.

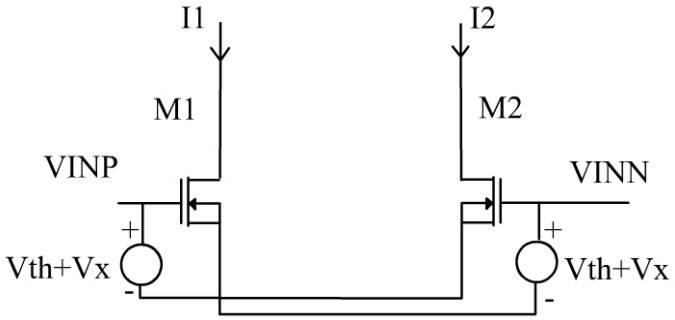


Figure 3 Ideal Nedungadi circuit

From Figure 3 we have,

$$I_1 = k(V_x + \nu)^2 \qquad (7)$$

$$I_2 = k(V_x - \nu)^2 \qquad (8)$$

If we calculate the differential output current, $i = I_1 - I_2$ that is mirror by a PMOS transistor,

$$i = I_1 - I_2 = 4kV_x\nu \qquad (9)$$

is achieved. And at this case we have the transconductance of, $g_m = 4kV_x$.

In practical approach we have,

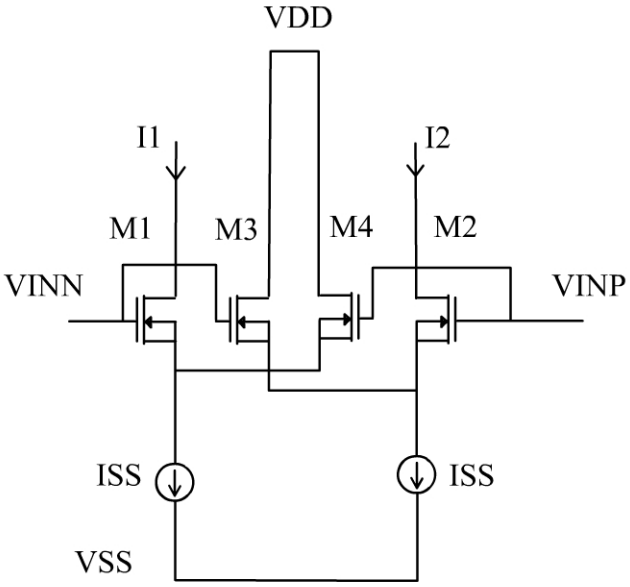


Figure 4 Practical Nedungadi input cell

At Figure 4, transistors M_3 and M_4 are n times wider than M_1 and M_2 and all transistors have same lengths. If we describe $V_b = \sqrt{\frac{I}{k}}$ and $x = \frac{\nu}{V_b}$, $y = \frac{i}{I}$ we achieve equations as,

$$y = \frac{i}{I} = \frac{i_1 + i_2}{I}, \quad \nu = V_1 - V_2, \tag{10}$$

$$\alpha = \frac{4n}{n+1}, \quad \beta = \frac{n}{(n+1)^2}, \quad \gamma = \frac{n(n-1)}{(n+1)^2} \tag{11}$$

If we want to write down the normalized output current, we achieve[2],

$$y = \alpha x\sqrt{1-\beta x^2}, \qquad |x| \le \sqrt{\frac{n+1}{n}} \tag{12}$$

$$y = 1 + \gamma x^2 + \alpha|x|\sqrt{1-\beta x^2}, \qquad \sqrt{\frac{n+1}{n}} \le |x| \le \sqrt{n+1} \tag{13}$$

$$y = (n+1)\,\mathrm{sgn}(x), \qquad |x| > \sqrt{(n+1)} \tag{14}$$

3.1.3 CROSS COUPLRED INPUT CIRCUIT

The main idea of this linearisation technique is the same as Nedungadi's input circuit. This time, V_{GS} of MOS transistors achieve constant voltage source. But the drawback of this circuit is the requirement of extra transistor level. The realization of circuit can be seen from

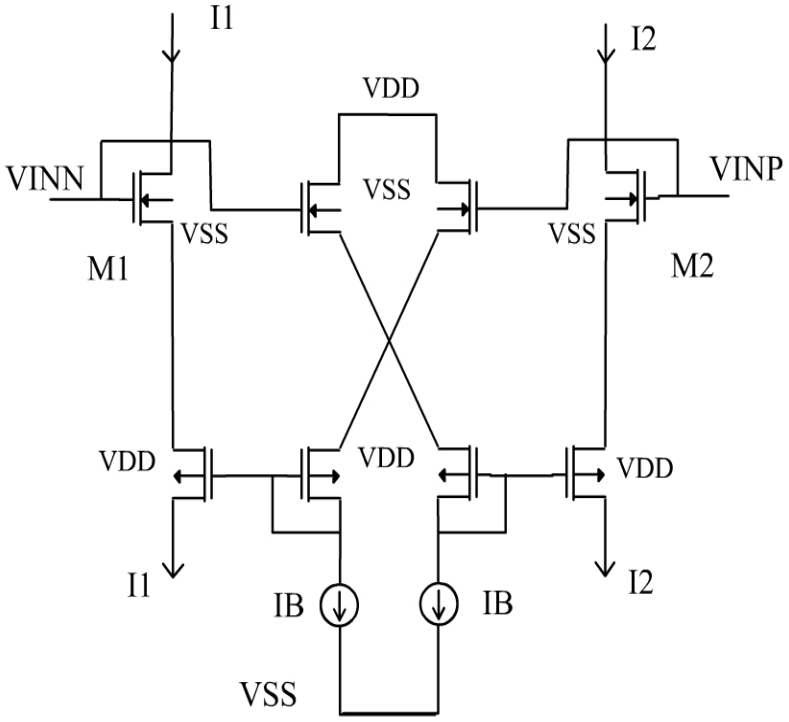


Figure 5 Cross coupled input circuit

If we want to write the equations,

$$I_{D1} = k(V_{GS1} - V_{th})^2 \tag{15}$$

$$I_{D2} = k(V_{GS2} - V_{th})^2 \tag{16}$$

Then we achieve the differential current,

$$\Delta I_D = I_{D1} - I_{D2} = k(V_{GS1} + V_{GS2} - 2V_{th})(\frac{V_{GS1} - V_{GS2}}{2}) \tag{17}$$

If we make $(V_{GS1} + V_{GS2} - 2V_{th})$ equal to a voltage source like V_b, we have

$$\Delta I_D = 2\beta V_b \nu \tag{18}$$

3.1.4 KRUMMENACHER INPUT CIRCUIT

This technique is linearisation by an emitter resistor. From bipolar versions of amplifiers this is a common way for linearisation. At CMOS circuits only the difference is usage of MOS transistors except the resistors. By doing this, smaller chip size can be achieved with less matching problems. Circuit can be seen from

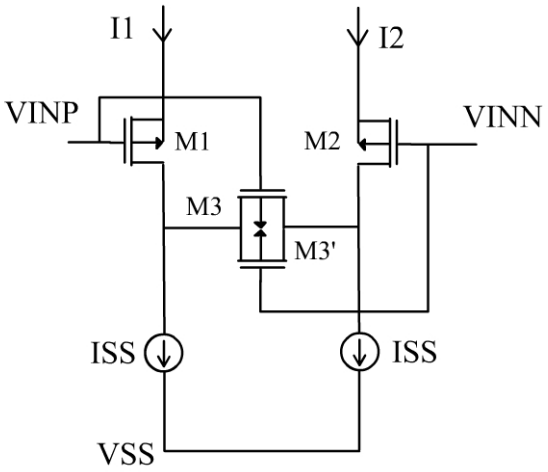


Figure 6 Krummenacher's input circuit

If M3 and M3' are not saturated, we have

$$I_{D3} = \mu C_{ox} \frac{W}{L}\left[(V_1 - V_{S2} - V_{th})(V_{S1} - V_{S2}) - \frac{(V_{S1} - V_{S2})^2}{2}\right] \tag{19a}$$

$$I_{D3'} = \mu C_{ox} \frac{W}{L}\left[(V_2 - V_{S2} - V_{th})(V_{S1} - V_{S2}) - \frac{(V_{S1} - V_{S2})^2}{2}\right] \tag{19b}$$

,
And from Kirchoff's law,

$$I_1 - I - I_{SS} = 0, \qquad I_2 + I - I_{SS} = 0 \tag{20}$$

are achieved. If we define $a = 1 + \frac{\beta_1}{4\beta_3}$, $v = g_{m0}$, $i = \frac{\Delta I_D}{I_{SS}}$, $g_{m0} = \frac{\partial \Delta I_D}{\partial \Delta V_i}$, we achieve the following equations.

$$i = v\sqrt{1 - \frac{v^2}{4}}, \quad g_{m0} = \left.\frac{\partial \Delta I_D}{\partial \Delta V_i}\right|_{v=0} = \frac{I_{SS}}{a(V_{GS} - V_{th})_{M1}} \tag{21}$$

If M3 and M3' are at saturation region,

$$|v| = \left|\frac{g_{m0}v}{I_{SS}}\right| > V_1 = \sqrt{\frac{a^2 + a + 0{,}5}{a^4 + 0.25}} \tag{22}$$

gives the linearity region. At this time output current equation is,

$$i = \pm \frac{\left[av\sqrt{4a-2} \pm \sqrt{4a - 1 - a^2v^2}\right]}{(4a-1)^2} \tag{23}$$

And maximum output current can be found from equation 24.

$$|v| = \left[\frac{g_{m0}v}{I_{SS}}\right] = V_2 = \frac{\sqrt{4a-2}}{a} \tag{24}$$

The results of DO-OTA circuits are at Chapter 5.

3.2 OUTPUT STAGES

To achieve best performance from a DO-OTA circuit, we must have a very high output resistance. The circuit at Figure 7, is a previous work by Zeki and Kuntman[1].

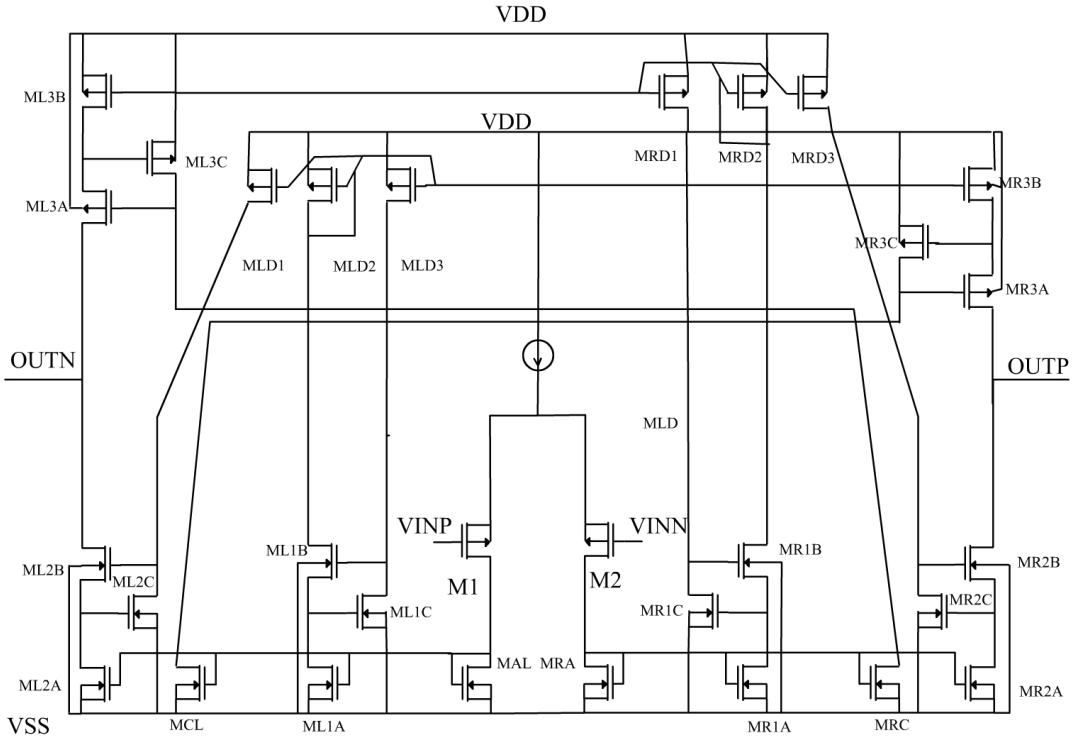


Figure 7 Regulated cascode stage (RGC)

and another output stage is another implementation of RGC stage with PMOS differential input and differential output. The previous work onthis output stage was on a NMOS single ended version.. Circuit topology can be seen from Figure 8.

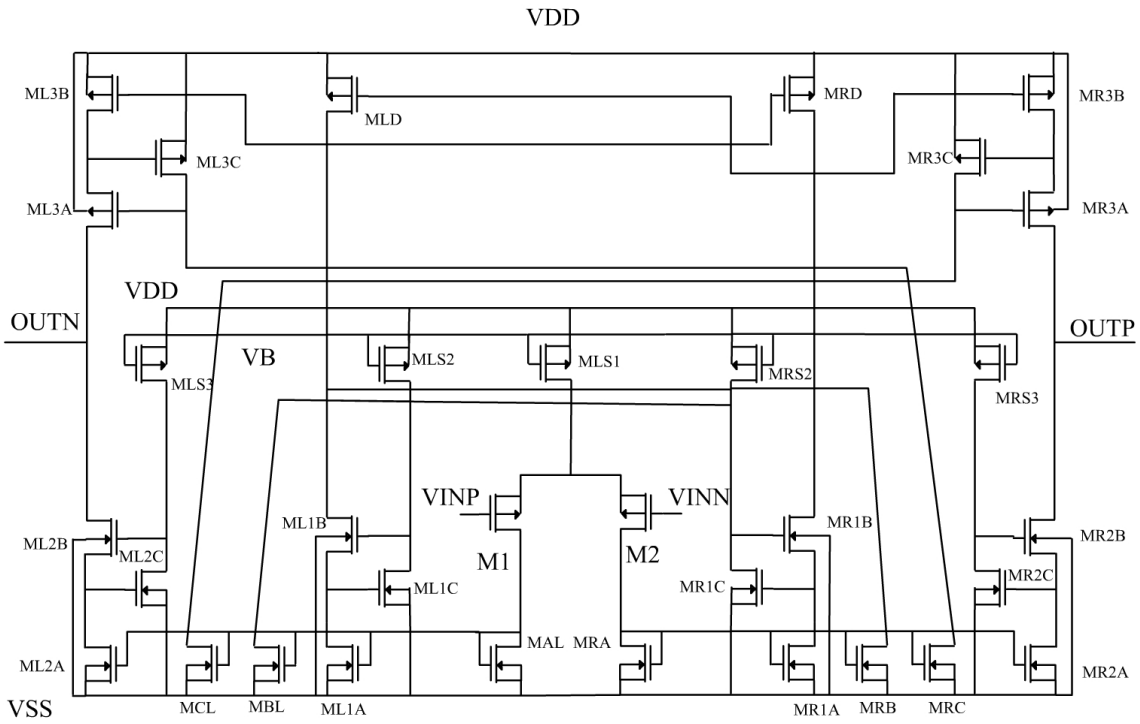


Figure 8 Proposed RGC

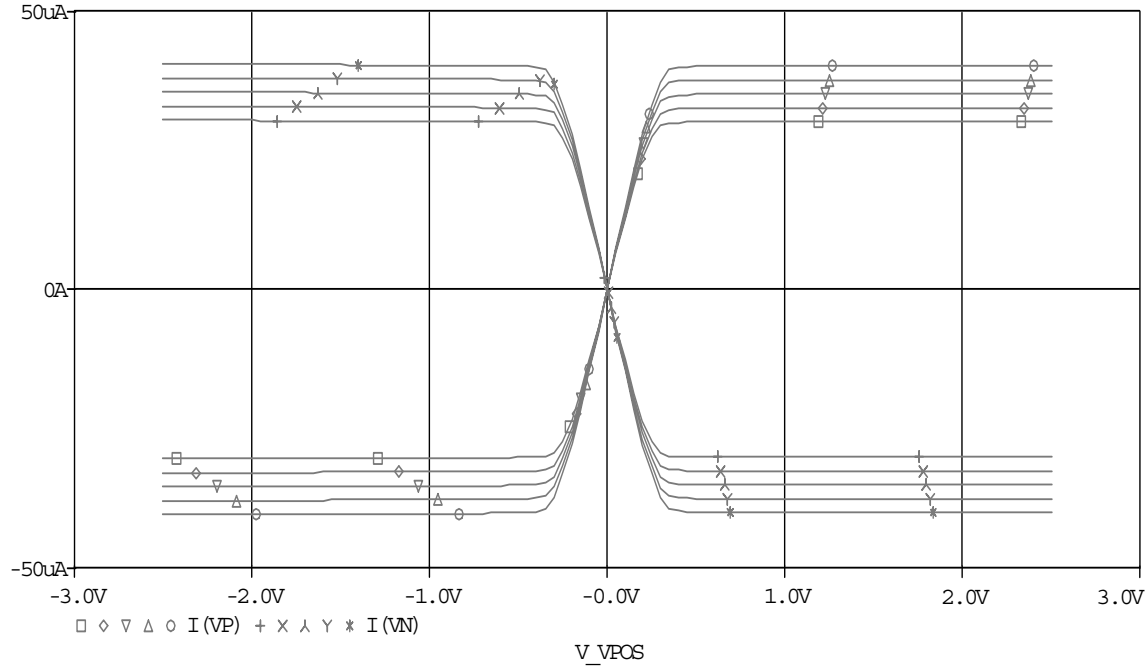
5 SIMULATION RESULTS

At simulations AMS 0.8µm MOS models are used. The supplies are 2.5 V and –2.5 V.

5.1 DC SIMULATIONS

5.1.2 Classical Input stage circuit simulation results:

With first output stage:



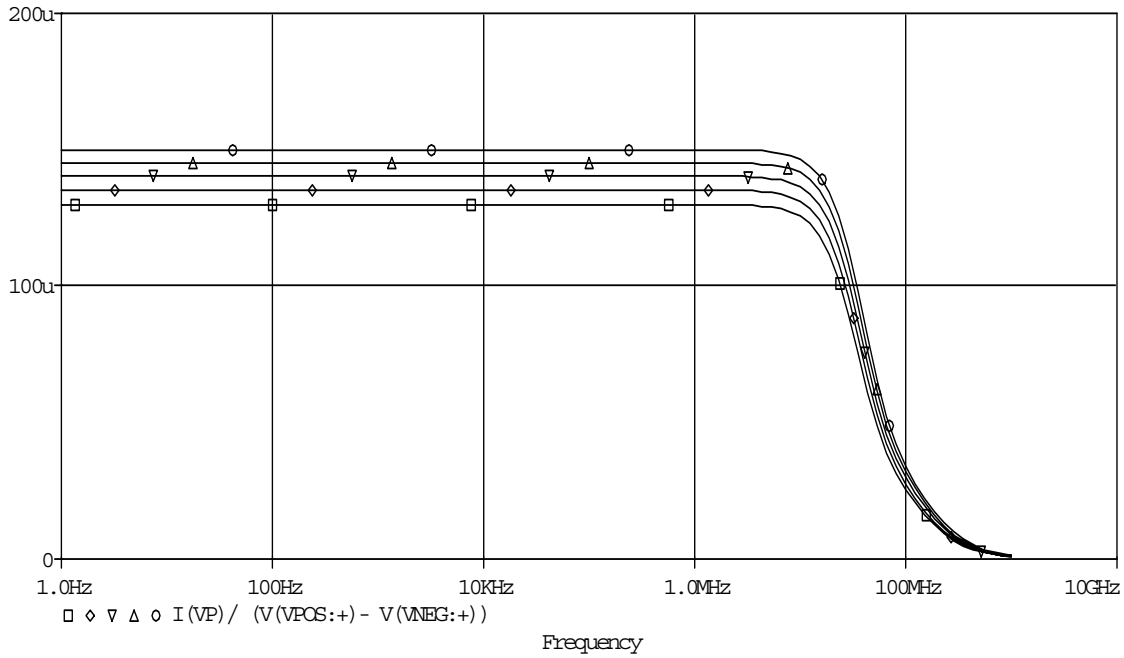
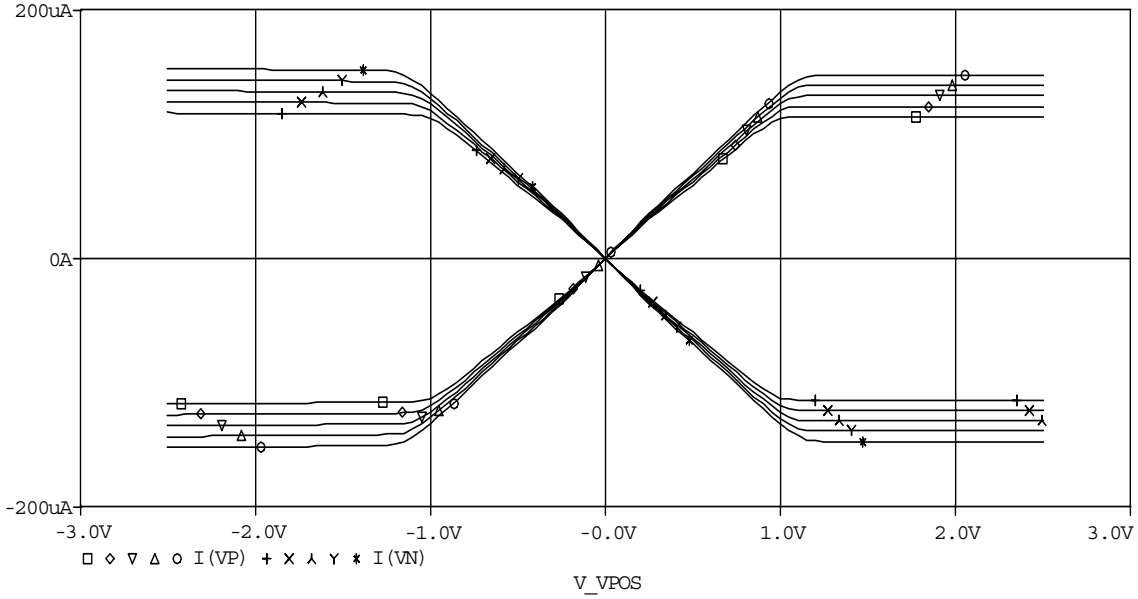


Figure 12a DC Characteristics **b)** Transconductance for biasing currents ranging 6µA to 10µA

5.1.3 Nedungadi Input stage circuit simulation results:

With first output stage:



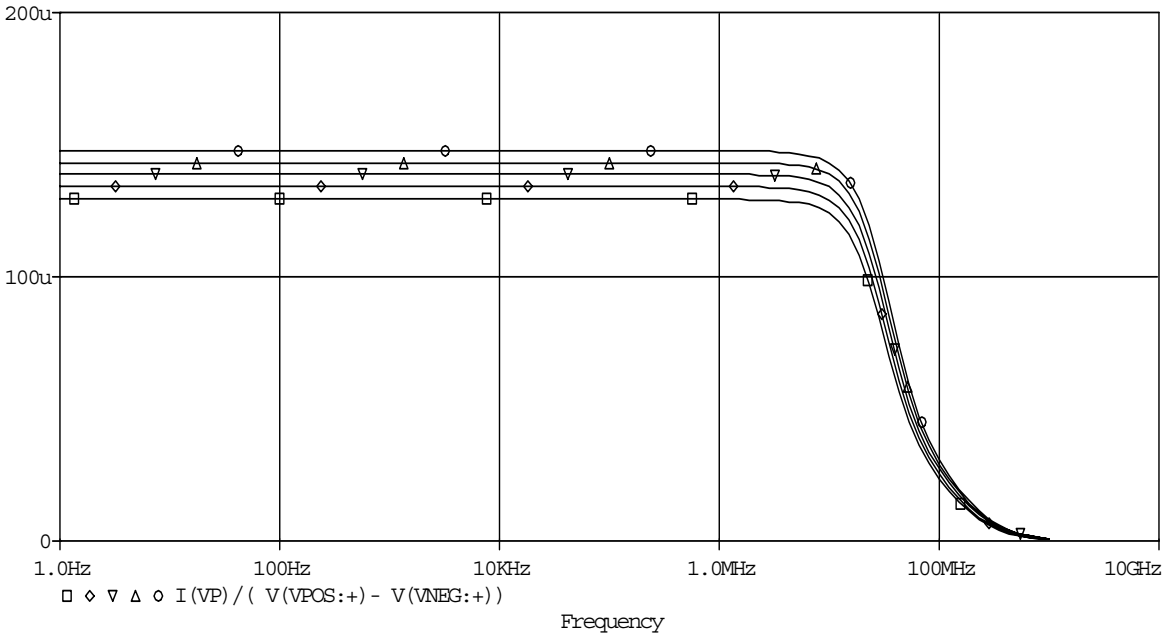
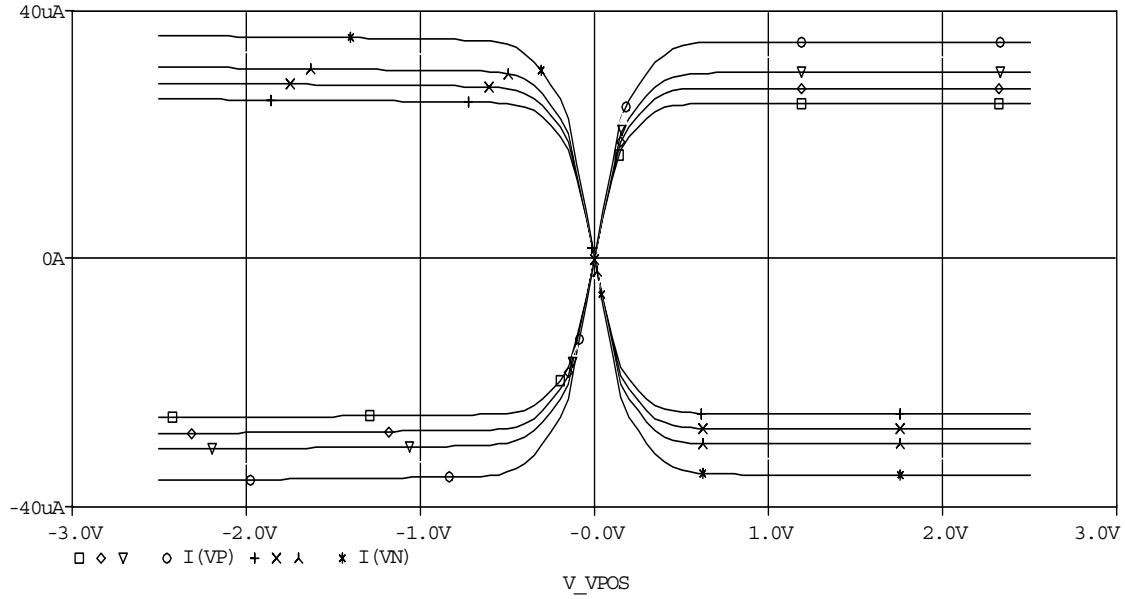


Figure 14a DC Characteristics **b** Transconductance for biasing currents ranging 11µA to 15µA

5.1.4 Cross coupled Input stage circuit simulation results:



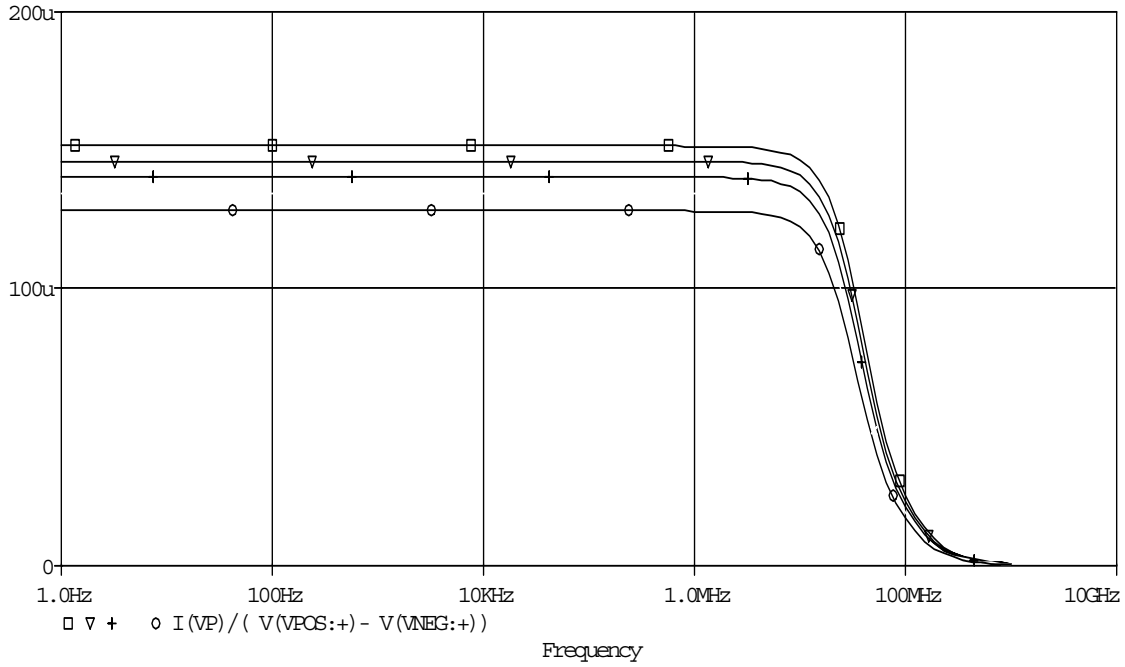
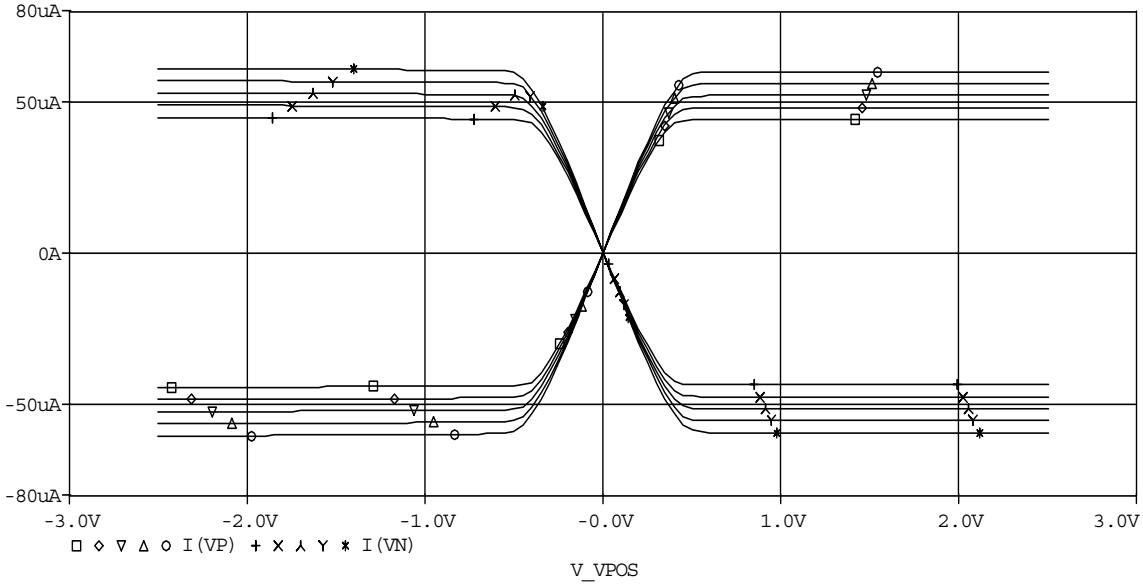


Figure 16a DC Characteristics **b)** Transconductance for biasing currents ranging 6µA to 10µA

5.1.5 Krummenacher Input stage circuit simulation results:

With first output stage:



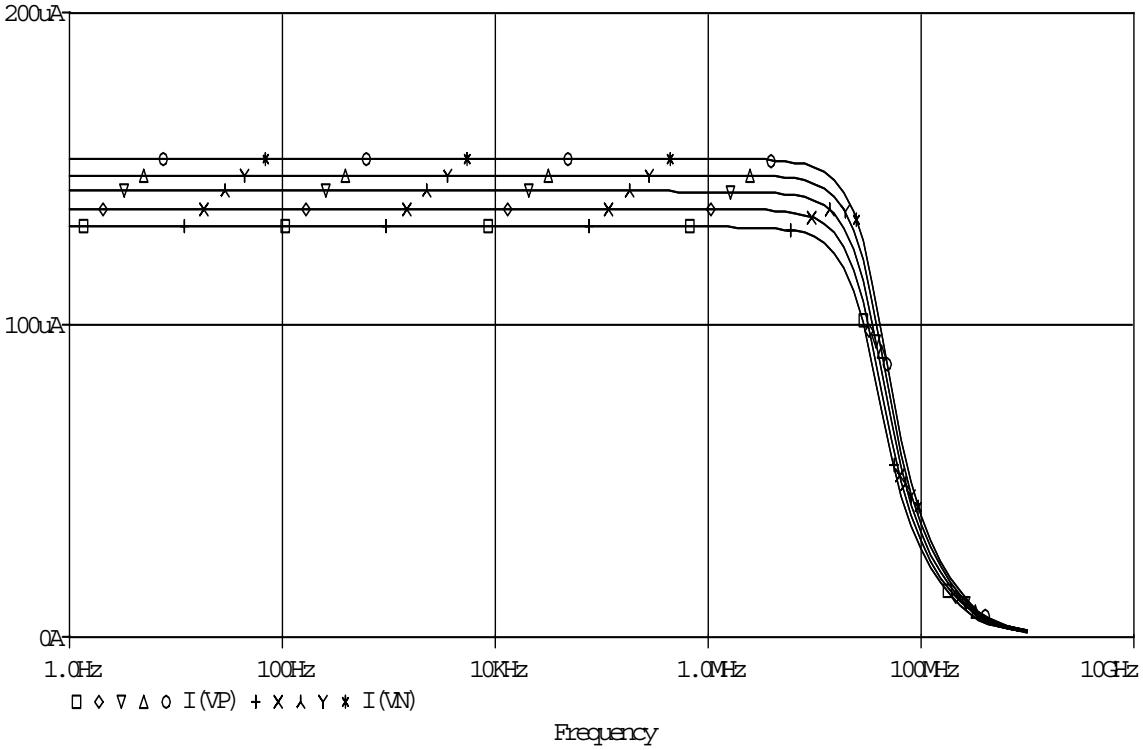


Figure 18a DC Characteristics **b)** Transconductance for biasing currents ranging 6µA to 10µA

5.2 THD Results

To compare the linearity regions of DO-OTA circuits, the integrator circuit on Figure 20 is used. Capacitors are 1 nF for all testy circuits.

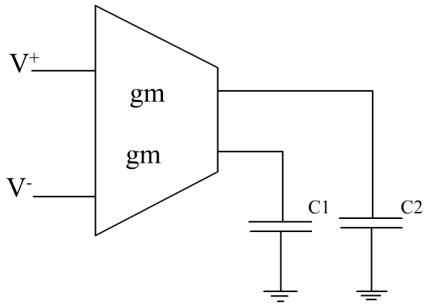


Figure 20 Integrator circuit

Results can be seen form Figure 21 and Figure 22. Comparison of theorical and practical linearity ranges can be seen from Table 1.

Table 1 Theorical and Practical Linearity ranges

	With First Output Stage		With Second Output Stage	
	Theorical(mV)	Practical(mV)	Theorical(mV)	Practical(mV)
Classical	330	380	110	180
Nedungadi	1420	1220	556	597
Cross Coupled	490	420	150	220
Krummenacher	930	510	700	280