The translinear principle, multipliers and dividers, the translinear cross-quad

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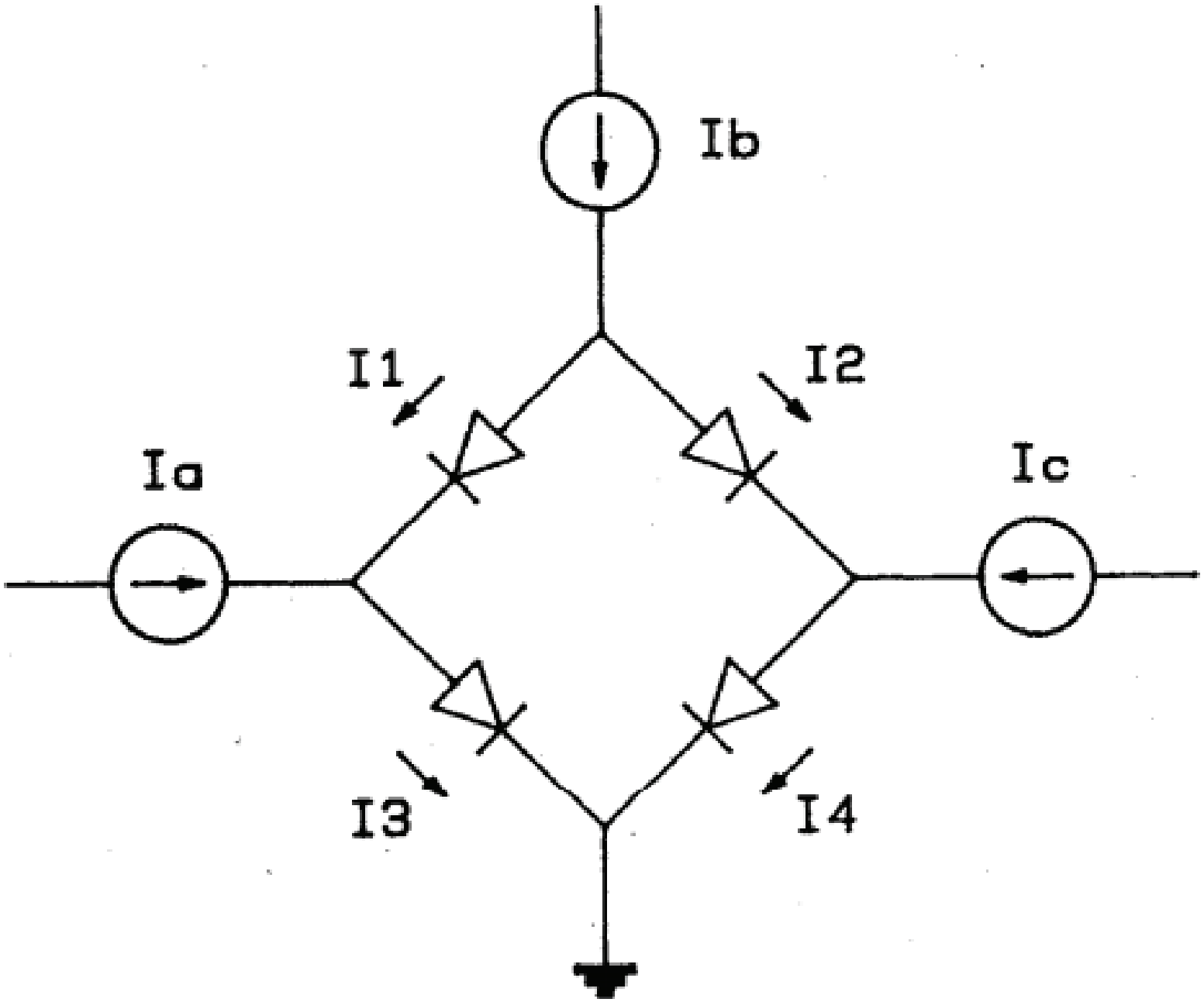
Current Mode Analog Circuit Design

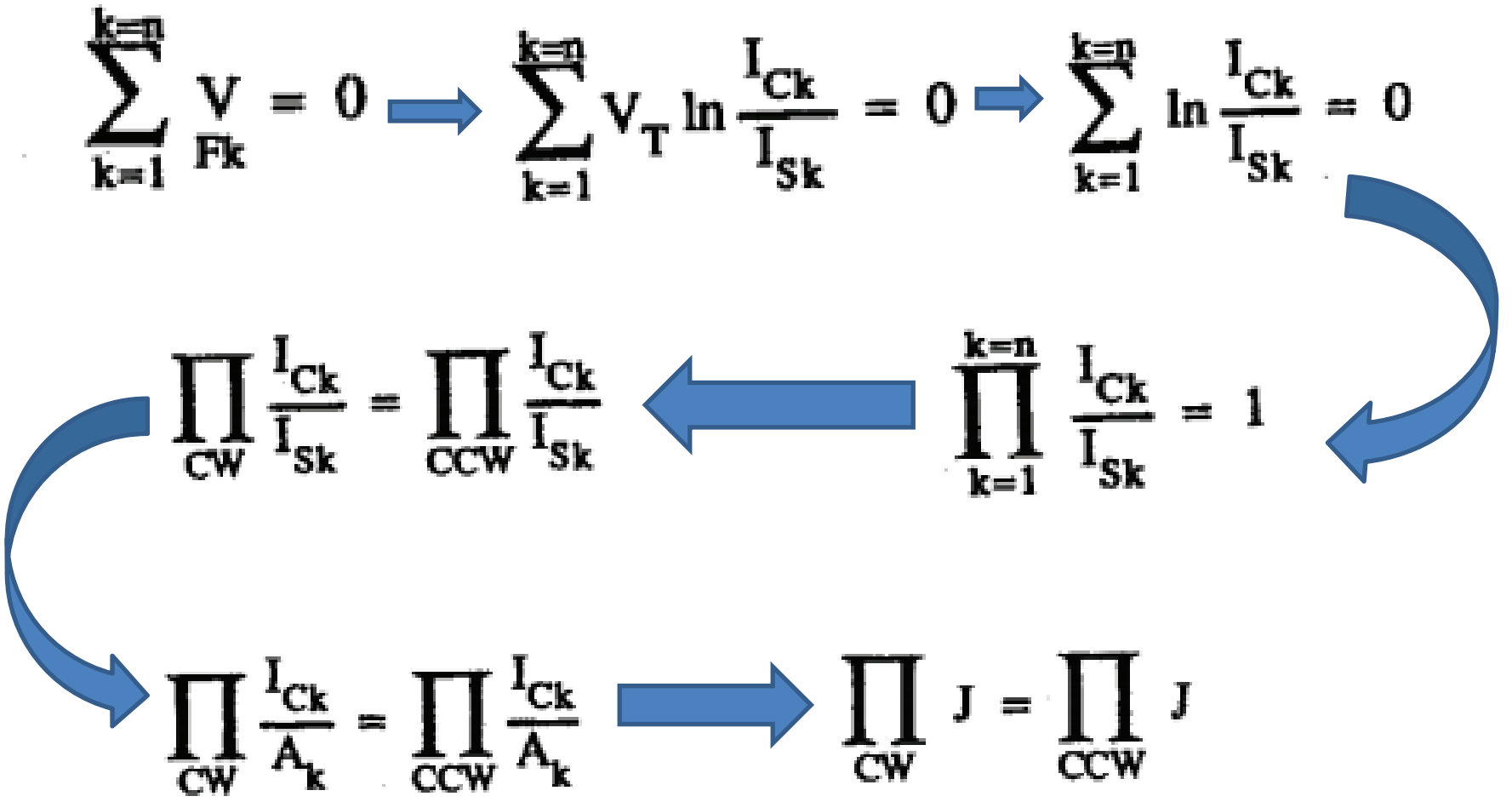
THE TRANSLINEAR PRINCIPLE

In a closed loop containing n PN junctons such as shown in the next slide, where the junctions are biased into forward conduction, the sum of the junction voltages, V_{FK}, must sum to zero.

$$\sum_{k=1}^{k=n} V_{Fk} = 0$$


Ib
I1
I2
Ia
Ic
I3
I4

THE TRANSLINEAR PRINCIPLE



THE TRANSLINEAR PRINCIPLE

Because $I_C / I_S \gg 1$,(Even if I_C=100pA, $I_C/I_S=10^4$) we can write the equation below if only these two is met:

1. **There must be an even number of junctions.**
2. **There must be an equal number of CW and CCW facing junctions.**

$$\prod_{k=1}^{k=n} \frac{I_{Ck}}{I_{Sk}} = 1$$

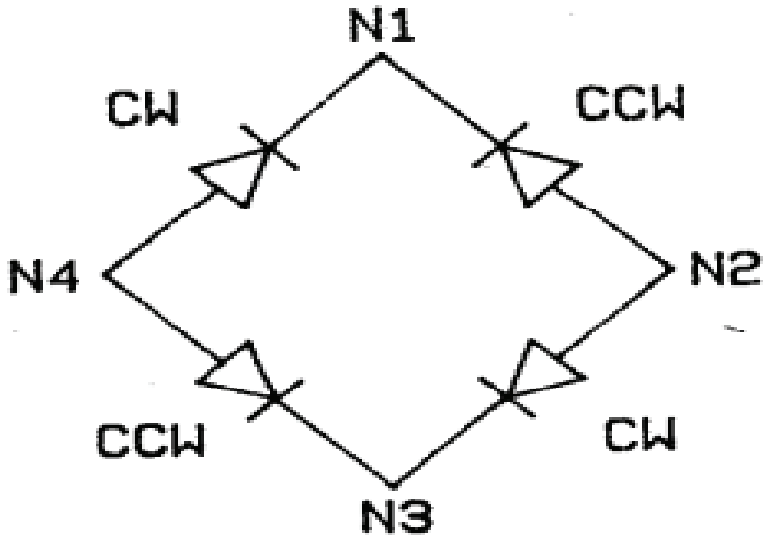
THE TRANSLINEAR PRINCIPLE

IN A CLOSED LOOP CONTAINING AN EVEN NUMBER OF FORWARD BIASED JUNCTIONS, ARRANGED SO THAT THERE ARE AN EQUAL NUMBER OF CW & CCW FACING POLARITIES, THE PRODUCT OF THE CURRENT DENSITIES IN THE CW DIRECTION IS EQUAL TO THE PRODUCT OF THE ONES IN THE CCW DIRECTION.

BASIC FOUR TRANSISTOR MULTIPLIER CELLS

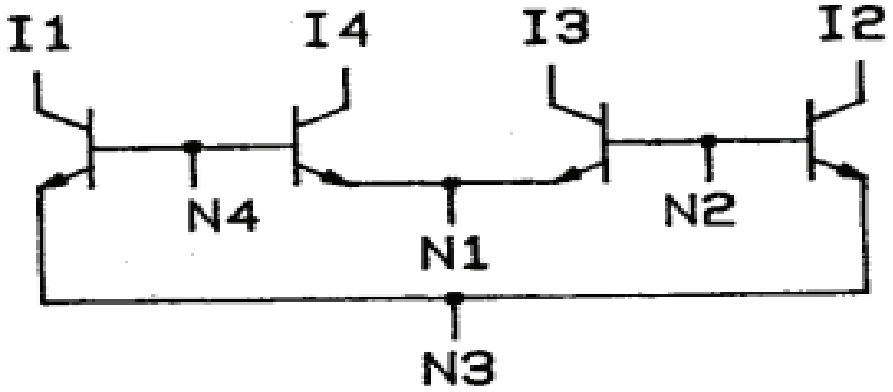
All TL multipliers are based on two basic cell types: TYPE A & TYPE B cells. These cells can be used to realize all multipliers and dividers. (1,2 and 4 quadrant ones) The common cell type is TYPE B.

TYPE A CELL



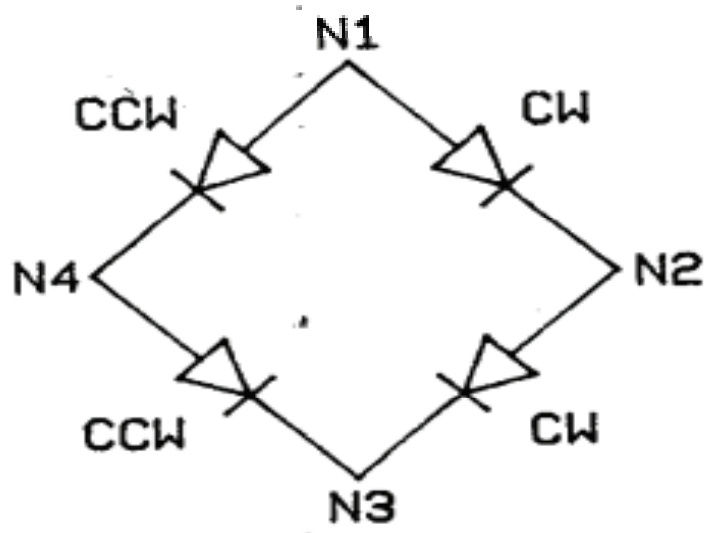
If all the four BJT s in this cell have equal emitter areas

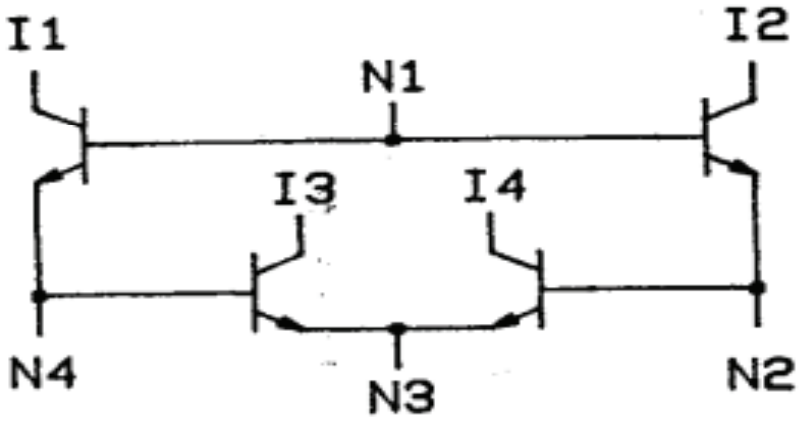
$I_1I_3=I_2I_4$



<u>Sequence:</u>
CW-CCW-CW-CCW

TYPE B CELL



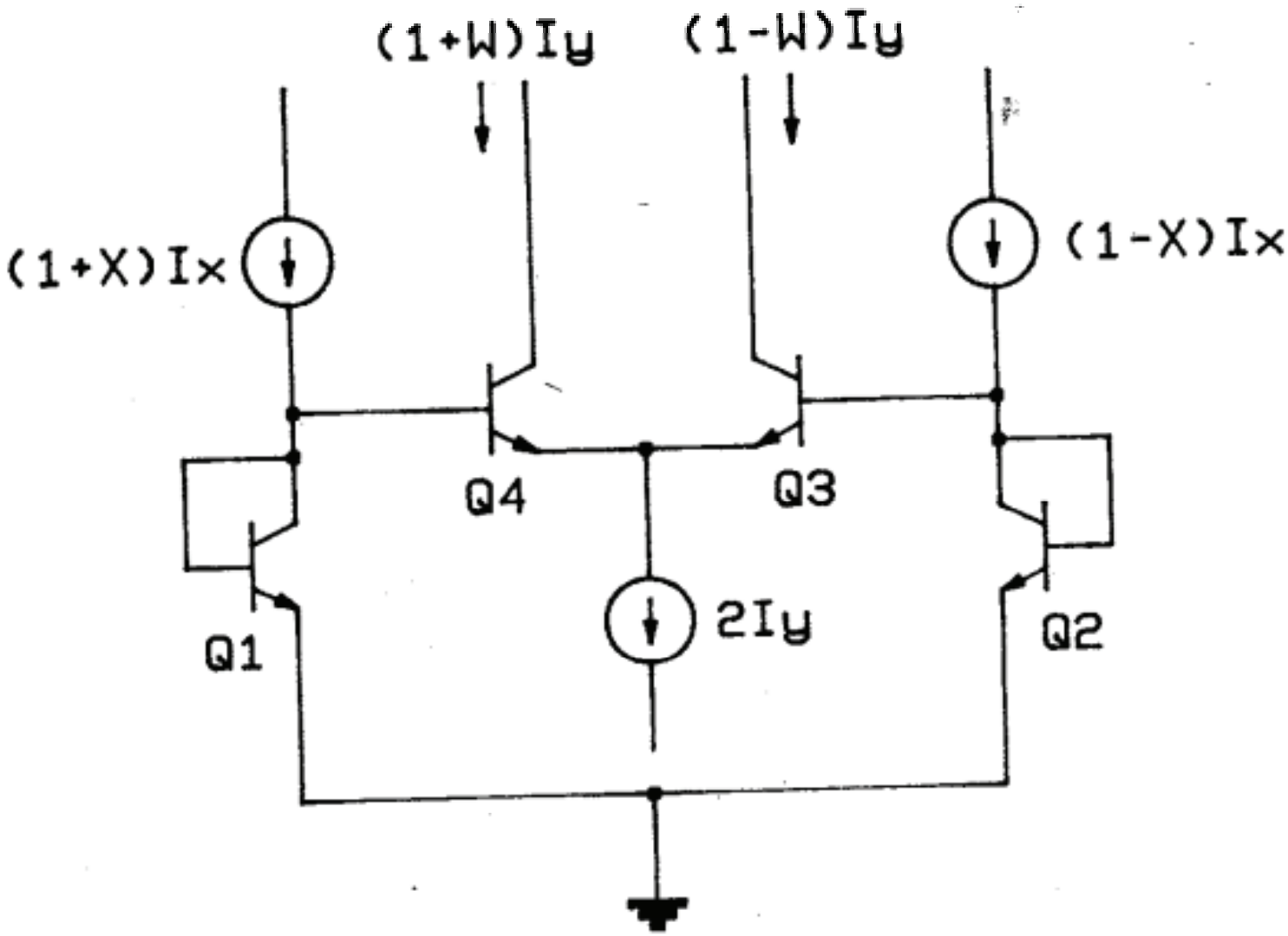


If all the four BJT s in this cell have equal emitter areas

$I_1 I_3 = I_2 I_4$

<u>Sequence:</u>
CW-CW-CCW-CCW

THE BETA-IMMUNE TYPE A CELL



THE BETA-IMMUNE TYPE A CELL

$$(1+W)Iy.(1-X)Ix = (1-W)Iy.(1+X)Ix$$

$$\Longrightarrow W \equiv X$$

$$Iw = (1+W)Iy - (1-W)Iy = 2XIy$$

For all values of I_Y and I_X, W=X. The dif. input is $2XI_X$. And the dif. output is $2XI_Y$. So the $G_i=I_Y/I_X$.

THE BETA-IMMUNE TYPE A CELL

Because W=X, for any transistor geometry and at any junction temperature, the currents in the inner pair are always an exact, linear replication of those in the outer pair. What is even more surprising is that the behaviour is essentially preserved even when we take into account any errors due to β. Let's define δ as either I_B/I_C or I_B/I_E and now rewrite equation.

THE BETA-IMMUNE TYPE A CELL

$$(1+W)I_y\{(1-X)I_x - \delta(1-W)I_y\} = (1-W)I_y\{(1+X)I_x - \delta(1+W)I_y\} \quad (2.30)$$

So we see still W=X, but we haven't finished the calculation yet.

$$I_w = (1-\delta)(1+W)I_y - (1-\delta)(1-W)I_y = 2(1-\delta)XI_y$$

So the output is a bit smaller, but only by the factor (1-δ) that is α. But the loss is quite independent of the gain I_Y/I_X. But the key is W & X is not affected.

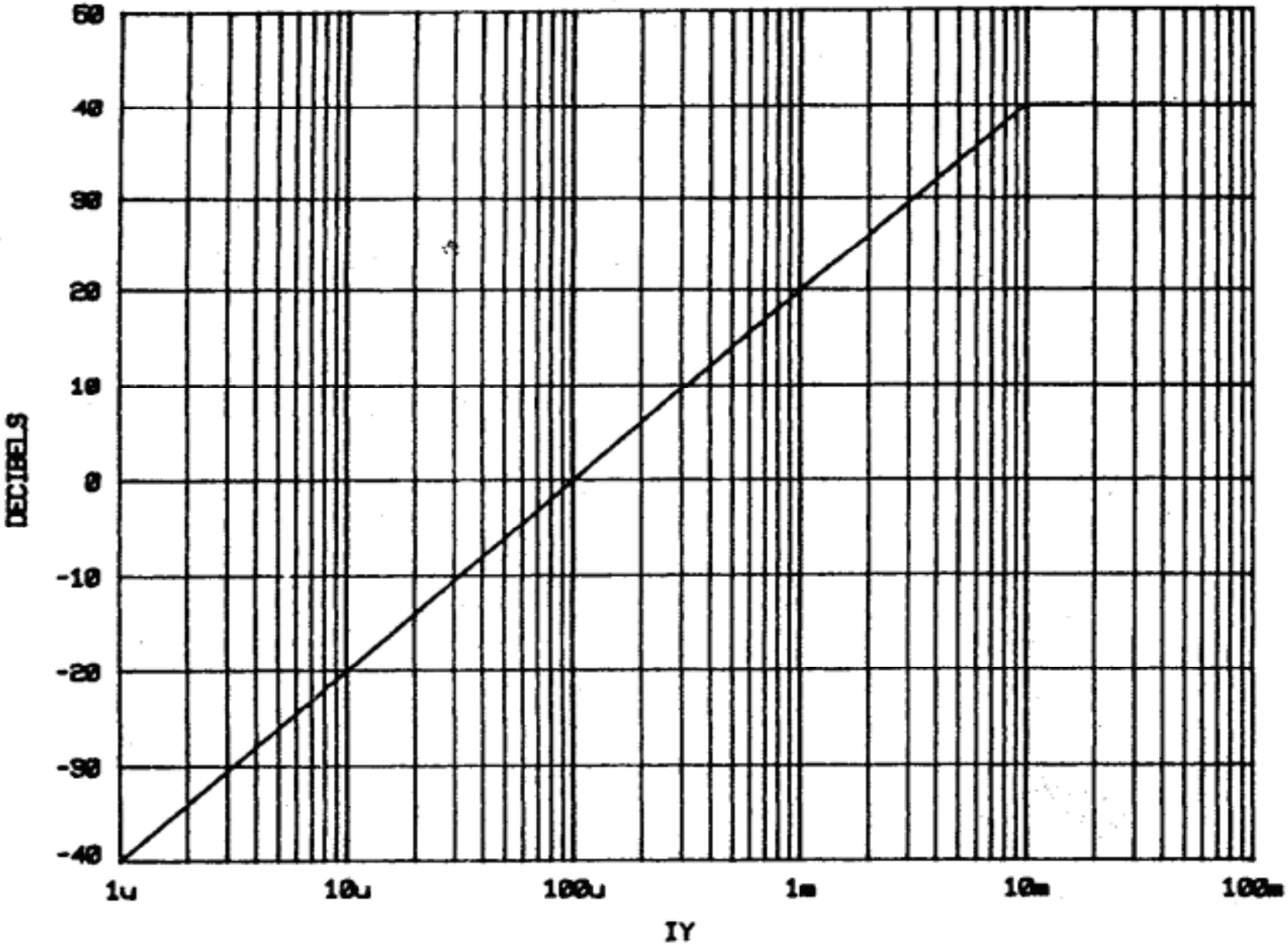


Figure 2.29 Simulation of the current gain of the cell shown in Figure 2.28 for Ix=100μA and β=100; it is exact right up to Iy=βIx.

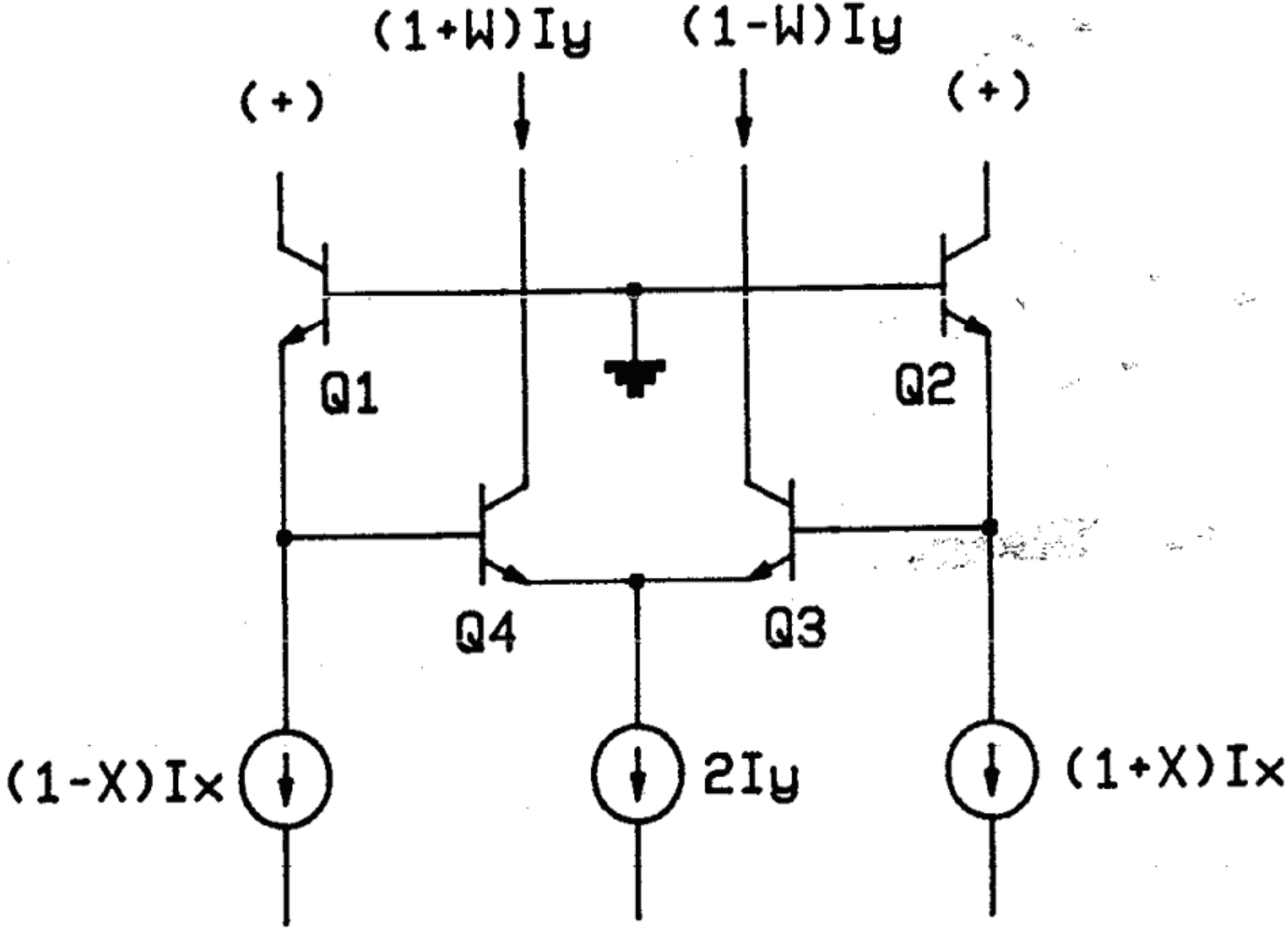
THE BETA-IMMUNE TYPE A CELL

The gain exactly follows the ideal function within -0.1dB – the α error – until $I_Y=I_X$, when it simply limits at +40dB, that is 20logβ. Remember that β=100.

Good performance can be obtained for gains up to β/10.

THE BETA-ALLERGIC TYPE B CELL

It is said *β-allergic* , because the ‘B’ cell doesn’t enjoy the the special beta-immunity of the ‘A’ cell. ‘B’ is not highly allergic, but it is a little more affected by finite beta than its genetically stronger cousin.


(1+W)Iy
(1-W)Iy
(+)
(+)
Q1
Q2
Q4
Q3
(1-X)Ix
2Iy
(1+X)Ix

THE BETA-ALLERGIC TYPE B CELL

$$(1+W)Iy\{(1-X)Ix + \delta(1+W)Iy\} = (1-W)Iy\{(1+X)Ix + \delta(1-W)Iy\}$$

$$W = \frac{X}{1 + 2\delta Iy/Ix}$$

$$Iw = (1 - \delta)(1 + W)Iy - (1 - \delta)(1 - W)Iy = 2XIy \frac{1-\delta}{1 + 2\delta Iy/Ix}$$

As it is obvious, if this cell is to be used in high I_Y/I_X values, some compensation will be necessary. Furthermore, linearity should be considered because of the non-constant denominator.

THE BETA-ALLERGIC TYPE B CELL

Fortunately, in four-quadrant multipliers which use two overlapping ‘B’ cells, nonlinearities in the two half multiplier sections cancel. Also, the ratio I_Y/I_X will usually be unity.

Gilbert gain cell is interesting in that it reuses the input signal, by summing the collector currents of Q_1 and Q_2 to the output.

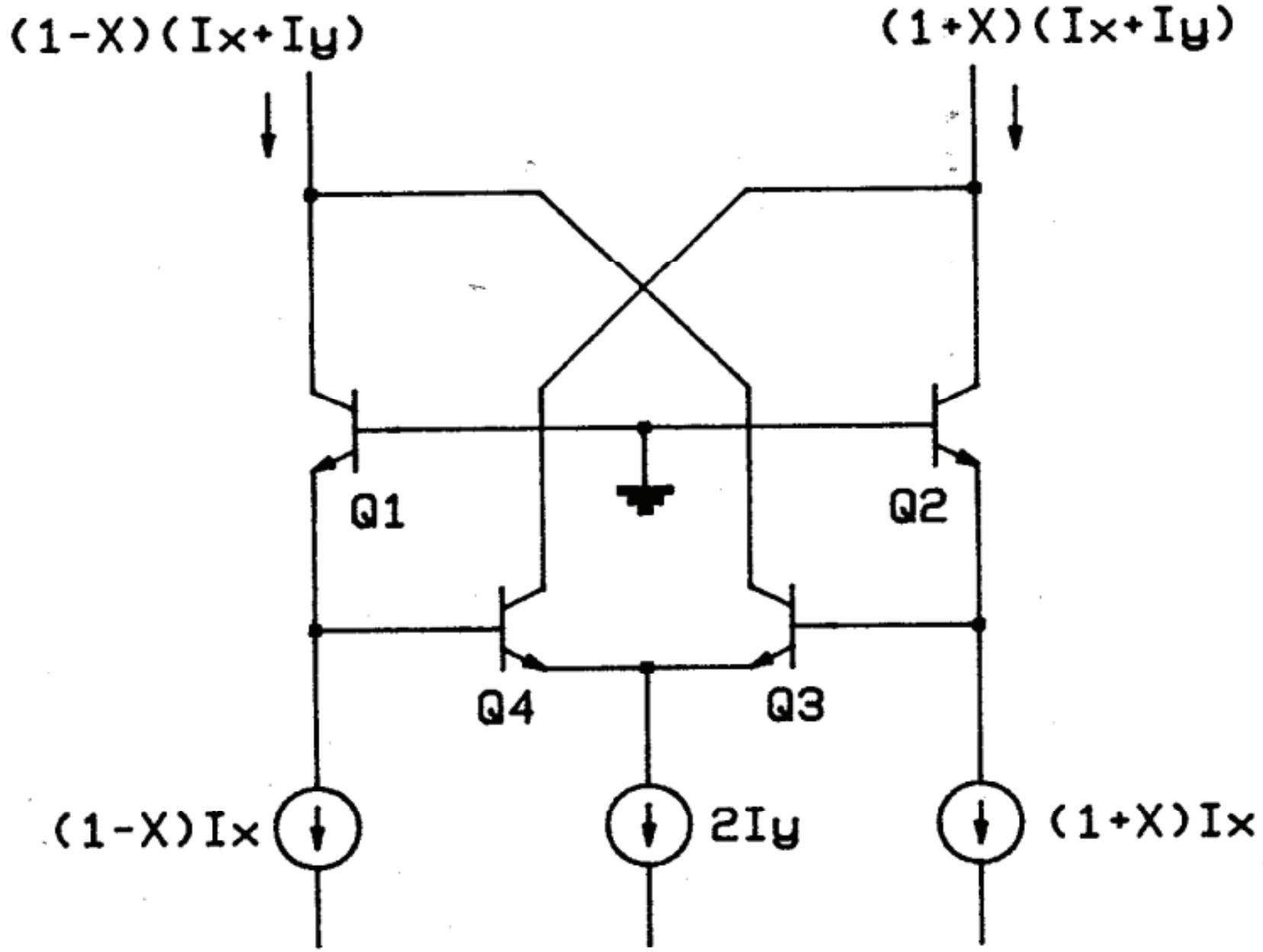


Figure 2.33 The "Gilbert Gain-Cell"; it provides a minimum gain of 1 and a maximum gain which is practically limited by beta to about 10.

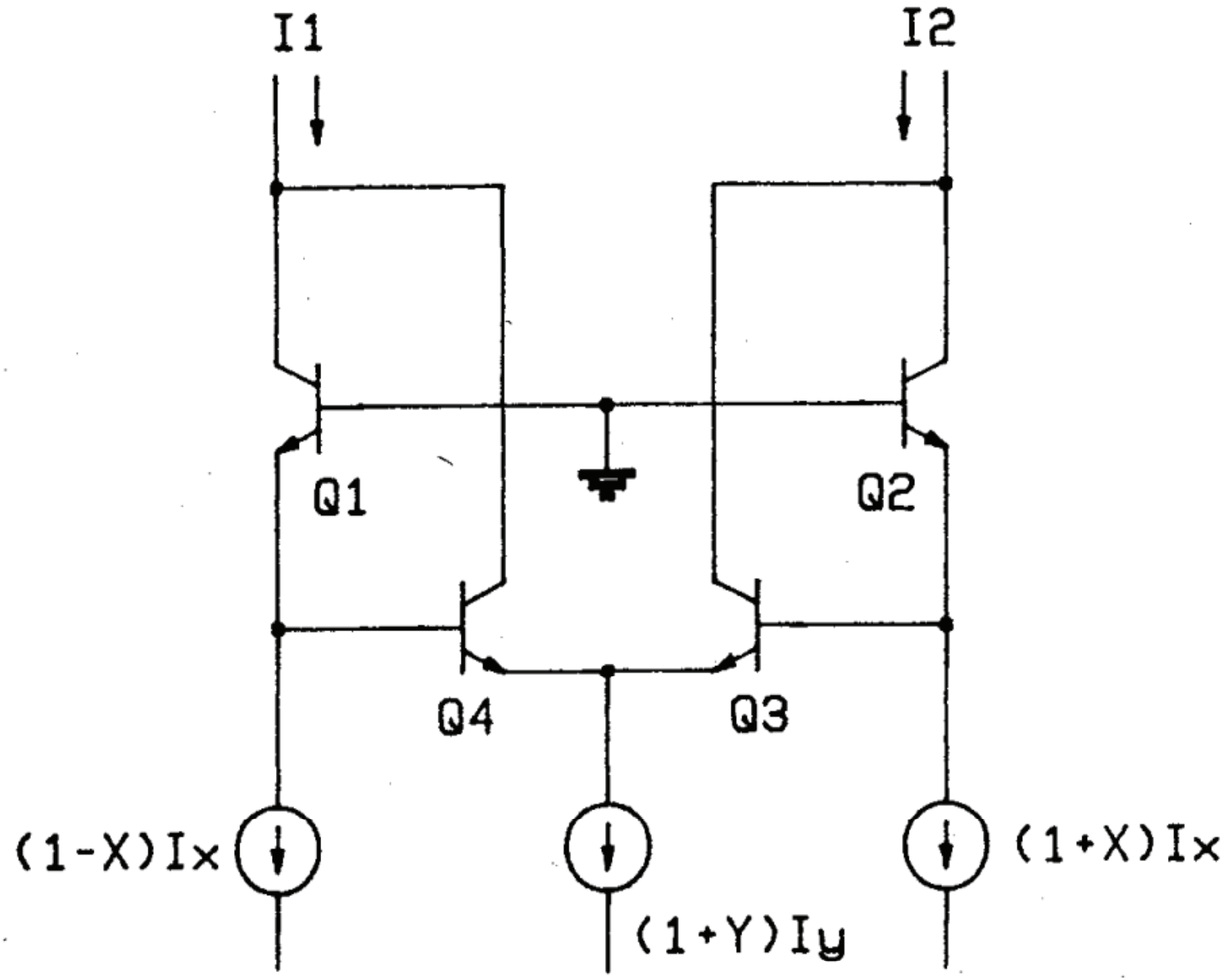


Figure 2.35 A four-quadrant multiplier based on the type 'B' cell; both X and Y can be bipolar.

THE BETA-ALLERGIC TYPE B CELL

In figure 2.35, four quadrant multiplication is performed in an economical and practical way. The tail current to Q_3 and Q_4 varies from 0 to 2Iy as Y varies over its peak range -1 to +1. When Y=-1, the differential output is just $2XI_X$. When Y=0, I_O=0. When Y=1, I_O= $2XI_X$.

This topology is not as accurate as the standart

6-transistor circuit. Moreover, the errors due to ohmic emitter resistance are asymmetric.

DISTORTION MECHANISMS

TL multipliers cells dealt quite thoroughly with the topic of distortion. These are due pimarily to emitter area mismatches, which cause parabolic nonlinearities, thus, even order harmonic distortion. Also finite ohmic resistances introduce cubic nonlinearity, thus odd order distortion. Demonstration of harmonic distortion caused by an emitter area mismatch of 1% is shown in figure 2.36.

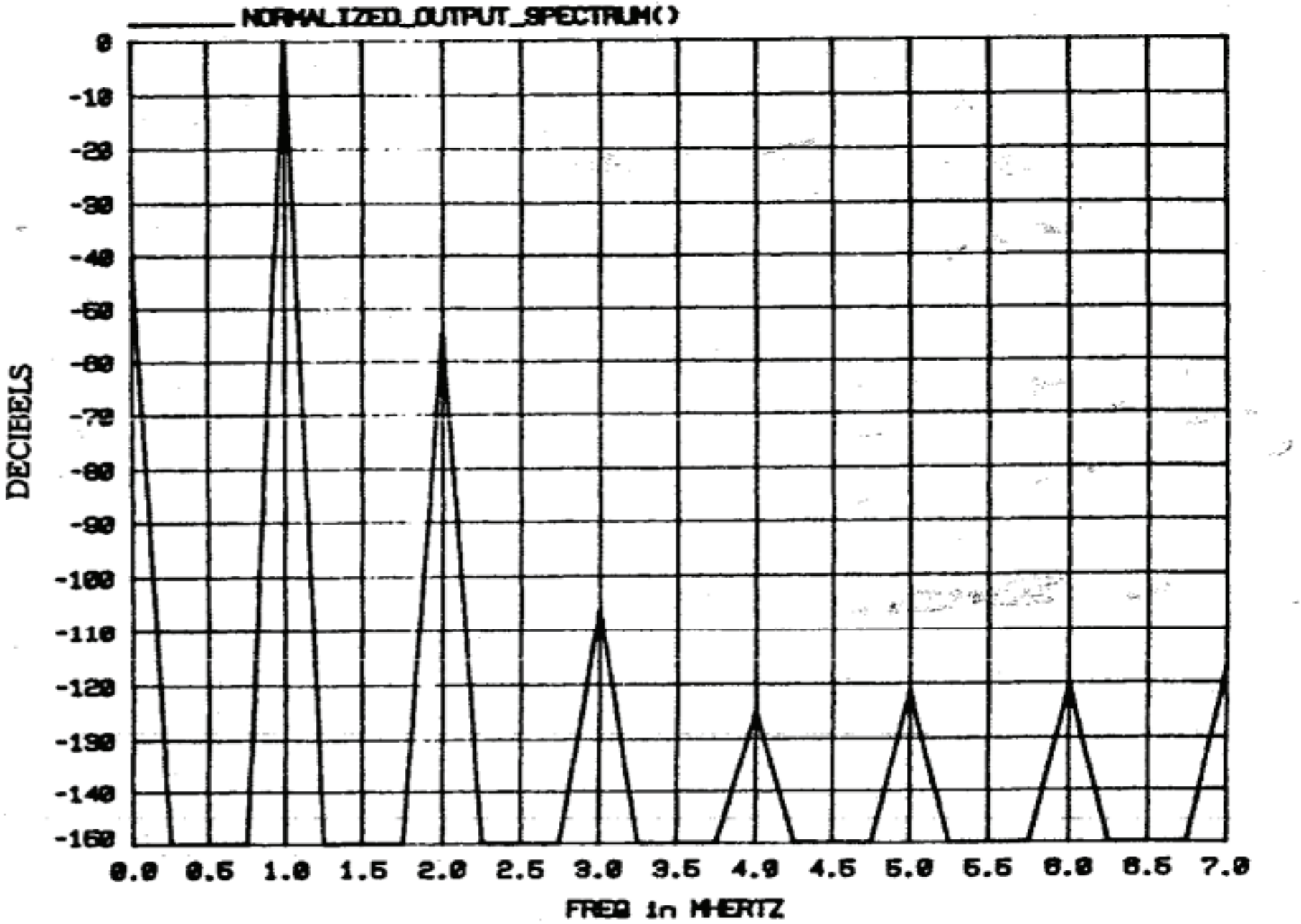


Figure 2.36 Demonstration of harmonic distortion caused by an emitter-area-mismatch of 1%; dominant feature is the -55dB 2nd harmonic.

THE BETA-ALLERGIC TYPE B CELL

Distortion caused by the ohmic emitter resistances of 1Ω will be discussed in figure 2.37.

It is seen that the odd order harmonic distortion is dominant.

In low distortion integrated circuits, lazer trimmed resistances are used as well.

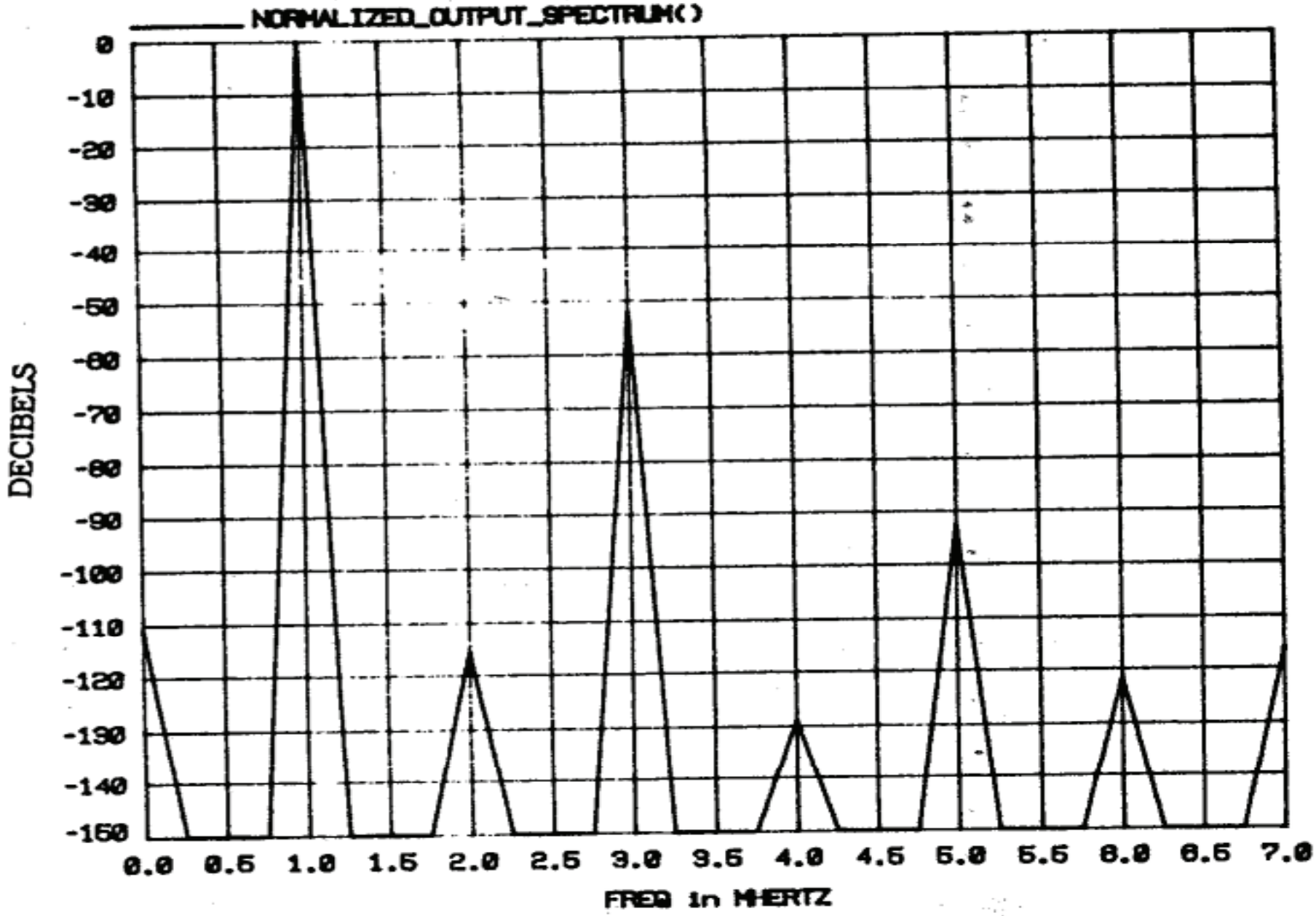


Figure 2.37 Harmonic distortion generated by ohmic resistance (see text for details); dominant feature is the -52dB 3rd harmonic.

THE LOG-ANTILOG MULTIPLIER

BJT multipliers were being designed before the TL principle was formulated and their design was approached from a different viewpoint, by thinking in terms of each transistor as a logarithmic element.

THE LOG-ANTILOG MULTIPLIER

Opamps were used to force collector currents I_X and I_Y in two input devices, and the resulting V_{BE}s summed. A third transistor was forced to operate at a current I_U, and its V_{BE} was subtracted from the sum. Finally this voltage was used as the V_{BE} of a fourth transistor, whose collector current was the output, say I_W.

$$\log Ix + \log Iy = \log Iu + \log Iw$$

THE LOG-ANTILOG MULTIPLIER

$$\log Ix + \log Iy = \log Iu + \log Iw$$

Of course this is nothing different from saying $I_X I_Y = I_U I_W$, just the TL principle!

The TL mulitipliers and the log-antilog ones use absolutely the same principle.

This can be seen by comparing a typical log-antilog embodiment with its TL reduction.

(Figures 2.38 & 2.39)

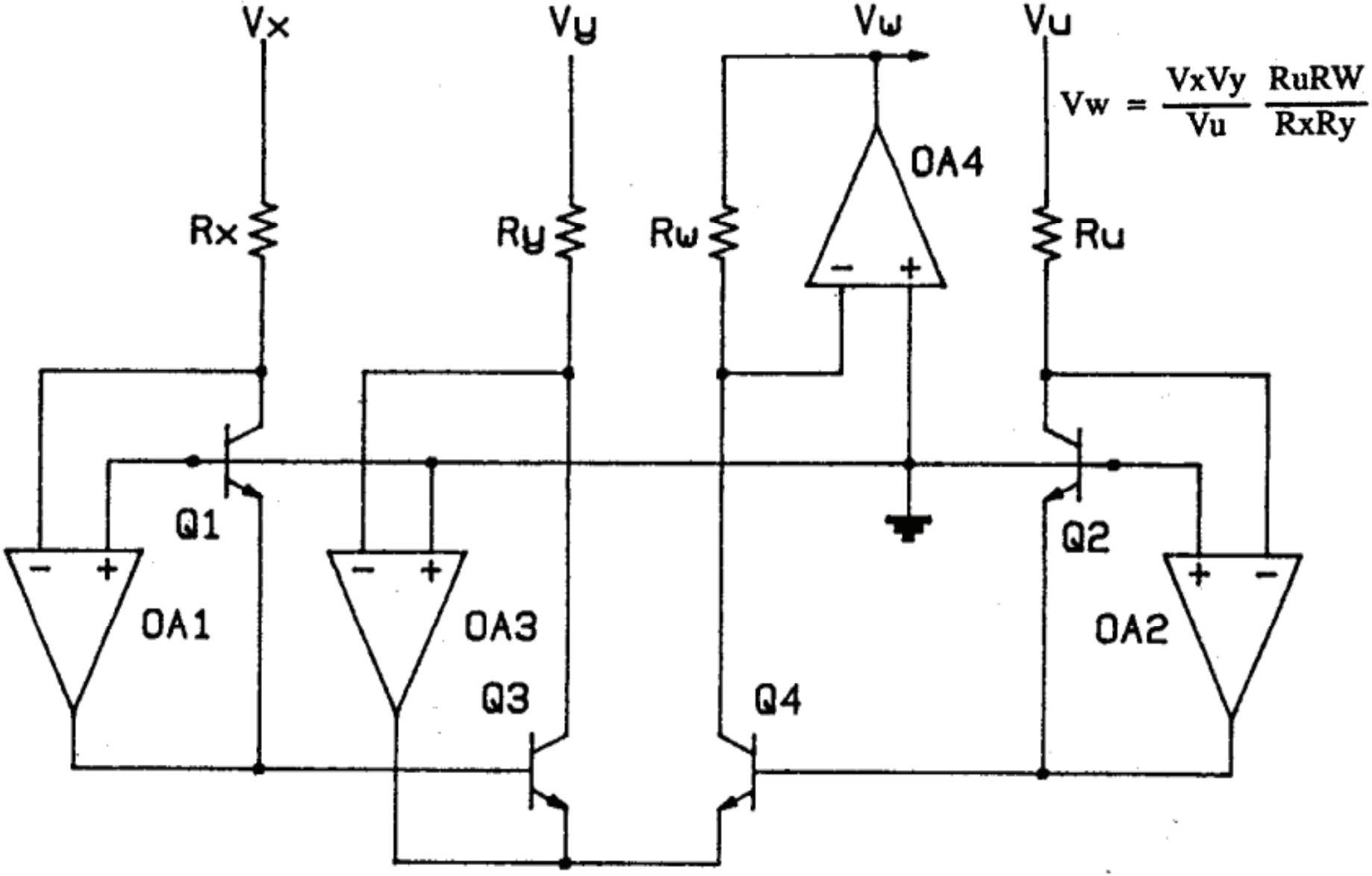


Figure 2.38 The "Log-Antilog" one-quadrant multiplier can also be viewed as a type 'B' cell supported by operational amplifiers.

$$I_W = \frac{I_X \cdot I_Y}{I_U}$$

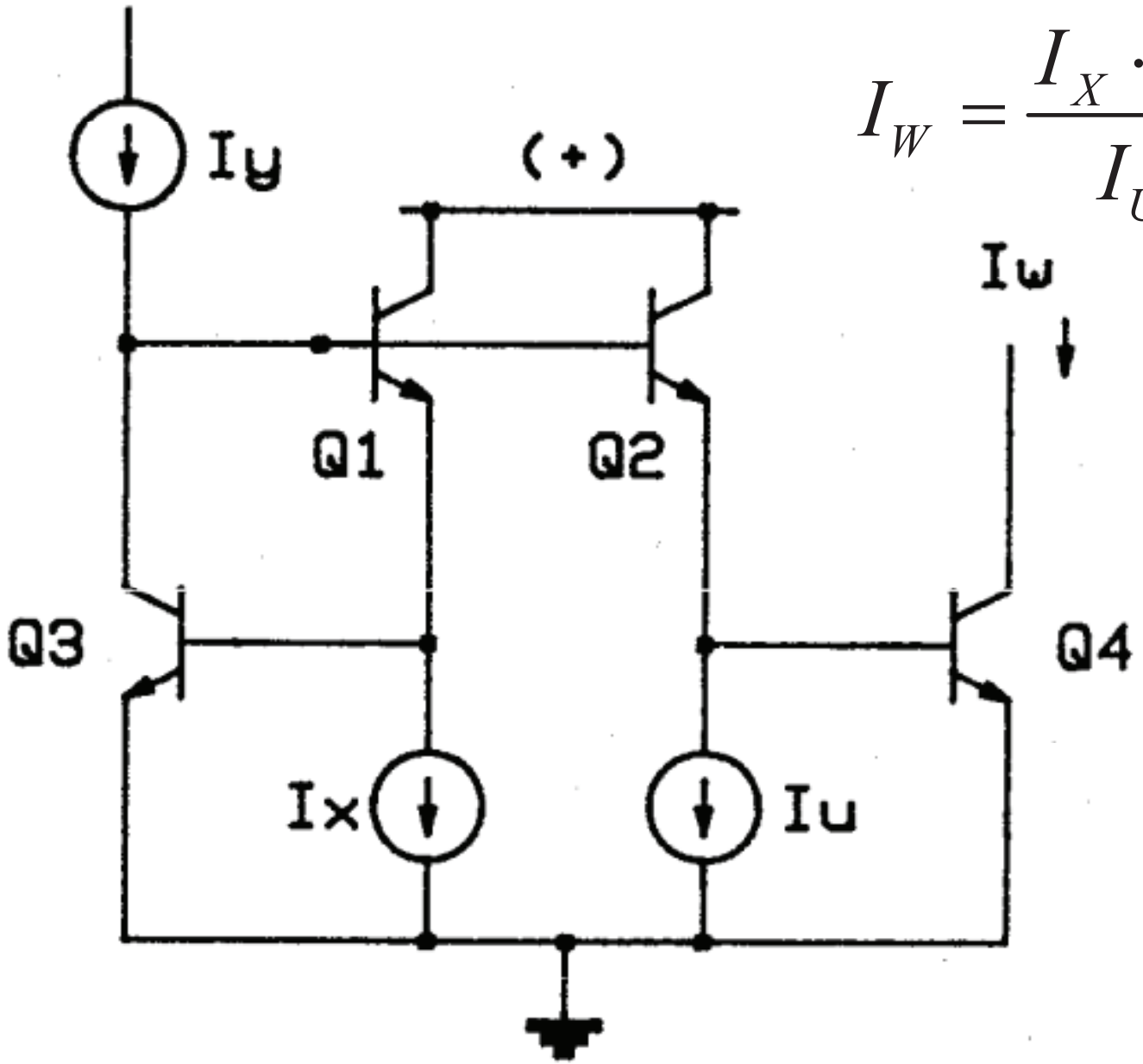


Figure 2.39 The TL reduction of the "Log-Antilog" multiplier.

THE LOG-ANTILOG MULTIPLIER

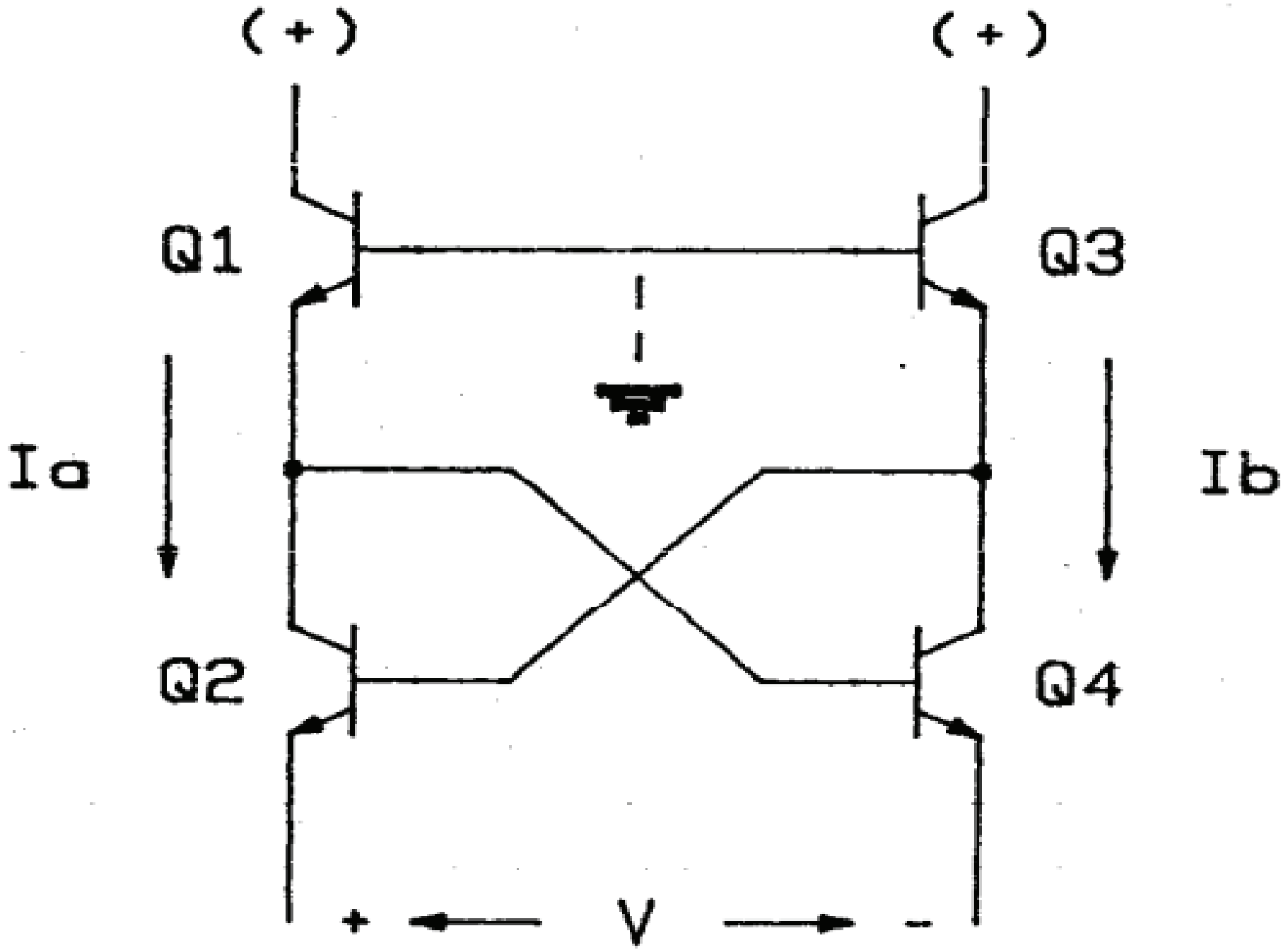
Many products based on this arrangement are available up to 0.05% multiplication error.

However, operation is limited to to one quadrant and the opamps limits the speed!

On the other hand, the TL form can operate very fast. Furthermore it is extremely compact when the signals are form of currents, compared to the one using opamps.

THE TRANSLINEAR CROSS-QUAD

The translinear cross-quad is not a strict-TL in form, the loop is broken making it a TN form. It has many uses by itself and embedded into TL circuits. Figure 2.41 shows the generic cell structure.


(+)
(+)
Q1
Q3
Ia
Ib
Q2
Q4
+
V
-

THE TRANSLINEAR CROSS-QUAD

If V were 0, then we could write the TL equation. Now let's assume V as 0. Then $I_{C1}I_{C4}=I_{C2}I_{C3}$. By neglecting the base currents, it can be written that: $\mathbf{I_{C1}=I_{C2}}$ and $\mathbf{I_{C3}=I_{C4}}$. Then $\mathbf{I_{C1}I_{C4}=I_{C2}I_{C3}}$ will always be valid, that is V=0. If we don't neglect the betas, then we can say:

V always remains very close to 0 even for large ratios of I_a/I_b.

THE TRANSLINEAR CROSS-QUAD

$$V = V_{BE4} + V_{BE1} - V_{BE3} - V_{BE2}$$

$$V_{BE} = V_T \cdot \ln\left(\frac{I_C}{I_S}\right)$$

$$V = V_T \ln\left\{1 + \delta\left(\frac{Ia}{Ib} - \frac{Ib}{Ia}\right)\right\} \sim V_T\,\delta\left(\frac{Ia}{Ib} - \frac{Ib}{Ia}\right)$$

By not neglecting the beta errors, equation above can be written.

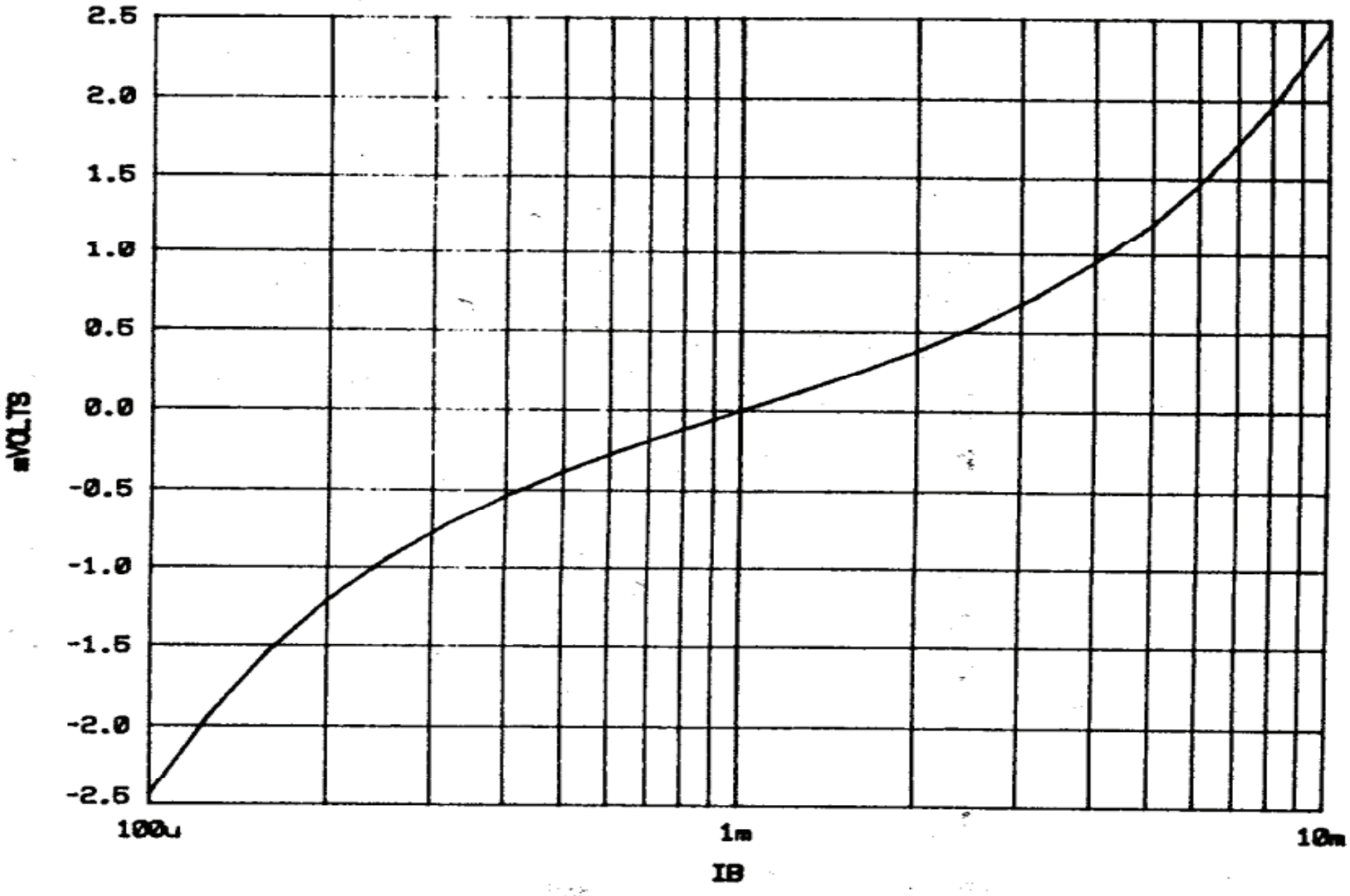
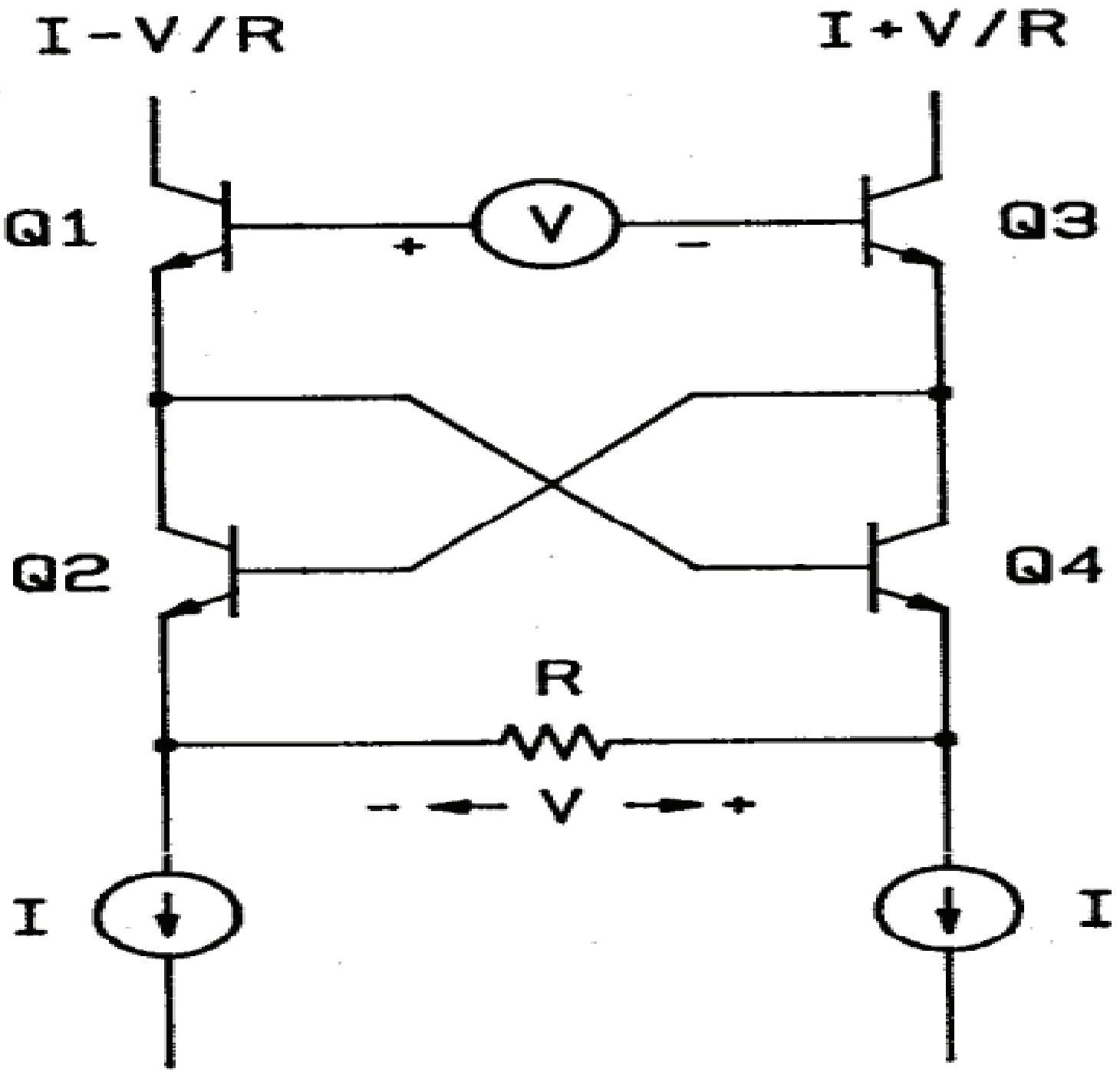


Figure 2.42 Demonstration of the low input voltage of the translinear cross-quad over a 100:1 range in Ib (Ia=1mA, β=100).

CAPRIO'S QUAD

By breaking the loop again, at the bases of Q_1 and Q_3, and applying a voltage source as shown in figure 2.43, we can obtain this voltage across the resistor, R with very small errors, because of the V_{BE} cancellation in the quad.


I-V/R
I+V/R
Q1
V
+
-
Q3
Q2
Q4
R
-
V
+
I
I

CAPRIO'S QUAD

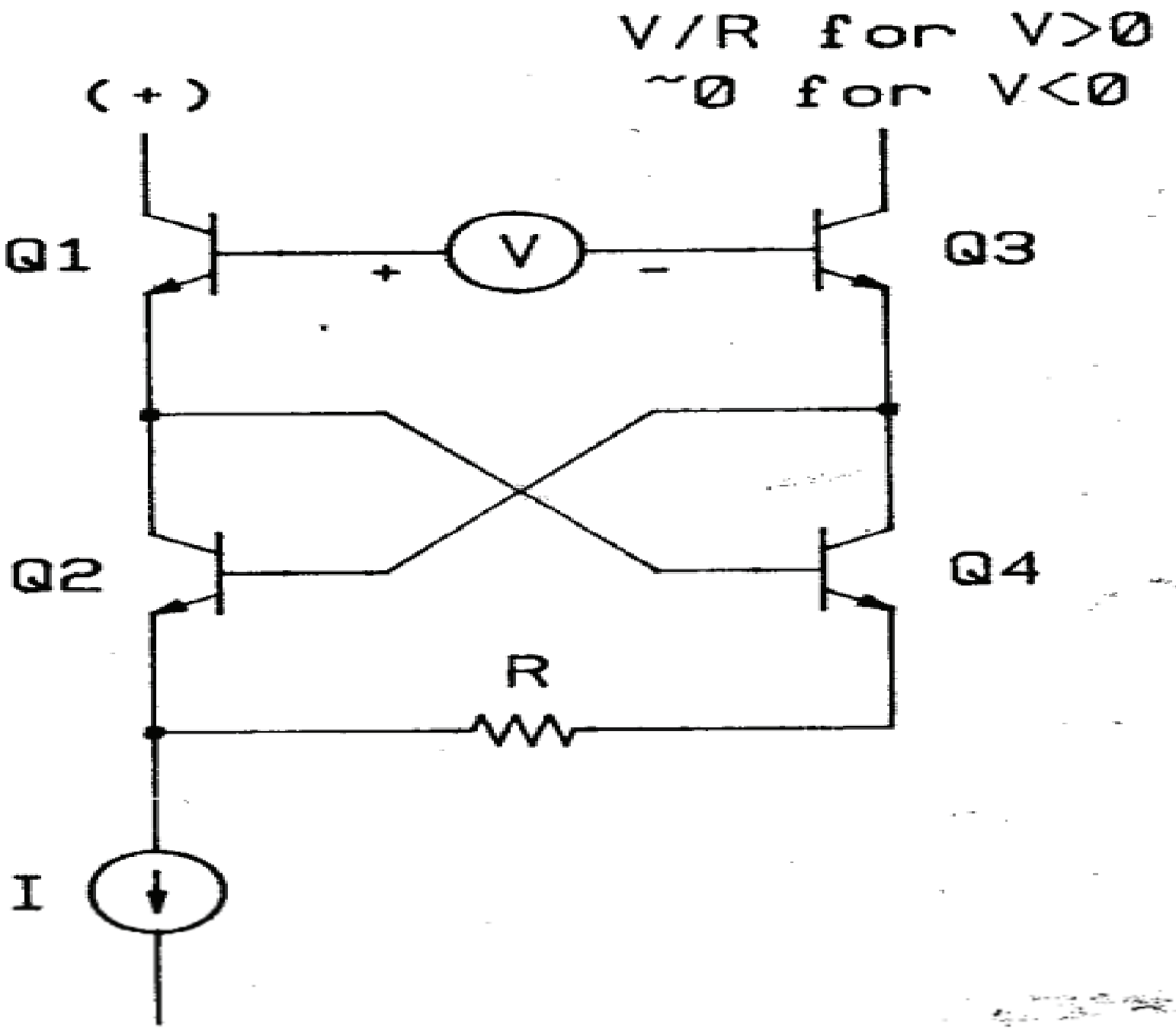
The arrangement has the weakness that:

The voltage swing at the input cannot be large(±400mV at most) because the bias voltages for the collectors of Q2 and Q4 are only one VBE at zero signal and these devices will saturate for large inputs.

LINEAR HALF-WAVE RECTIFIER

By modificating the Caprio's quad, a half wave transconductance rectifier as shown in figure 2.44 can be obtained. When the input voltage is more than about 50mV negative, the output is at its minimum value, which is simply I/β. When the input voltage is 0, most of the bias current continues to flow in the Q1/Q2 branch, but the output will now be slightly larger.

$$V_T \ln\left\{1 + \delta\frac{(2x - 1)}{x(1 - x)}\right\} + xIR = V \qquad Io = I\{\delta + \sqrt{(\delta VT/IR)}\}$$


V/R for V>0
~0 for V<0
(+)
Q1
V
+
−
Q3
Q2
Q4
R
I

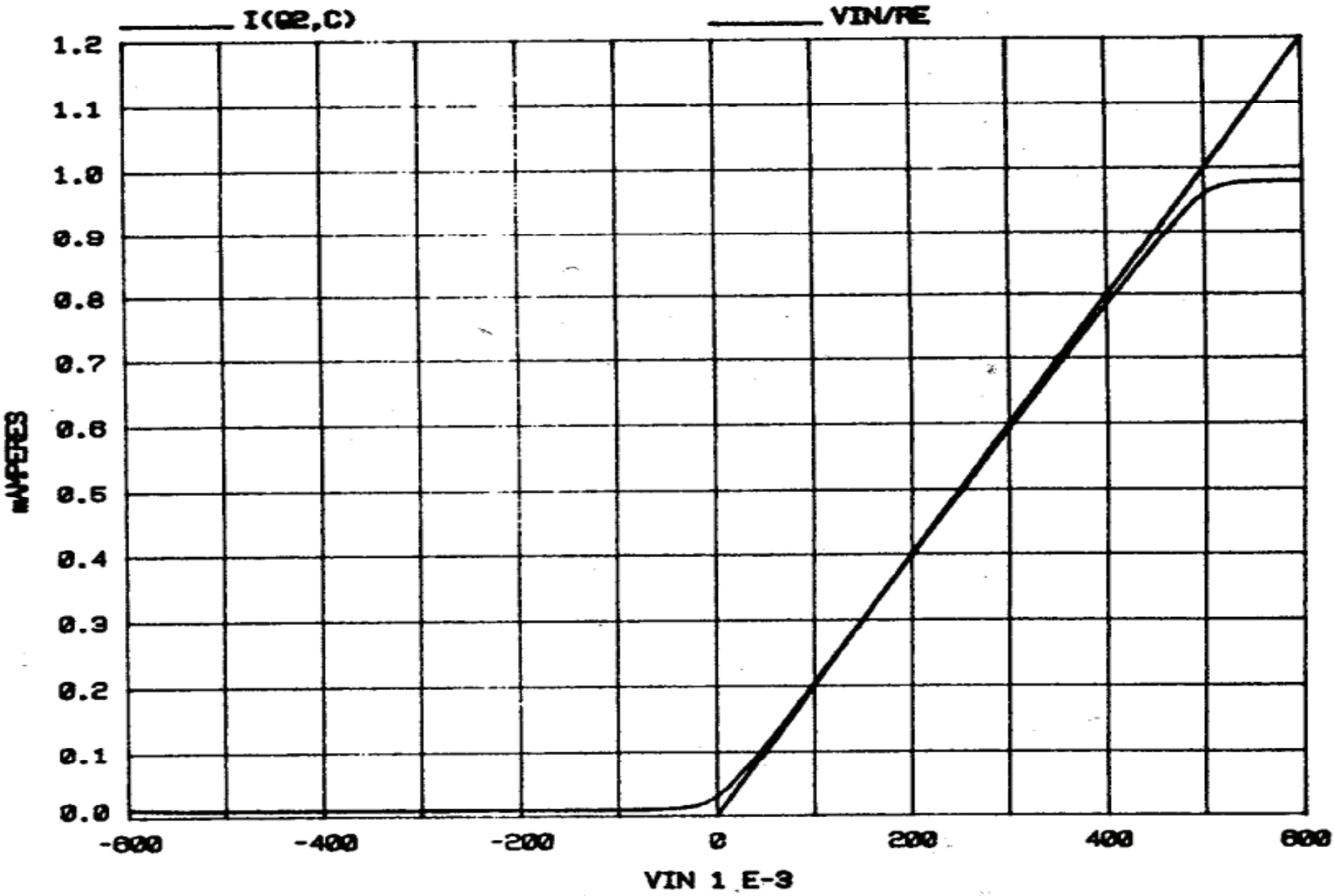


Figure 2.45 Simulated result for the half--wave rectifier; see text for details.

PTAT (DELTA-V_{BE}) CELL

The translinear quad finds common usage in biasing circuits as a delta-VBE cell, for generating voltages or currents proportional to absolute temperature(PTAT).

As V_T=kT/q, the thermal voltage increases proportionally with absolute temperature.

At 20 ^oC, V_T=25.2 mV.

Figure 2.46 shows the PTAT cell.

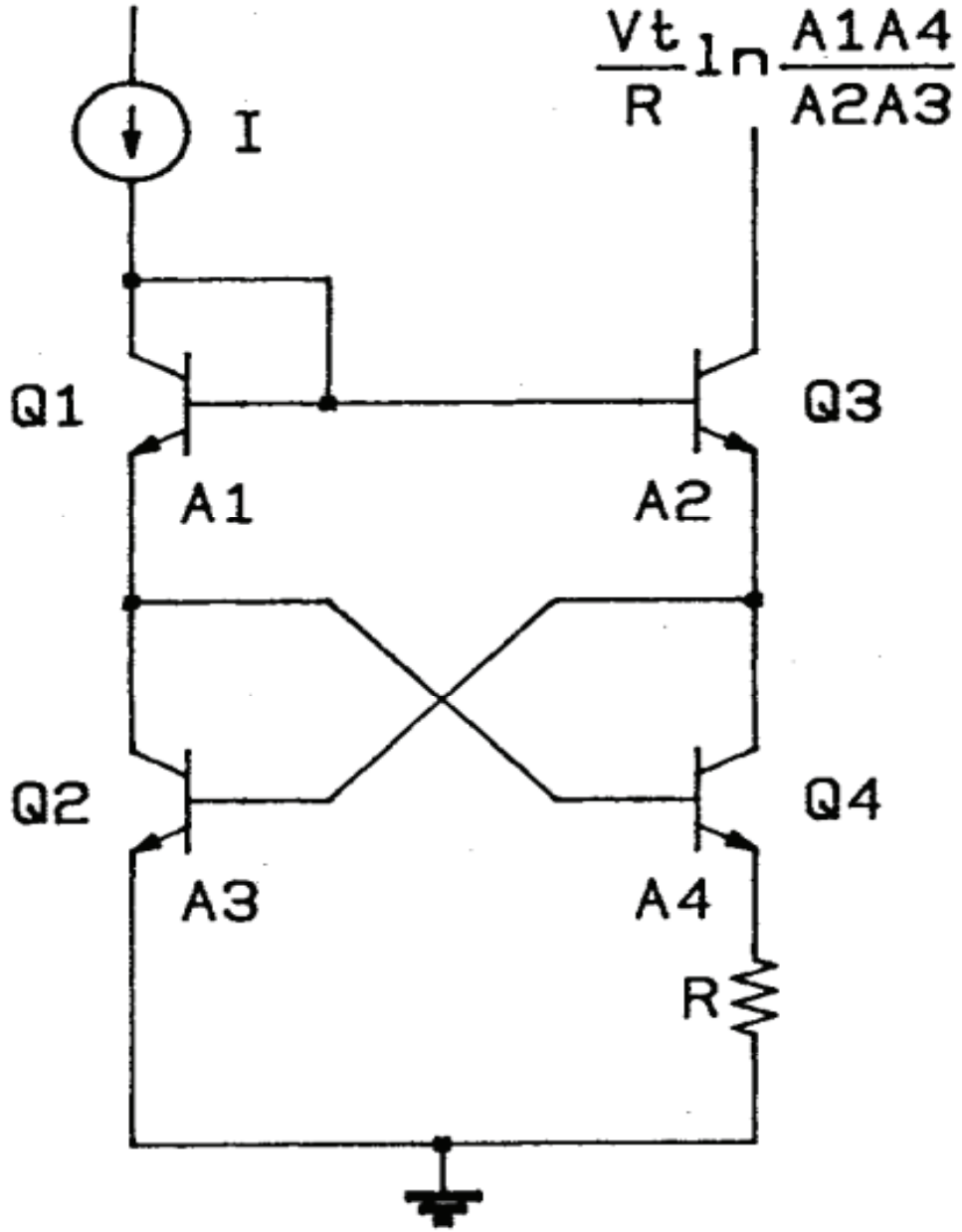


Figure 2.46 Delta-V_{BE} cell using the translinear cross-quad; the bias current I is not critical in determining the PTAT output current.

PTAT (DELTA-V_{BE}) CELL

The output is relatively immune to the bias current, I. By consideration of the TN path:

$$V_R = I_{C3} \cdot R = V_T \ln\left(\frac{A_1 A_4}{A_2 A_3}\right)$$

As seen, output voltage or current is proportional to V_T.

ANOTHER WIDEBAND SQUARER

The translinear cross-quad can be used to generate a virtual ground node so the voltages can be converted into currents with good linearity, in an analogous way to the use of the opamps , but without the speed limitatios of an opamp.

Figure 2.49 shows a two-quadrant squarer based on the translinear cross-quad.

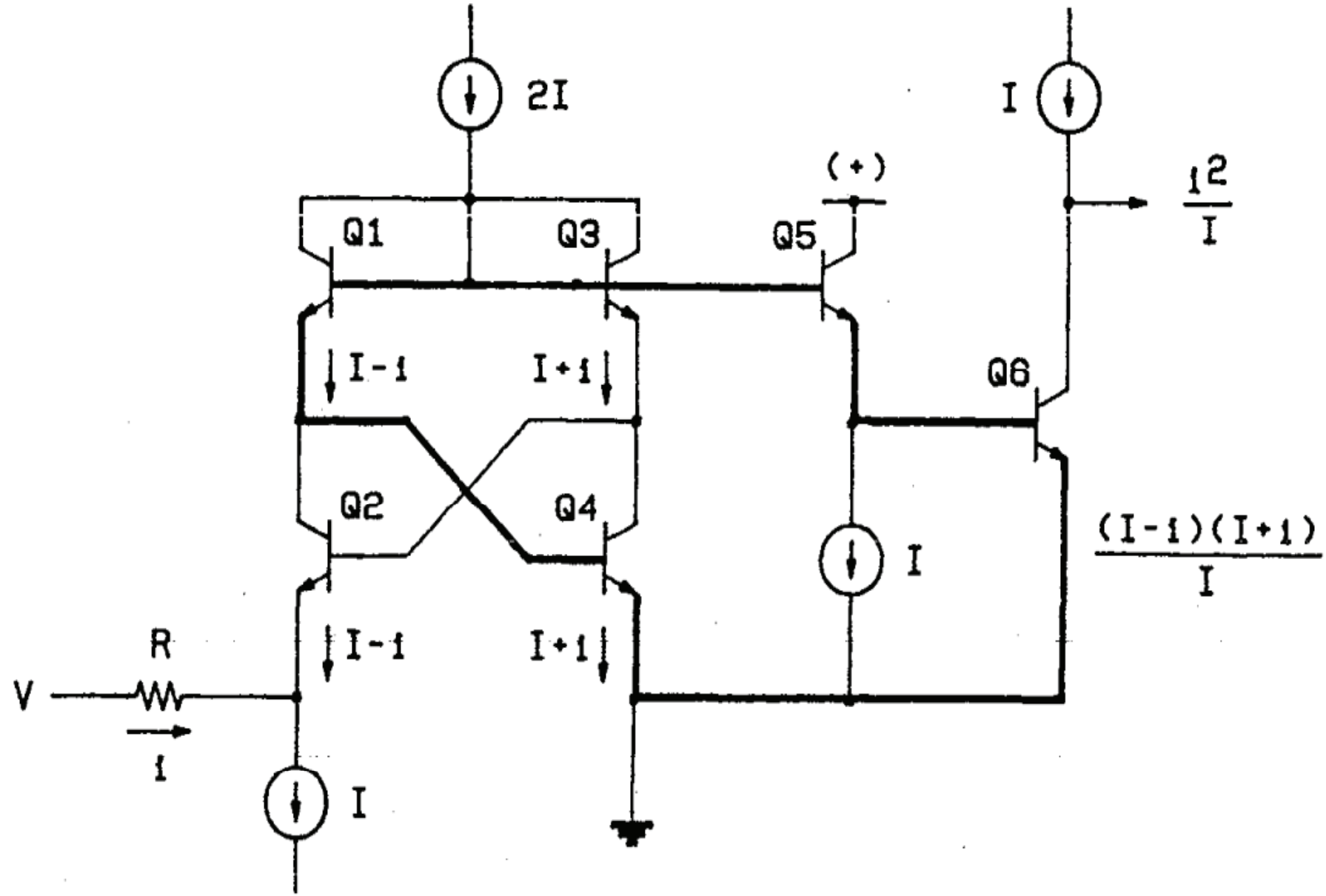


Figure 2.49 A two-quadrant squarer based on the translinear cross-quad, a mixed TN/TL circuit. The heavy line shows the main TL loop.

ANOTHER WIDEBAND SQUARER

From the TN loop (Q_1, Q_2, Q_3, Q_4) :

$I_{C1}= I_{C2}=I-i$ & $I_{C3}= I_{C4}=I+i$ & $i=V/R$ (vir. gnd)

From the TL loop (Q_1, Q_4, Q_5, Q_6) :

$(I-i)(I+i)=I\ I_{C6}$

$I_{C6}=I - i^2/I$

$I_O=I - I_{C6}=i^2/I$

ANOTHER TWO-QUADRANT MULTIPLIER

A further application of the TL cross-quad is shown in figure 2.50. The TN path (Q_1, Q_2, Q_5, Q_6) performs the V-I conversion by creating a virtual ground node. And a differential output current($I_O=I_3-I_4$) is created by using the TL loop(Q_1, Q_2, Q_3, Q_4). By constructing two equations from these loops, the multiplier circuit can be easily analysed.

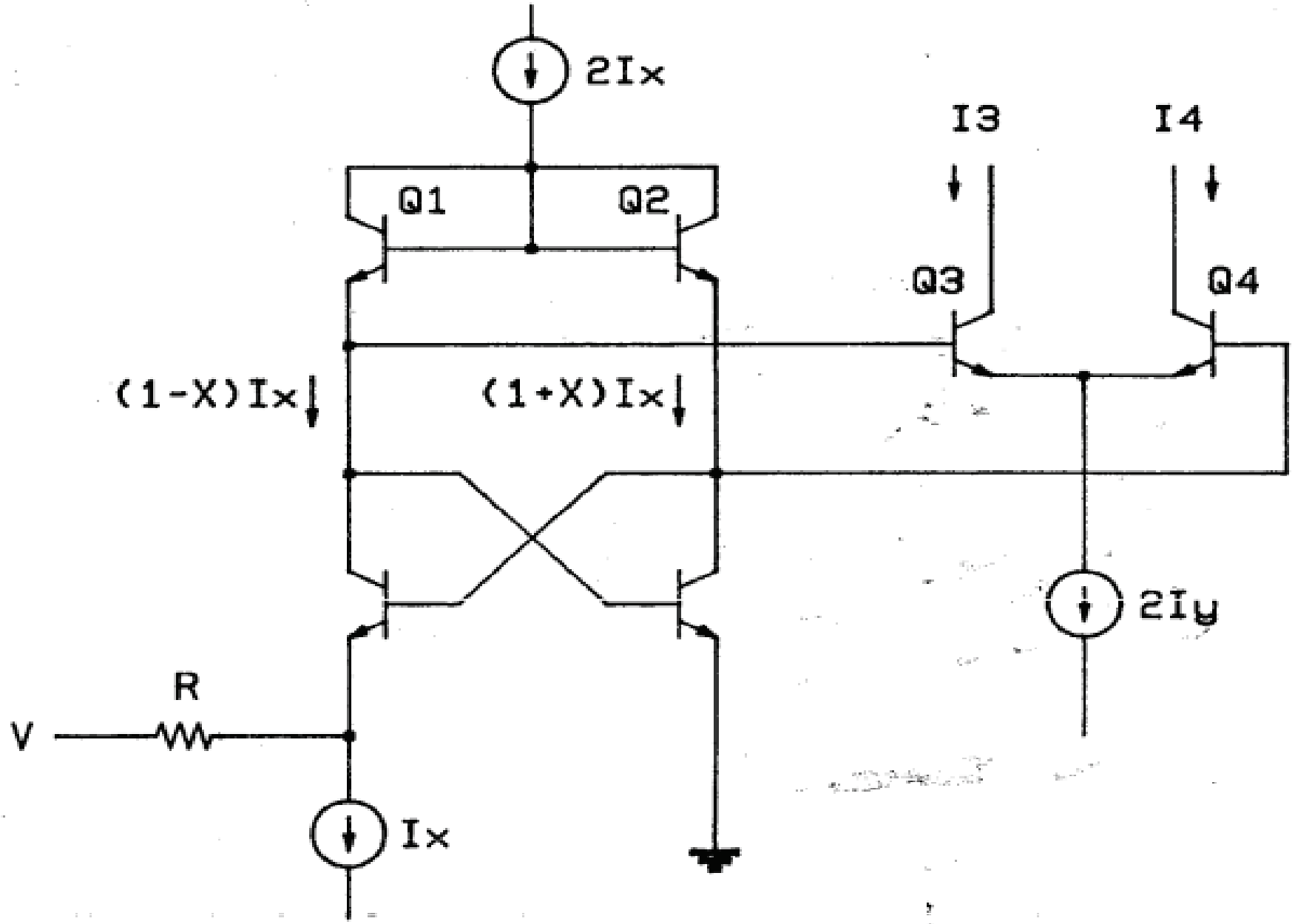


Figure 2.50 A two-quadrant multiplier based on the translinear cross-quad, another example of mixed TN/TL concepts.

ANOTHER TWO-QUADRANT MULTIPLIER

From the TN loop (Q_1, Q_2, Q_5, Q_6) :

$I_{C1}= I_{C6}=I-i$ & $I_{C2}= I_{C5}=I+i$ & $i=V/R$ (vir. gnd)

From the TL loop (Q_1, Q_4, Q_5, Q_6) :

$I_{C2}I_{C4}=I_{C1}I_{C3}$ ⇒ $(I_X+i)(2I_Y-I_{C3})=(I_X-i)I_{C3}$

$$I_{C3} = \left(\frac{I_Y}{I_X} \right) \cdot i + I_Y \qquad I_{C4}=2I_Y-I_{C3}$$

So $I_O=I_{C3}-I_{C4}=2\dfrac{I_Y}{I_X}\cdot i$

References:

[1] C. Toumazou, F.J. Lidgey, D.G. Haigh (ed.), Analog IC design: the current-mode approach, Peter Peregrinus Ltd., 1998.

Thanks…