Nth-Order Current Transfer Function Synthesis Using a High-Performance Electronically Tunable Current Conveyor

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Introduction

- A well-known current-mode circuit is the second generation current conveyor (CCII) [1]. Current conveyors are widely used by analog designers especially as basic building blocks for filters.
- When designing filters, it is desirable to vary the filter coefficients electronically.
- Although operational transconductance amplifiers (OTAs) can be used to perform the tuning, the nonvirtually zero voltage which exist between the input terminals of the OTAs is a considerable drawback in filter design.
- The concept of the electronically tunable current conveyor (ECCII) was first proposed by Senani [2] using operational amplifier (OA) and operational transconductance amplifier (OTA). Then the ECCII was designed and realized in both CMOS and Bipolar technology.
- In [3] (our reference article by Hakan Kuntman, Shahram Minaei, Onur Korhan Sayin), a general circuit configuration for realizing *n*th-order current transfer function is derived using a novel CMOS implementation of the ECCII based on an improved active-feedback cascode current mirror.

The ECCII (Electronically Tunable Current Conveyor)

- The terminal relations of an ideal ECCII, with its electrical symbol as shown in Figure 1.

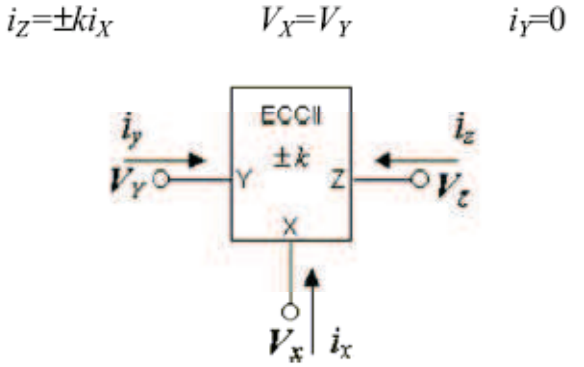

Figure 1. Electrical symbol of the ECCII.

- According to this equation an ECCII has a unity voltage gain (voltage follower) between terminals Y and X and a tunable $\pm k$ current gain between terminals X and Z. The plus and minus signs of k denote positive (ECCII+) and negative (ECCII-) type conveyors, respectively.

The ECCII (Electronically Tunable Current Conveyor)

- It is possible to represent an ECCII using an OA and a small signal current amplifier as shown in Figure 2 [4].

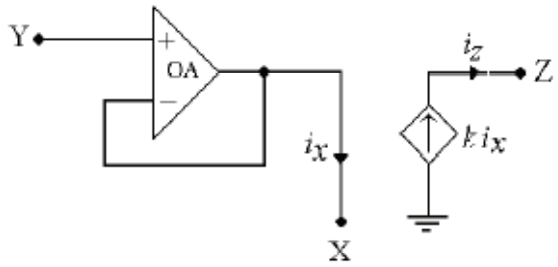

Figure 2. Implementation of an ideal ECCII.

- The Y and Z terminals have a high impedance level, ideally infinite, whereas X terminal shows a low impedance level, ideally zero.

CMOS implementation of ECCII+

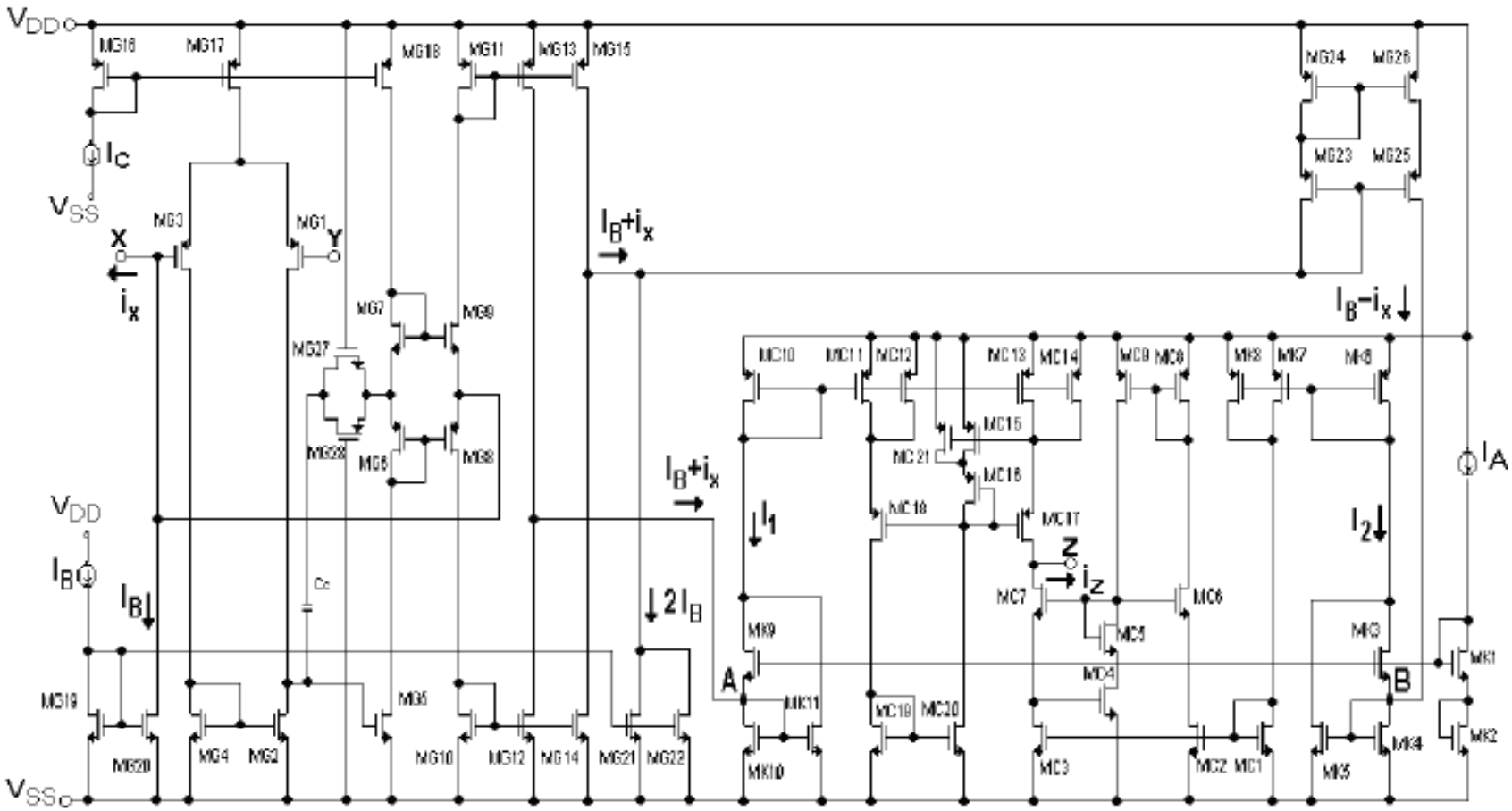

Figure 3. The proposed high performance ECCII+.

CMOS implementation of ECCII+

- The first part of the circuit is a two-stage class AB high performance OA composed of transistors MG1-MG9, MG16-MG17 and compensation network (transistors MG27-MG28 and capacitor *C*). The unity voltage transfer function Vx/Vy is ensured by the differential pair MG1-MG3.
- The feedback connection at X node provides the low impedance terminal. Using current mirrors of (MG11, MG13, MG10, MG12), (MG19, MG21, MG22) and (MG23, MG24, MG25, MG26) the currents IB+Ix and IB-Ix are transferred to the input terminals of the small signal current amplifier circuit A and B, respectively.
- The second part of the proposed ECCII+ circuit is the small signal current amplifier constructed with high performance current mirrors known as improved active-feedback cascode current mirrors (IAFCCM) [5] in its output stage.

CMOS implementation of ECCII+

- The output resistance at terminal Z of the proposed ECCII

$$Z_z = \left[g_{m_{MC7}} g_{m_{MC4}} r_{ds_{MC3}} r_{ds_{MC7}} (r_{ds_{MC4}} // r_{ds_{MC9}}) \right] // \left[g_{m_{MC17}} (g_{m_{MC15}} + g_{m_{MC21}}) r_{ds_{MC17}} (r_{ds_{MC13}} // r_{ds_{MC14}}) (r_{ds_{MC15}} // r_{ds_{MC21}} // r_{ds_{MC20}}) \right]$$

- The output current of the circuit *Iz* can be calculated as

$$i_z = 2I_1 - 2I_2 = \left(\frac{I_B}{I_A} \right) i_x = k.i_x \qquad k = I_B / I_A$$

- The small signal current gain (k) of the amplifier and can be controlled electronically by means of DC bias currents *IA* and *IB*

Nth-Order Current Transfer Function Synthesis

- A synthesis method for the realization of tunable *n*th-order current transfer function is proposed[6]. The proposed method is based on realizing the *n*thorder current transfer function using a signal flowgraph and then obtaining, from the graph, the active- RC circuit involving positive and negative ECCIIs.
- Let the *n*th-order current transfer function be expressed as

$$T(s) = \frac{I_{out}}{I_{in}} = \frac{a_n s^n + a_{n-1} s^{n-1} + \ldots\ldots\ldots + a_1 s + a_0}{s^n + b_{n-1} s^{n-1} + \ldots\ldots\ldots\ldots + b_1 s + b_0}$$

Nth-Order Current Transfer Function Synthesis

- The signal flow-graph model for realizing the transfer function $T(s)$ is shown in Figure 4. This may be easily verified using the well-known Mason gain formula.

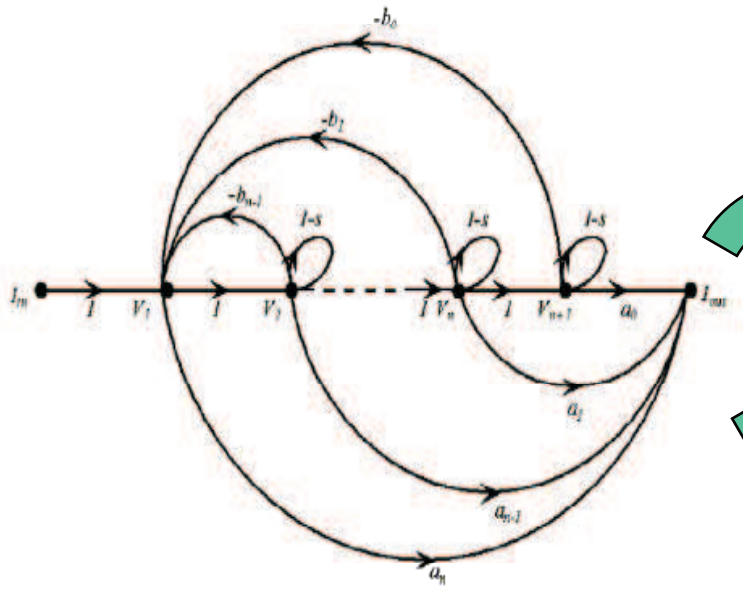

Figure 4. Signal flow-graph representing $T(s)$

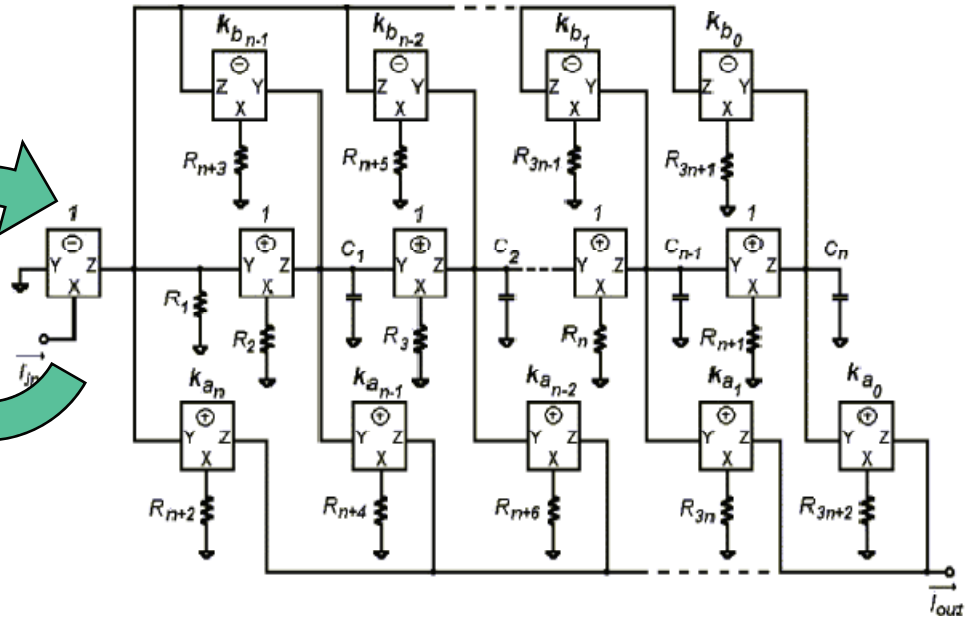

Figure 5. Implementation of T(s)

Nth-Order Current Transfer Function Synthesis

- The circuit of Figure 5 includes 3n+2 ECCIIs, 3n+2 resistors and n grounded capacitors. All of the resistors and capacitors in the proposed circuit are grounded which is attractive for integrated circuit implementation. The current transfer function $T(s)$ of the circuit can be found as:

$$T(s)=\frac{I_{out}}{I_{in}}=\frac{k_{a_n}s^n\left(\frac{R_1}{R_{n+2}}\right)+k_{a_{n-1}}s^{n-1}\left(\frac{R_1}{R_{n+4}R_2C_1}\right)+k_{a_{n-2}}s^{n-2}\left(\frac{R_1}{R_{n+6}R_2R_3C_1C_2}\right)+..+k_{a_0}\left(\frac{R_1}{R_{3n+2}(R_2..R_{n+1})(C_1..C_n)}\right)}{s^n+k_{b_{n-1}}s^{n-1}\left(\frac{R_1}{R_{n+3}R_2C_1}\right)+k_{b_{n-2}}s^{n-2}\left(\frac{R_1}{R_{n+5}R_2R_3C_1C_2}\right)+...+k_{b_0}\left(\frac{R_1}{R_{3n+1}(R_2....R_{n+1})(C_1....C_n)}\right)}$$

An Example (Second Order Filter)

- The second order generalized transfer function is given;

$$T(s)=\frac{I_{out}}{I_{in}}=\frac{k_{a_2}\left(\frac{R_1}{R_4}\right)s^2+k_{a_1}\left(\frac{R_1}{R_6R_2C_1}\right)s+k_{a_0}\left(\frac{R_1}{R_8R_2R_3C_1C_2}\right)}{s^2+k_{b_1}\left(\frac{R_1}{R_5R_2C_1}\right)s+k_{b_0}\left(\frac{R_1}{R_7R_2R_3C_1C_2}\right)}$$

- The ωo and Q parameters of the filter are obtained as;

$$\omega_o=\sqrt{\frac{k_{bo}R_1}{R_7R_2R_3C_1C_2}}$$

$$Q=\frac{R_5}{k_{b1}}\sqrt{\frac{k_{bo}R_2C_1}{R_1R_7R_3C_2}}$$

It can be seen that the parameter ωo can be tuned electronically by adjusting k_{bo}. By keeping the value of k_{bo} constant and varying k_{b1} the parameter Q can also be tuned.

An Example (Second Order Filter) - Realization

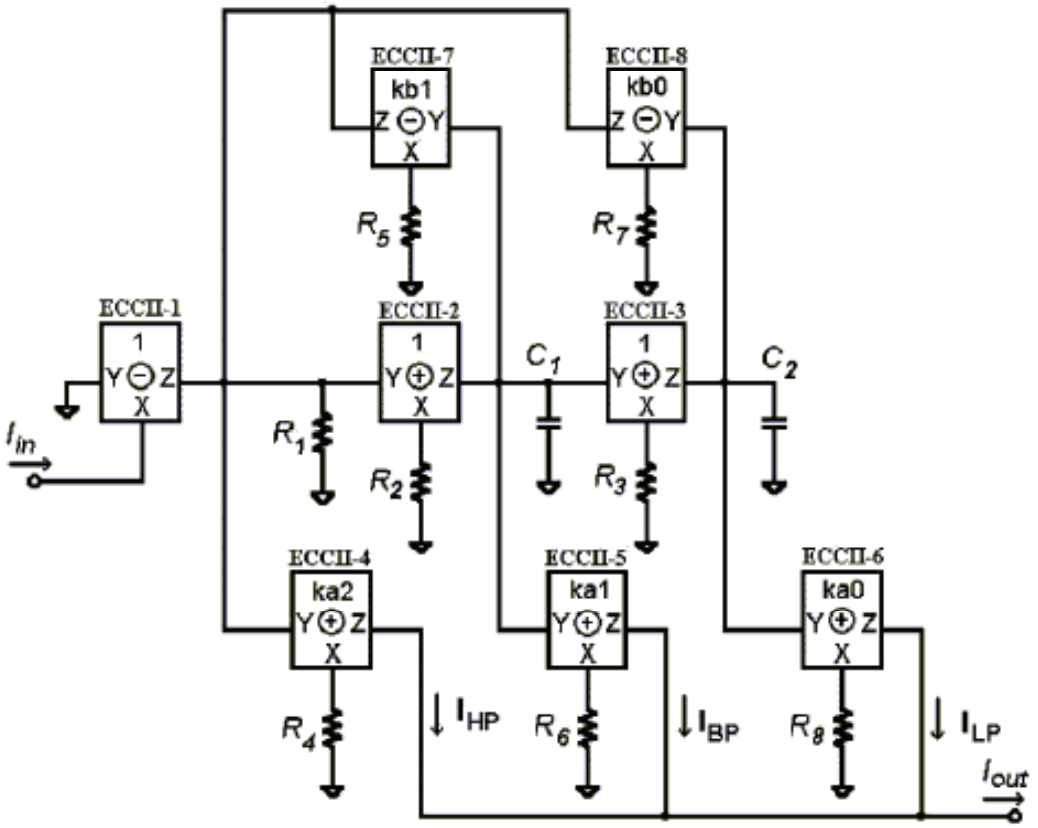

Figure 6. Second-order current-mode filter realization

An Example (Second Order Filter) - Results

- The second order filter has been simulated using SPICE circuit simulation program. For the ECCIIs the schematic implementation shown in Figure 3 with a DC supply voltage ±2.5V has been used.
- The biasing currents are selected as $I_A = I_B$ = 50μA which results in a current gain of unity for the ECCIIs. Also the biasing current I_C =100μA and compensation capacitor C_C = 1pF are selected. Transistors are simulated using 0.5μm MIETEC CMOS technology.

An Example (Second Order Filter) - Results

- The passive elements have been selected as: R_i=25kΩ (i=1,2…8), C_1=C_2=42pF to obtain the lowpass, bandpass and highpass responses with a natural pole frequency of f_0=151kHz and a pole quality factor of Q=1.
- Transistor aspect ratios are shown in the table.

.1 Transistor	W/L (μm)
MG1, MG3	67.5/1
MG2, MG4	12.5/1
MG6, MG8	100/2
MG5, MG7, MG9-MG28, MC1-MC21, MK6-MK8	40/2
MK1-MK5, MK9-MK11	50/1

Table 1. Transistor dimensions of the ECCII.

An Example (Second Order Filter) - Results

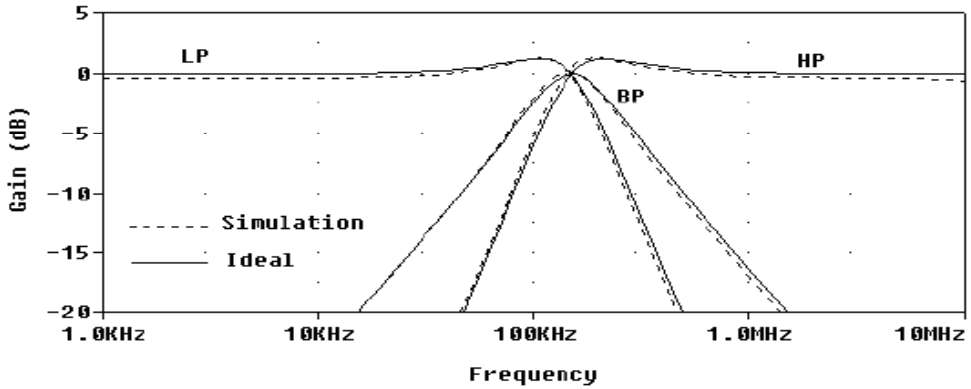

Figure 7. The frequency responses of the second-order current-mode filter.

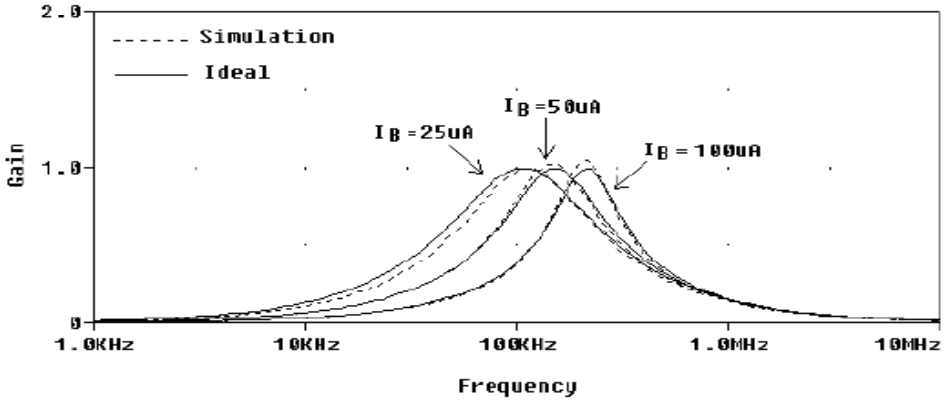

Figure 8. Tuning of the natural frequency of the band-pass response.

References

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- [2] R. Senani, "Novel circuit implementation of current conveyors using an OA and an OTA", *Elect. Lett.*, 16, pp. 2-3, 1980
- [3] . Minaei, O. K. Sayin, H. Kuntman, 'Nth-Order Current Transfer Function Synthesis Using a High-Performance Electronically Tunable Current Conveyor' Proceedings of MELECON'06: The 13th IEEE Mediterranean Electrotechnical Conference, pp.15-18, 16-19 May 2006
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- [6] G. Ferri, and N.C. Guerrini, "Low-Voltage Low-Power CMOS Current Conveyor", *Kluwer Academic Publishers, Boston* 2003.