Novel High Precision Current-mode Multiplier/Divider

S. Menekay, R.C. Tarcan, H. Kuntman

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Prof. Dr. Hakan Kuntman

Nazan İltüzer

504081217

INTRODUCTION

- In this paper, a method to reduce the second order effects on the circuit performances caused by the small sized MOS transistors is proposed and a squarer/divider circuit is designed using this method.

INTRODUCTION

- **Due to the decrease in dimensions of MOS transistor in IC fabrication technology**

- the MOS transistor voltage–current relationship deviates from square-law.
- second order effects like short channel effect cause more errors in the MOSFET performance.

INTRODUCTION

- In this paper, a **method** is proposed to reduce the errors generated by the second order effects in the current-mode circuits with using MOS translinear loop.
- The output current function of the proposed circuit can be controlled by a control voltage.
- The proposed method enables the use of much smaller transistors and the circuits to be designed are smaller than their counterparts. Thus they may be operated at much higher frequencies.

INTRODUCTION

- **Where is the proposed circuit can be used?**

- filtering in square-root domain,
- fuzzy logic controllers,
- artificial neural networks,
- modulators,
- phase discriminators,
- adaptive filters,
- RMS-DC converters,
- sine/cosine synthesizers,
- cryptography systems, etc.

Current-mode multiplier/divider circuit

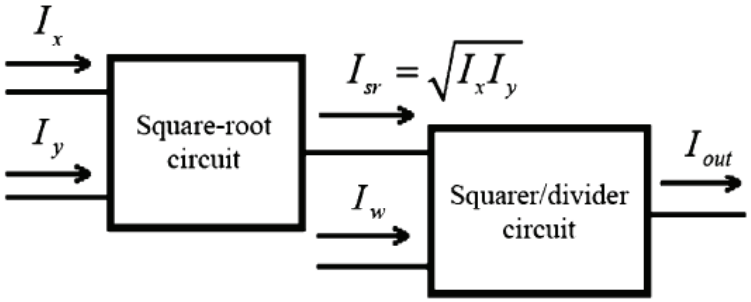


Figure 1. Simplified diagram of the multiplier/divider circuit

Since I_X and I_Y are the input currents of the square-root circuit, the output function of the first circuit can be written as

$$I_{sr} = \sqrt{I_x I_y}$$

Assuming that this current is the one of the input currents and applying a second I_W to the input, the output current of the whole circuit can be expressed as

$$I_{out} = \frac{I_{in}^2}{I_w} = \frac{\left(\sqrt{I_x I_y}\right)^2}{I_w} = \frac{I_x I_y}{I_w}$$

- In order to implement a multiplier/divider circuit, square-root and squarer/divider circuits must be designed

Current-mode multiplier/divider circuit

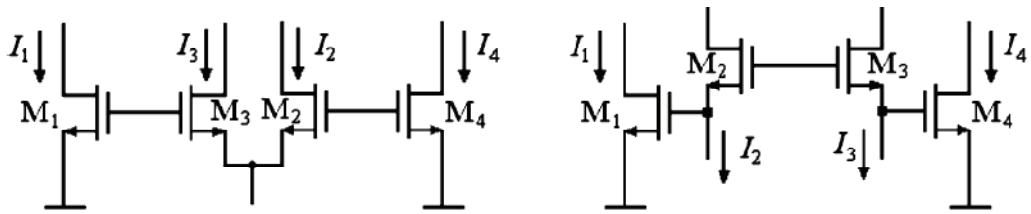


Figure 2. a)Up-down VTL loop b) Stacked VTL loop

Both square root circuit and squarer/divider circuit can be obtained by using either the up-down or stacked voltage translinear (VTL) loops

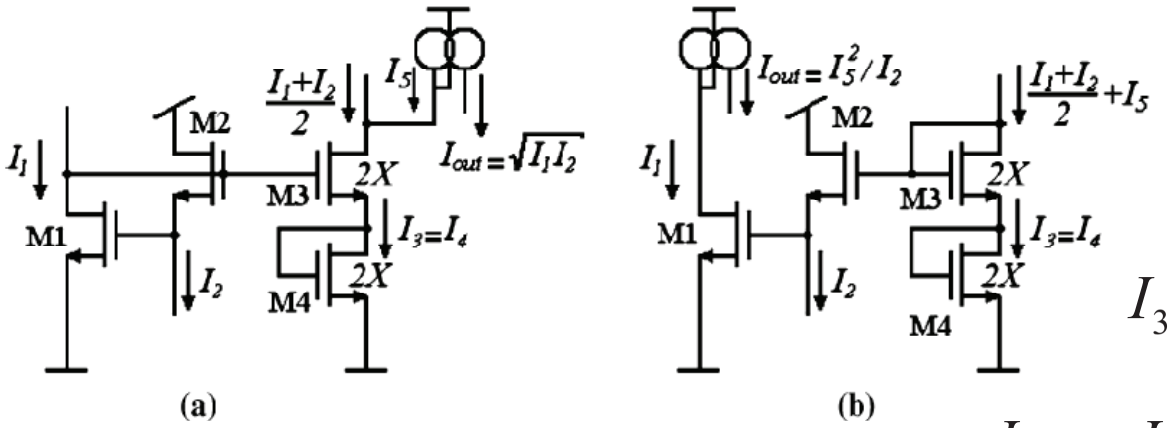
- Assuming that the aspect ratios of the transistors satisfy

$$\beta_1 = \beta_2 = \beta \; and \; \beta_3 = \beta_4 = 2\beta$$

- using the VTL law $V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4}$
- Assuming that the second order effects are negligible $I_D = \frac{\beta}{2}(V_{GS} - V_T)^2$
- Assuming that the Vth of MOSFETs are same

$$\sqrt{\frac{2I_1}{\beta}} + \sqrt{\frac{2I_2}{\beta}} = \sqrt{\frac{2I_3}{2\beta}} + \sqrt{\frac{2I_4}{2\beta}}$$

Current-mode multiplier/divider circuit



$$I_3 = \sqrt{I_1 I_2} + \frac{1}{2}(I_1 + I_2)$$

$$I_{out} = I_3 - \frac{1}{2}(I_1 + I_2) = \sqrt{I_1 I_2}$$

Figure 3. Applications of the stacked VTL loop
(a) Square-root cell (b) Squarer/divider cell.

- a square-root circuit can be obtained as shown in (a) if I_1 and I_2 are the input currents and the output current is a copy of I_5.
- a squarer/divider circuit can be obtained as shown in (b) if the output is a copy of either I_1 or I_2 and the inputs are the remaining two currents.

Proposed current-mode multiplier/divider circuit

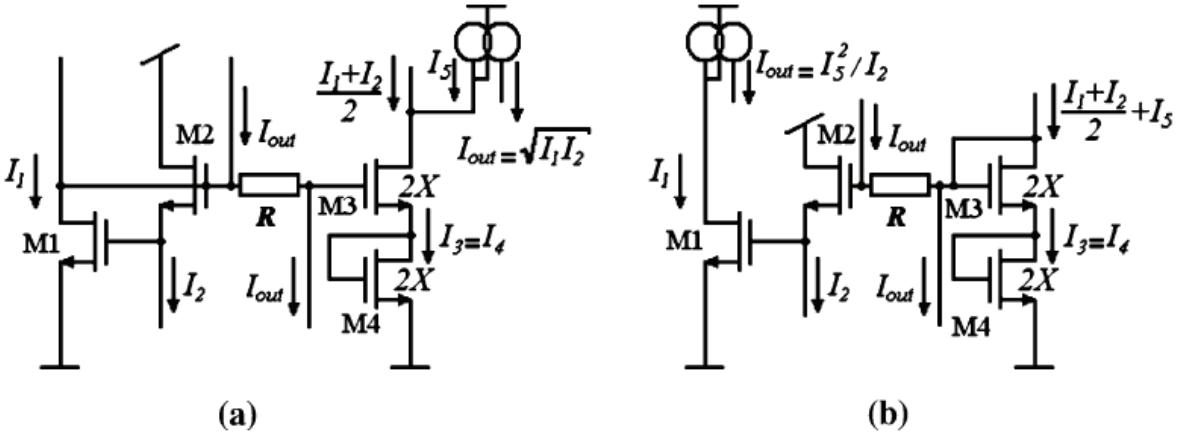


Figure 4. Modified current-mode circuits
a) square-root cell b) squarer/divider cell

Due to the second order effects small sized MOS transistors do not operate properly and therefore errors may occur in the output current function.

- The error of the output current function can be reduced using the resistance R between the gates of the MOS transistors M2, M3 and letting the output current Iout flow through this resistance. In this case, a new voltage term that is added to the VTL loop function which eliminates the error of the output current function.

Proposed current-mode multiplier/divider circuit

- with using the VTL law at figure 4

$$V_{GS1} - V_{TH1} + V_{GS2} - V_{TH2} = I_{out} \cdot R + V_{GS3} - V_{TH3} + V_{GS4} - V_{TH4}$$

- If the mobility reduction is taken into consideration, the drain current of a MOS transistor operated in saturation is given by

$$I_D = \frac{\beta}{2} \frac{(V_{GS} - V_{TH})^2}{1 + \theta'(V_{GS} - V_{TH})} \qquad V_{GS} - V_{TH} = \frac{I_D \theta'}{\beta} + \sqrt{(\frac{I_D \theta'}{\beta})^2 + \frac{2I_D}{\beta}}$$

$$(\frac{I_D \theta'}{\beta})^2 \square \frac{2I_D}{\beta} \qquad V_{GS} - V_{TH} \approx \frac{I_D \theta'}{\beta} + \sqrt{\frac{2I_D}{\beta}}$$

$$\frac{I_1 \theta'}{\beta} + \sqrt{\frac{2I_1}{\beta}} + \frac{I_2 \theta'}{\beta} + \sqrt{\frac{2I_2}{\beta}} = I_{out} \cdot R + \frac{I_3 \theta'}{2\beta} + \sqrt{\frac{I_3}{\beta}} + \frac{I_4 \theta'}{2\beta} + \sqrt{\frac{I_4}{\beta}}$$

Proposed current-mode multiplier/divider circuit

- As shown in Figure 4, $I_3=I_4$:

$$\frac{I_1\theta'}{\beta}+\sqrt{\frac{2I_1}{\beta}}+\frac{I_2\theta'}{\beta}+\sqrt{\frac{2I_2}{\beta}}=I_{out}\cdot R+\frac{I_3\theta'}{\beta}+2\sqrt{\frac{I_3}{\beta}}$$

- Using KCL equation at the output node of the modified square root cell

$$I_3=\sqrt{I_1I_2}+\frac{1}{2}(I_1+I_2)\Rightarrow I_3=\frac{1}{2}\left[\sqrt{I_1}+\sqrt{I_2}\right]^2$$

- Multipliying 4/β each term and taking the square root on both sides,

$$\sqrt{\frac{2I_1}{\beta}}+\sqrt{\frac{2I_2}{\beta}}=2\sqrt{\frac{I_3}{\beta}}$$

$$I_{out}\cdot R=\frac{\theta'}{\beta}\left(I_1+I_2-I_3\right)\qquad R=\frac{\theta'}{\beta}\left[\frac{I_1+I_2}{2\sqrt{I_1I_2}}-1\right]$$

Proposed current-mode multiplier/divider circuit

- Considering the mobility reduction effect, this equation indicated that the value of the resistance R to decrease the output current function error of the circuit.
- This equation can be expressed as

$$\sqrt{I_1 I_2} = (I_1 + I_2)\frac{\theta'}{2(\beta \cdot R + \theta')} \cdot E$$

- E is defined as

$$E = \frac{\sqrt{I_1 I_2}}{I_1 + I_2}\frac{2(\beta \cdot R + \theta')}{\theta'}$$

Proposed current-mode multiplier/divider circuit

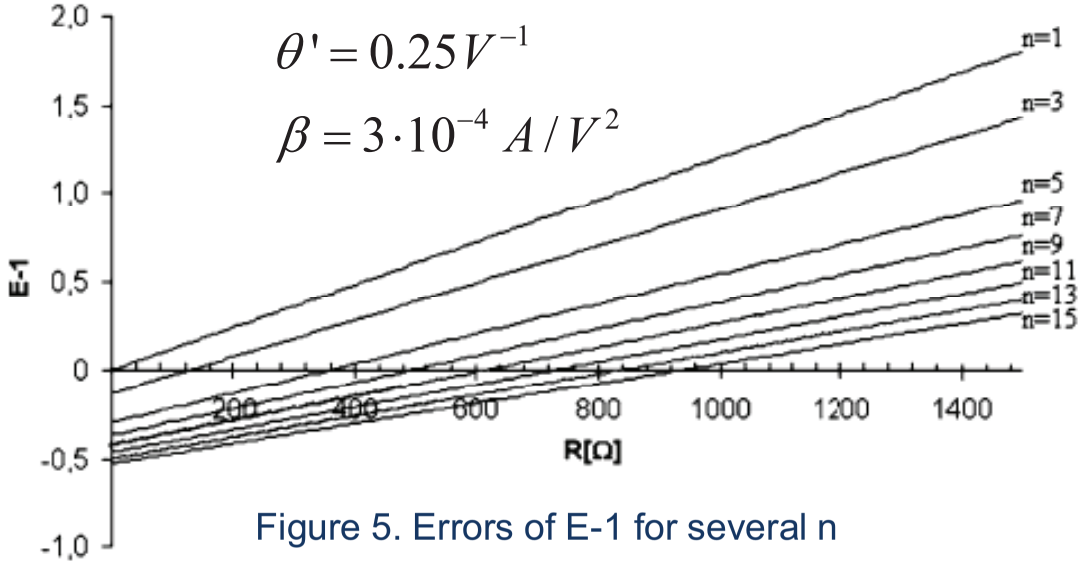


Figure 5. Errors of E-1 for several n

- If $I_2=nI_1$, then the E-1 error function is drawn in Figure 5.
- When input currents, I_1 and I_2 are equal (n = 1) output current function error generated by mobility reduction will be zero. the resistance R value will be zero.
- As the difference between two input currents (I_1, I_2) increases, the value of the resistance R which will compensate for the error will also increase.

Proposed current-mode multiplier/divider circuit

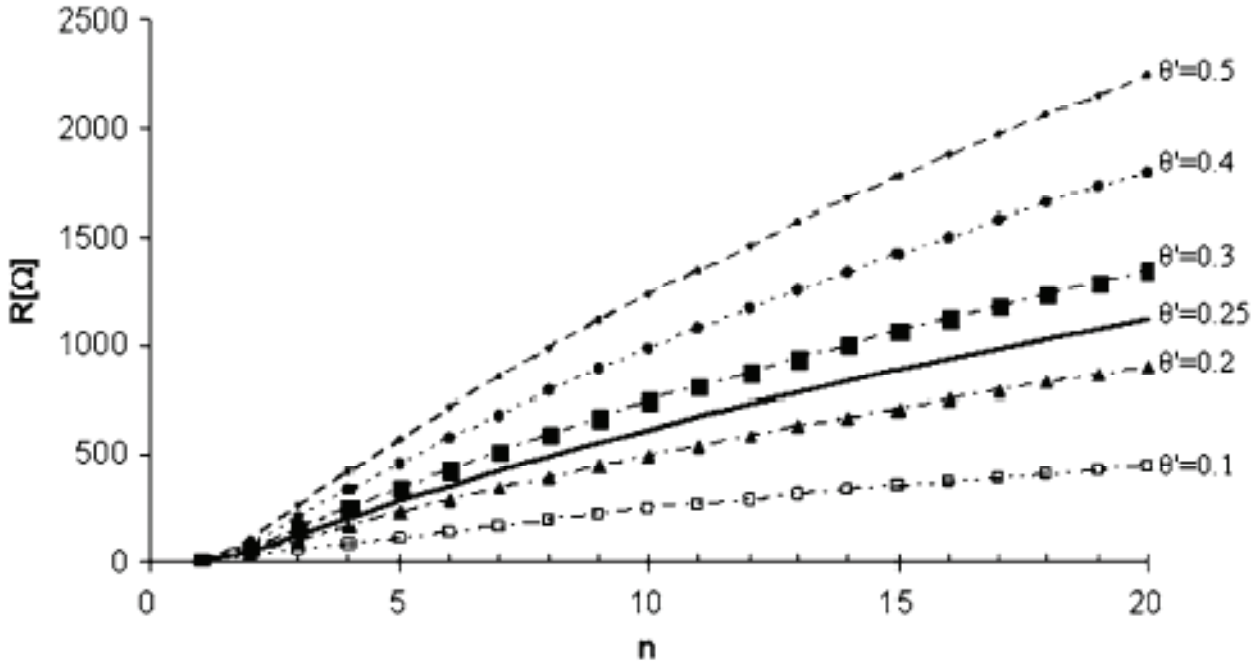


Figure 6. Variation in resistance R value with respect to n corresponding to different θ'

- As θ' increases, error generated by circuit increases as well as the value of the resistance which will compensate for it.

Proposed Circuit

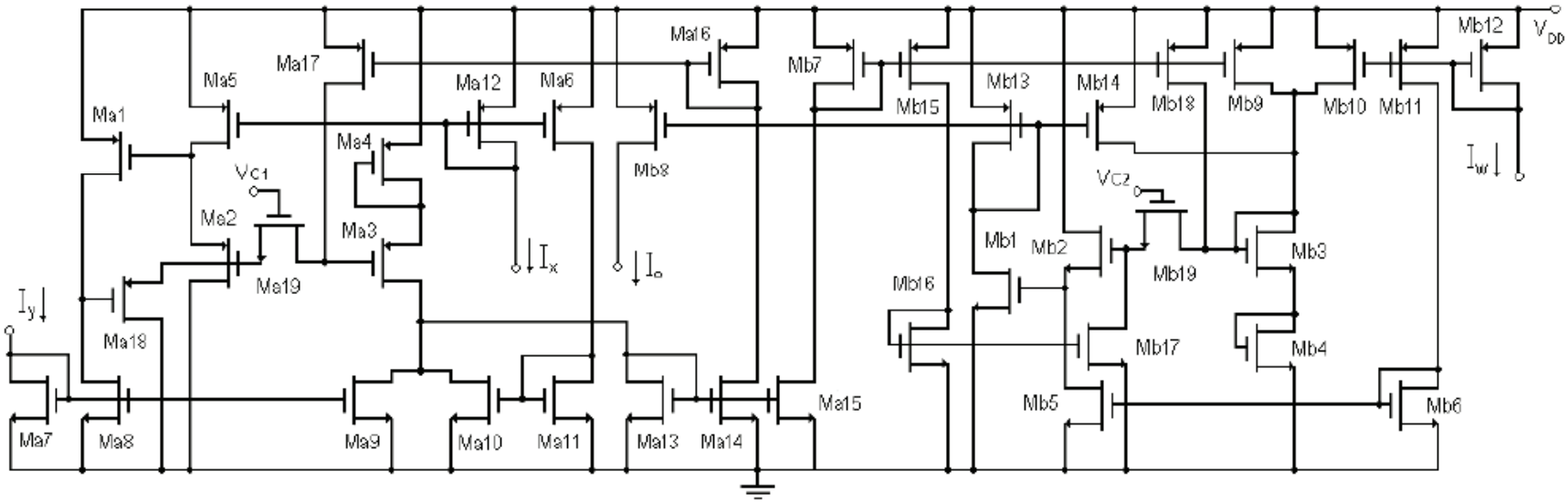


Figure 7. Proposed current-mode multiplier/divider circuit

- Resistances are realized with the transistors in Figure 7 and their value can be controlled by the VC control voltages. By this way output current function of the circuit can be controlled and the function errors of the current can be eliminated.

Proposed Circuit

- The output current function error of the square-root circuit that forms the left part of the circuit is reduced by the current flowing over the resistor R1. This process is carried out by flowing output current over the transistors Ma14, Ma16, Ma17, Ma18.

- The output current function error of the squarer/divider circuit that forms the right part of the circuit is reduced by the current flowing over the resistor R2. Mb15, Mb16, Mb17, Mb18 are used to provide the correction current flowing over the R2 resistor.

Simulation results

Table 1. Transistor dimensions

	W/L (μm)		W/L (μm)		W/L (μm)		W/L (μm)
Ma1	6/.7	Ma11	12/.7	Mb1	12/.7	Mb11	12/.7
Ma2	6/.7	Ma12	12/.7	Mb2	12/.7	Mb12	12/.7
Ma3	12/.7	Ma13	12/.7	Mb3	24/.7	Mb13	12/.7
Ma4	12/.7	Ma14	12/.7	Mb4	24/.7	Mb14	6/.7
Ma5	12/.7	Ma15	12/.7	Mb5	12/.7	Mb15	12/.7
Ma6	12/.7	Ma16	12/.7	Mb6	12/.7	Mb16	12/.7
Ma7	12/.7	Ma17	12/.7	Mb7	12/.7	Mb17	12/.7
Ma8	12/.7	Ma18	12/.7	Mb8	12/.7	Mb18	12/.7
Ma9	6/.7	Ma19	10/.7	Mb9	12/.7	Mb19	80/.7
Ma10	6/.7			Mb10	6/.7		

- SPICE simulations were performed using TSMC 0.35μm LEVEL 3 CMOS process parameters.
- The power supply voltage is 3V.

Simulation results

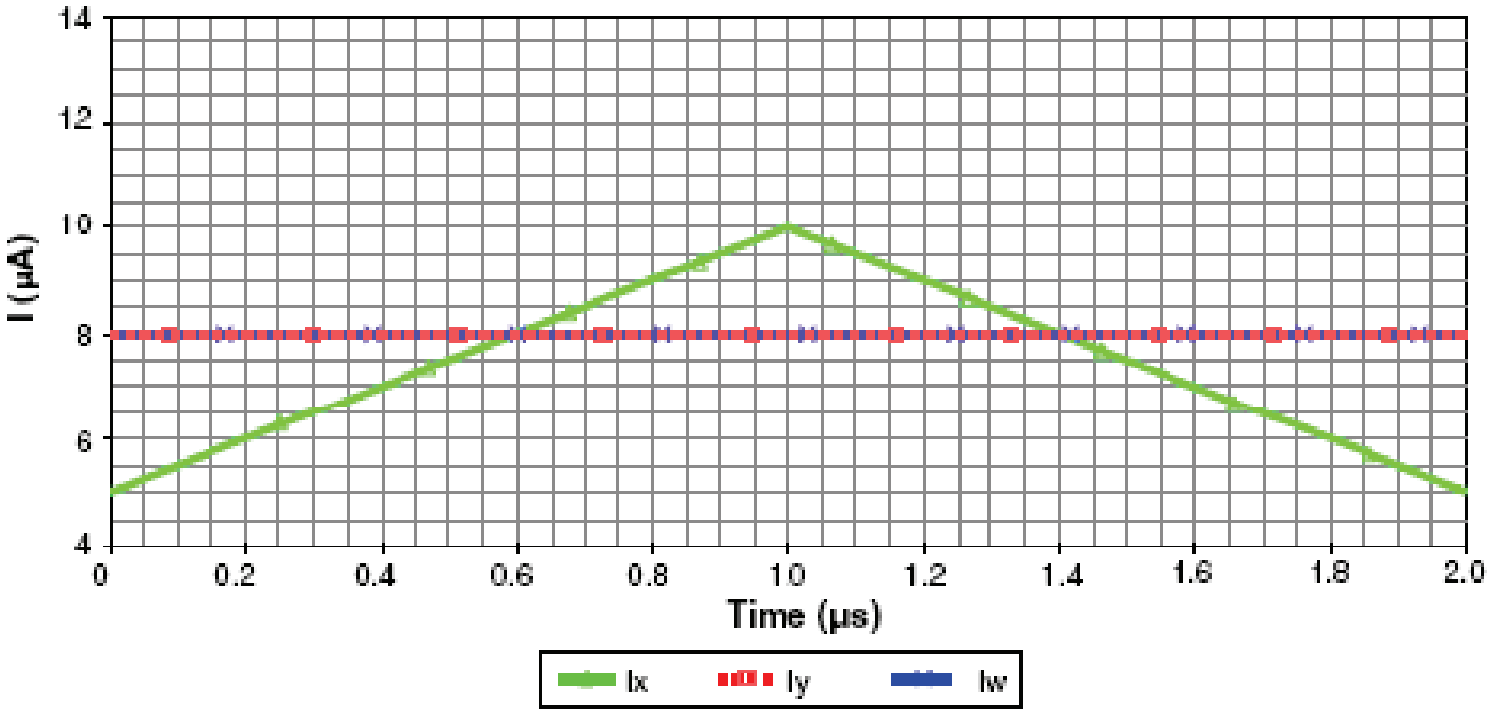
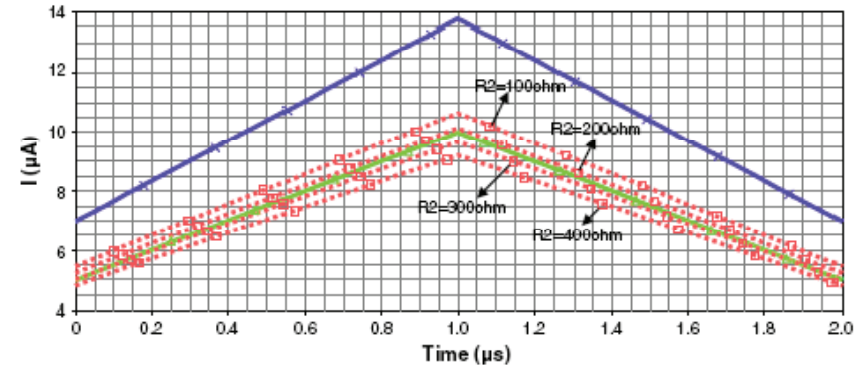
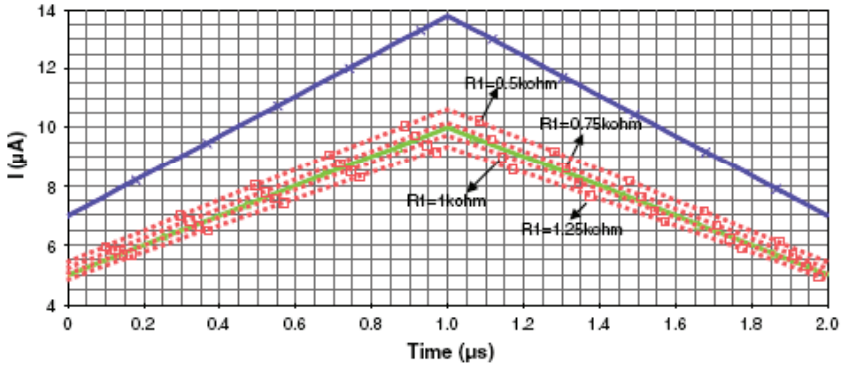


Figure 8. Input currents Ix, Iy and Iw of the proposed multiplier/ divider

Simulation results



R1=500 ohm



R2=50 ohm

Figure 9. Comparison of the output currents and the ideal curve

- As expected, for different values of the resistances R_1 and R_2 the output current function varies around the ideal curve.
- Because of the second order effects the output current function of the conventional circuit is different from the ideal curve.
- It is apparent that the error of the output current function can be reduced by choosing appropriate resistance values.

Simulation results

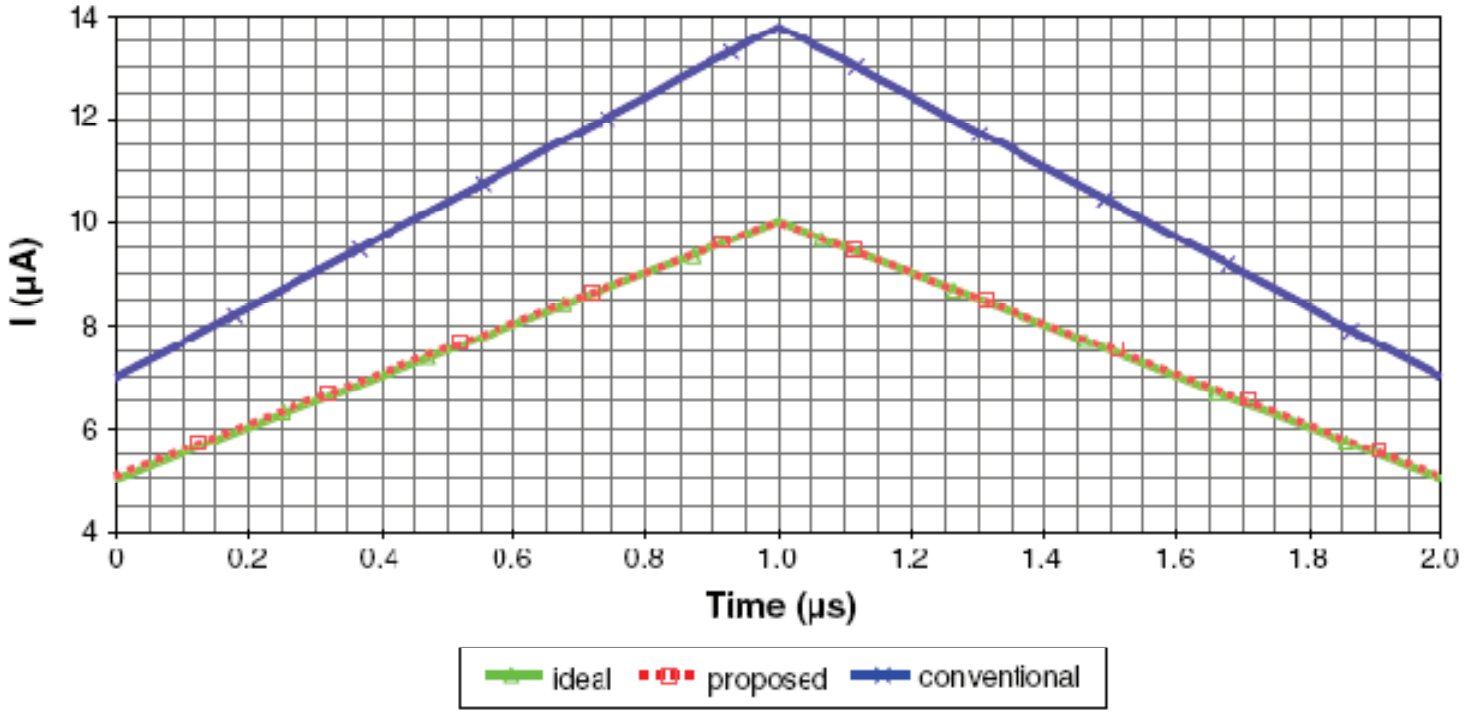
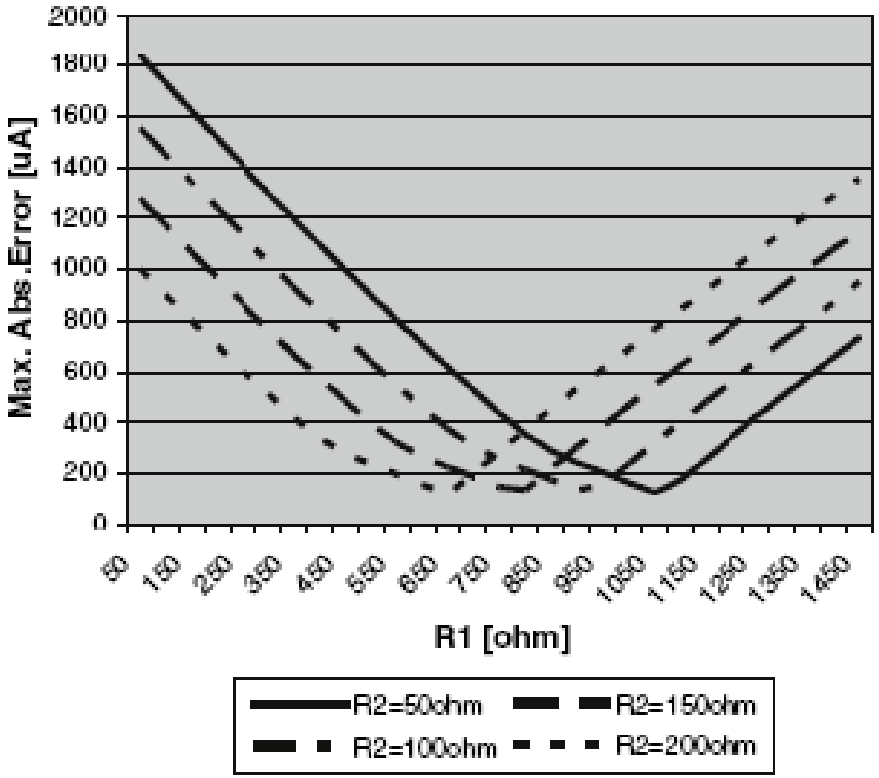


Figure 10. Comparison of the output currents and the ideal curve

- V_{C1} and V_{C2} are taken 2.09 V and 5 V.

Simulation results



- In Figure 11, it can be easily seen that the output current function error is reduced by changing the values of the resistances R_1 and R_2.

Figure 11. Maximum absolute errors for different values of R1 and R2

Simulation results

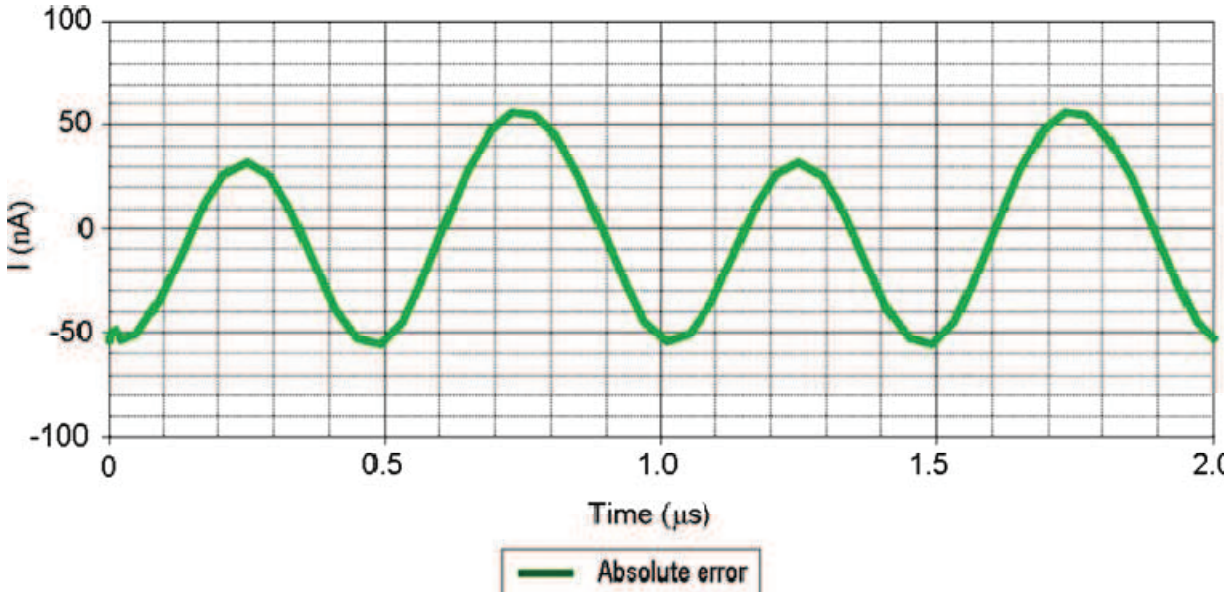


Figure 12. Simulated absolute error of the proposed multiplier/divider

- The absolute error of the simulated output, i.e., $(I_x.I_y/I_w)-I_z$, where the input currents are $I_x = I_y = I_w = 5(2+\sin 2\pi ft)$ μA with f = 1 MHz.
- The simulated absolute error is less than 0.055 μA, thus confirming the high precision of the proposed multiplier/divider circuit.

Simulation results

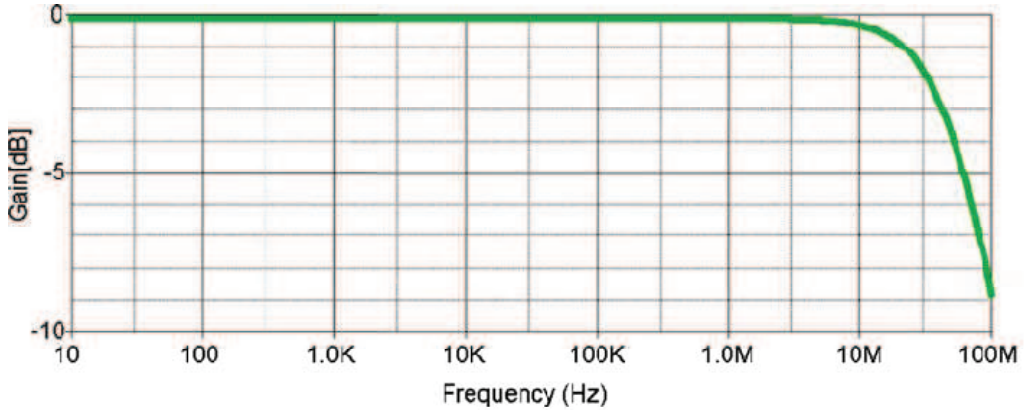


Figure 13. Frequency characteristics of the proposed multiplier/divider

- The small-signal bandwidth measured from the input I_x to the output (with $I_y = I_w = 15$ μA) is 44MHz

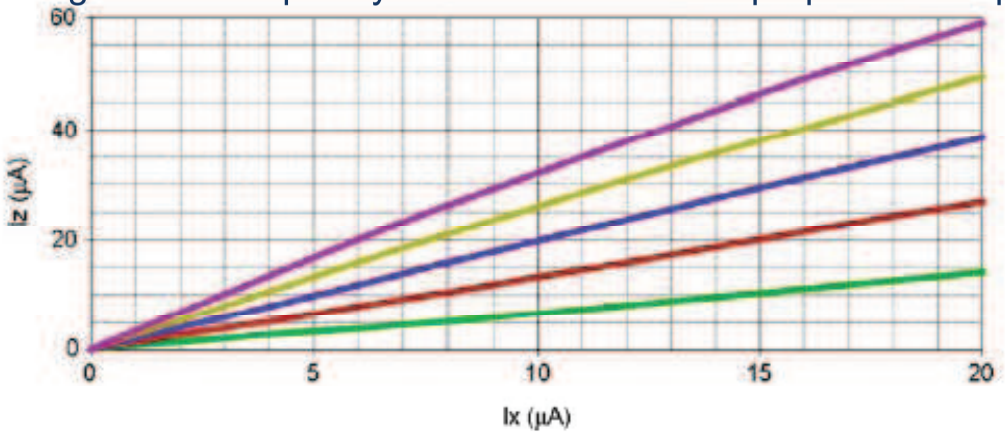


Figure 14. Simulated DC transfer characteristics of the multiplier/ divider

- Input currents were $I_w = 3$ μA, I_y values ranging from 2 μA to 10 μA in 2μA steps and I_x swept from 0 to 20 μA.

Using of the proposed circuit as an analog amplitude modulator

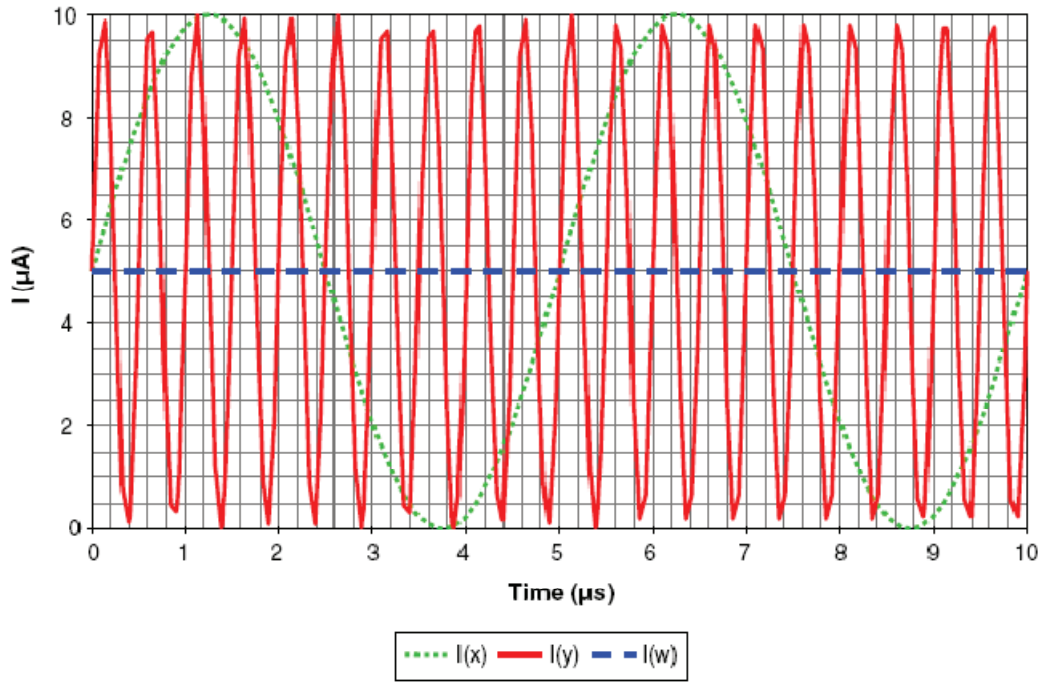


Figure 15. Input currents of the multiplier/divider as an amplitude modulator

- Input currents are taken as $I_x = 5(1+\sin 2\pi ft)$ μA with f = 0.2MHz, $I_y = 5(1+\sin 2\pi ft)$ μA with f = 2MHz and I_w is taken as a fix current of 5μA as shown in Fig. 15.

Using of the proposed circuit as an analog amplitude modulator

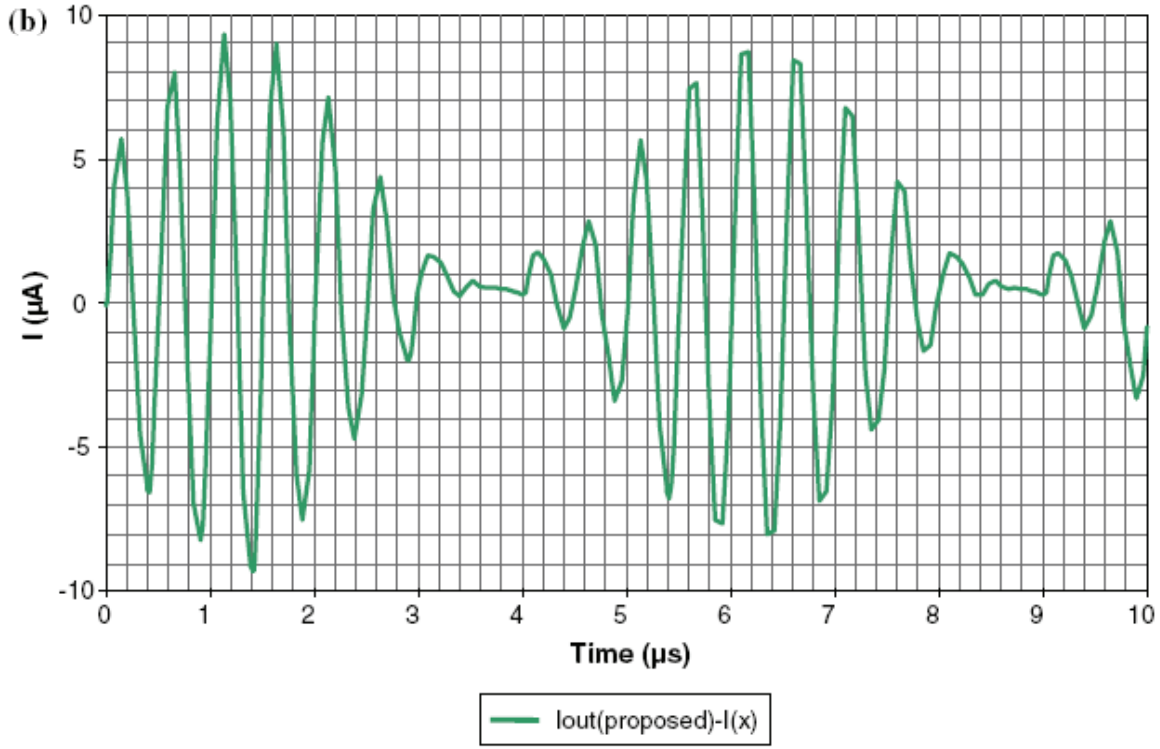


Figure 16. Modulated ac output current of the multiplier/divider as an amplitude modulator

Using of the proposed circuit as an analog amplitude modulator

Table 2. Performance parameters of the multiplier/divider

Parameter	Value		
	Proposed	Cruz-Blas et al. [2]	Oliveira and Oki [3]
Technology	0.35 μm CMOS	0.8 μm CMOS	0.35 μm CMOS
Supply voltage	3 V	1.5 V	1.5 V
THD	0.14% (input: 10 μA_{pp} at 1 MHz)	0.90% (input: 24 μA_{pp} at 1 kHz)	0.83% (input: 20 μA_{pp} at 10 MHz)
BW (simulated)	44 MHz	5.5 MHz	140 MHz
Area	0.01 mm^2	0.10 mm^2	0.02 mm^2

- The circuit proposed provides to the IC designers advantages such as smaller chip size and lower distortion.

CONCLUSION

- This paper proposes a method to reduce the errors generated by the second order effects in the current-mode circuits employing MOS translinear loop. In addition, a high-precision multiplier/divider circuit is also designed using the introduced method.

The main advantages of the proposed circuit can be summarized as,

- a smaller area on the chip
- operation at higher frequencies
- power efficiency
- High precision
- possibility of controlling the output current with the control voltage
- reduced errors of the output current function which is caused by secondary effects

Reference

[1] S. Menekay, R.C. Tarcan, H. Kuntman, 'Novel high-precision current mode multiplier/divider', Analog Integrated Circuits and Signal Processing, Vol.60, No.3, 237-248, 2009.

[2] C. A. De La Cruz-Blas, A. J. Lopez-Martin and A. Carlosena, "1.5 V four-quadrant CMOS current multiplier/divider." Electronics Letters, 39(5), 434-436. doi:10.1049/el:20030298, 2003.

[3] V. J. S. Oliveira and N. Oki, "Low voltage four-quadrant current multiplier: An improved topology for n-well CMOS process." In Design & technology of integrated systems in nanoscale era, DTIS. International conference (pp. 52-55), 2007.