LOW DRIVE CURRENT AMPLIFIERS

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Summary

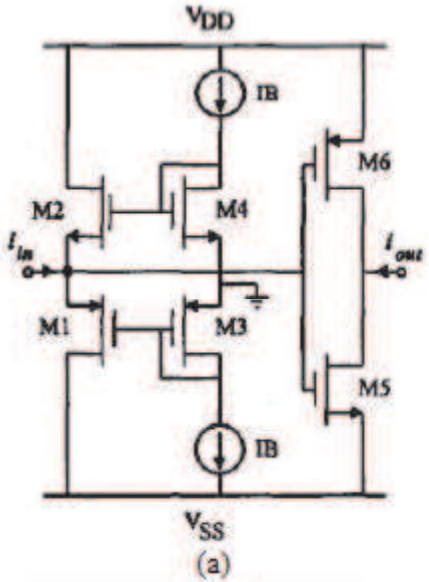
- Introduction
- Input Stages:
  - The CCII
  - Class A Input Stages
  - Class AB Input Stages
- Class A Output Stages
- Current Comparators

What is low drive current amplifier?

These amplifiers find applications in on chip environments, where load resistances are strictly controlled by the designer unlike high drive amplifiers where off chip loads are driven. For this reason, they are not required to deliver output currents higher than the quiescent current of the output branches.

Their low voltage and high speed capability is important.

Simple Current Amplifiers

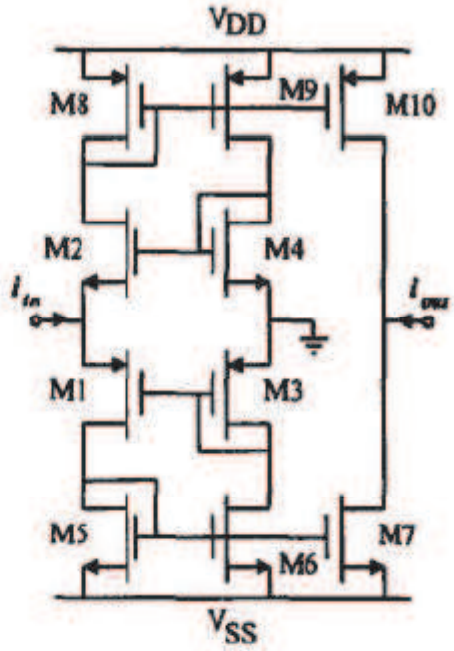


(a)

The circuit in Fig.1a :
Input voltage is equal to ground potential under both AC and DC conditions due to translinear loop, formed by M1-M4.

$$r_{in} \cong \frac{1}{g_{m1} + g_{m2}}$$

$$A = \frac{i_{out}}{i_{in}} = (g_{m5} + g_{m6}) r_{in}$$



(b)

The circuit in Fig.1b :
Bias currents are not defined well. For this reason, important performance parameters are not defined well.

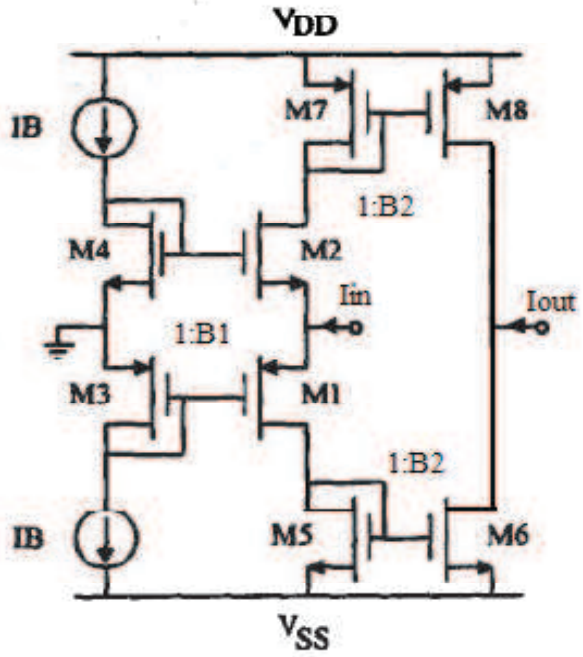
Positive feedback decreases the input resistance.

$$r_{in} \cong \left[\frac{1}{g_{m1}}\left(\frac{1}{g_{m5} r_{d1} // r_{d5}} + \frac{1}{g_{m3} r_{d3} // r_{d6}}\right)\right] // \left[\frac{1}{g_{m2}}\left(\frac{1}{g_{m8} r_{d8} // r_{d2}} + \frac{1}{g_{m4} r_{d4} // r_{d9}}\right)\right]$$

$$A = \frac{i_{out}}{i_{in}} = \frac{(W/L)_1}{(W/L)_5} = \frac{(W/L)_{10}}{(W/L)_8}$$

Figure 1: Simple Current Amplifiers

Simple Current Amplifiers



All currents are set by the aspect ratios. For this reason, important performance parameters are defined well.

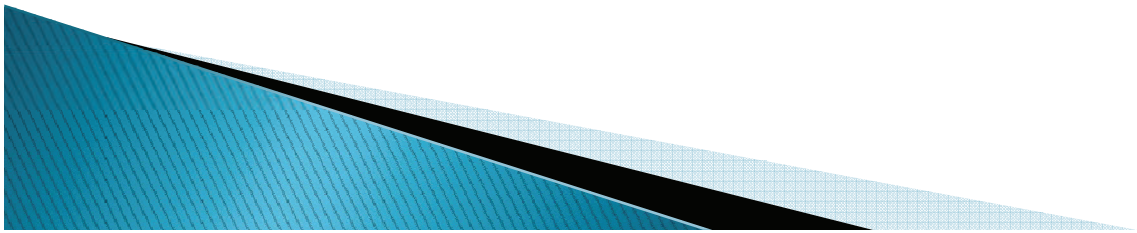
$$r_{in} \cong \frac{1}{g_{m1} + g_{m2}}$$

$$A = \frac{i_{out}}{i_{in}} = \frac{(W/L)_6}{(W/L)_5} = \frac{(W/L)_8}{(W/L)_7} = B2$$

Figure 2: Mirrored Current Amplifier

Input Stages

- Circuit performance parameters such as input resistance, gain, bandwidth, systematic offset, noise, etc., must be accurately set.
- These parameters need well defined bias current in the input stage. Moreover, well defined input bias voltage is required to prevent systematic offset and to bias input signal generators.



Input Stages: CCII

CCII is a three terminal device with X, Y and Z terminals. Port relations are given in the matrix:

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix}$$

$$V_y = V_x \quad I_Z = \pm I_X$$

$$I_y = 0$$

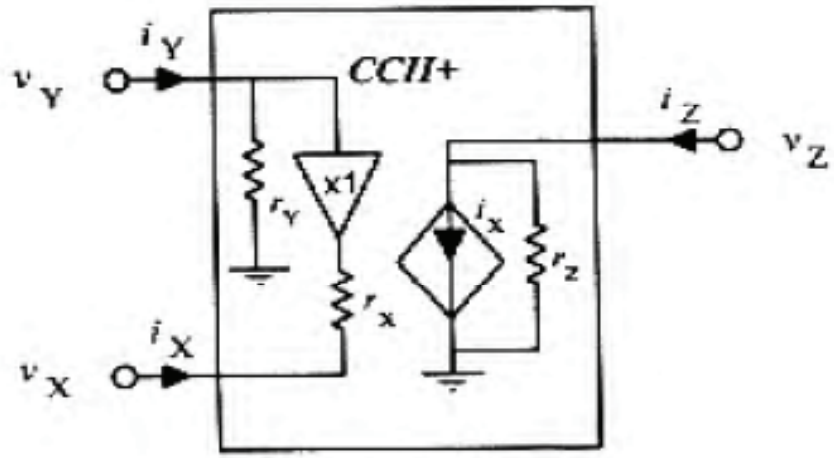


Figure 3: CCII+ block diagram

r_Z r_Y r_X are finite internal resistances.

r_Z and r_Y are ideally infinite. r_X is ideally zero.

CCII

- Noise Equivalent of CCII Circuit

Noise in CCII can be modeled by three noise generators: V_{nY}, I_{nY} and I_{nX}.

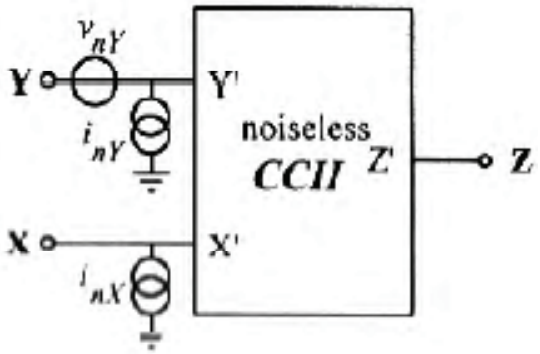
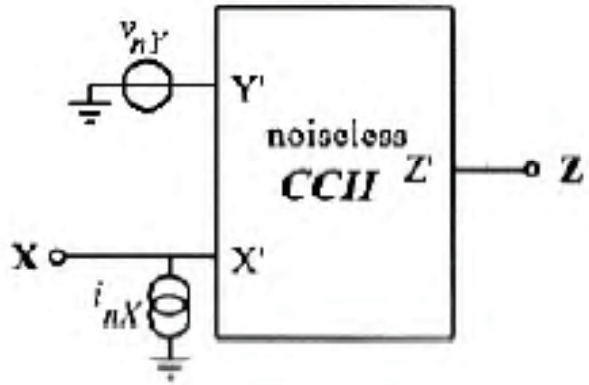


Figure 4: CCII noise equivalent Circuit

-Noise voltage is only associated with Y terminal since any noise voltage source in series with X terminal can be directly transferred to the Y terminal.

-Terminal X is characterized by only one current generator since any current noise sources in parallel with Z terminal can be transferred to the X terminal.

CCII



In Current mode amplifiers Y terminal is always grounded. New equivalent circuit is given in Figure 5.

Figure 5: Noise model for CCII used as an input stage

The voltage and current output noise powers at terminal X and Z:

$$N_{vX} = \overline{v_{nY}^2}$$

$$N_{iZ} = \overline{i_{nX}^2}$$

Class A Input Stages

Simple implementation of Class A CCII- is given in Figure 6. Its main drawbacks are high r_X and error in voltage transfer.

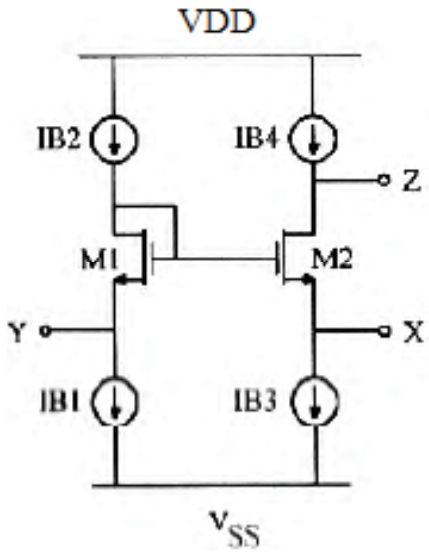


Figure 6: Class A CCII- implementation

$$\frac{V_X}{V_Y} = \frac{1}{1+\frac{1}{g_{m2}r_{b3}}} \qquad \frac{i_z}{i_X} = -1$$

$$r_X = \left(\frac{1+g_{d2}(r_{b4} // R_{LZ})}{g_{m2}} \right) // r_{b3}$$

$$r_z = \left(\frac{g_{m2}}{g_{d2}} R_{LX} \right) // r_{b4}$$

r_b:Current source resistances
R_L: Equivalent load resistances

Class A Input Stages

CCII+ can be obtained by adding current mirror to the CCII- so that current in Z terminal is inversed.

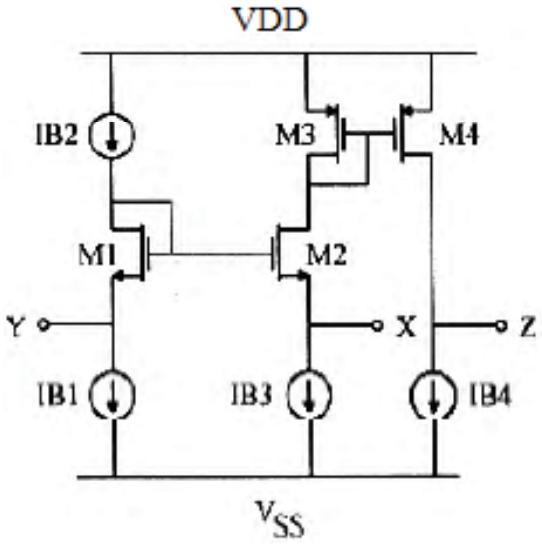


Figure 7: Class A CCII+ implementation

-Voltage gain is same with CCII-

$$A_i = \frac{g_{m4}}{g_{m3}}$$

$$r_X \approx \frac{1}{g_{m2}}$$

$$r_Z \approx \frac{1}{g_{d4}} // r_{b4}$$

$$V_{OS} = V_X - V_Y \approx (V_{T2} - V_{T1}) + \left(\sqrt{\frac{I_{D2}}{B_2}} - \sqrt{\frac{I_{D1}}{B_1}} \right)$$

Class A Input Stages

Class A CCIIs can also be implemented with differential amplifiers.

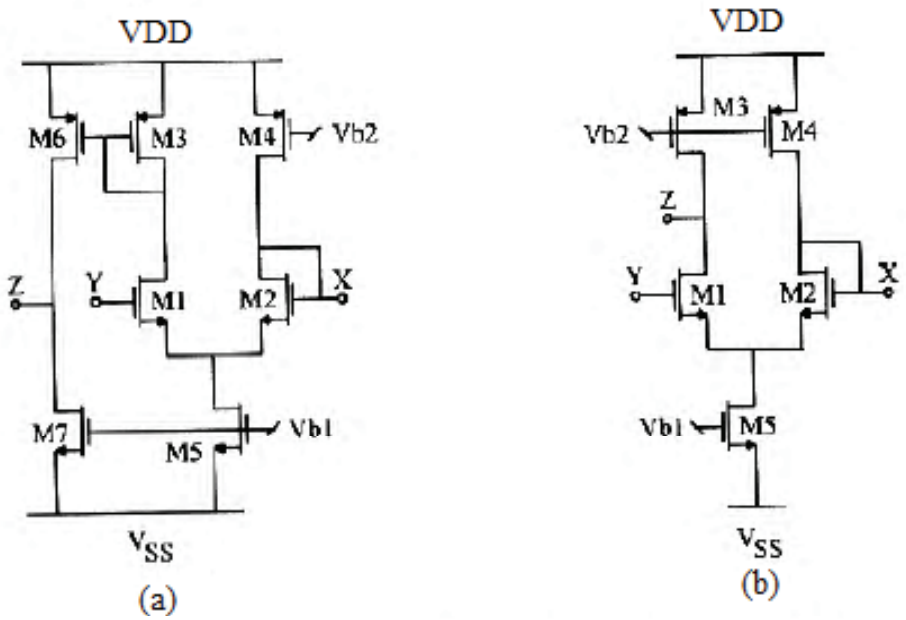


Figure 8: Differential Class A CCIIs

$$A_V = \frac{1}{1 + \frac{1}{\frac{1}{2}\frac{g_{m1,2}}{g_{d1,2} + g_{d3}}}}$$

$$r_X \approx \frac{2}{g_{m1,2}}$$

$$r_Z(a) \approx \frac{1}{g_{d6} + g_{d7}}$$

$$r_Z(b) \approx \frac{1}{g_{d3}}$$

Class A Input Stages

IMPROVED CCII SOLUTIONS [1]

Relatively high r_X resistances can be decreased using this configuration. Thanks to M9 source follower stage. Current mirrors M3 and M4 helps to obtain full transconductance so that gain increases with respect to mentioned differential class A input stages.

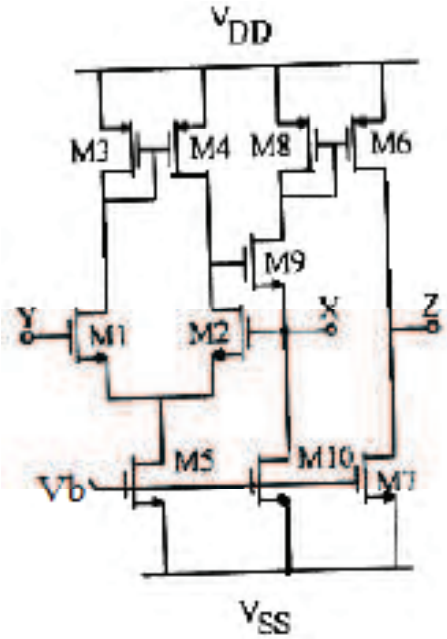


Figure 9: Improved CCII configuration

$$A_V \approx \frac{1}{1+\dfrac{g_{d1,2}+g_{d4}}{g_{m1,2}}}$$

$$r_X \approx \frac{1}{g_{m9}\dfrac{g_{m1,2}}{g_{d1,2}+g_{d4}}}$$

Class A Input Stages

IMPROVED CCII SOLUTIONS [2]

A simple alternative to the circuit in Figure 9 is given below. Matching is an important problem for this circuit and this causes offset problems. The circuit in Figure 10b is used to reduce offset. MC1 and MC3 are matched to M1 and M3 and aspect ratio of MC2 is half that of M5.

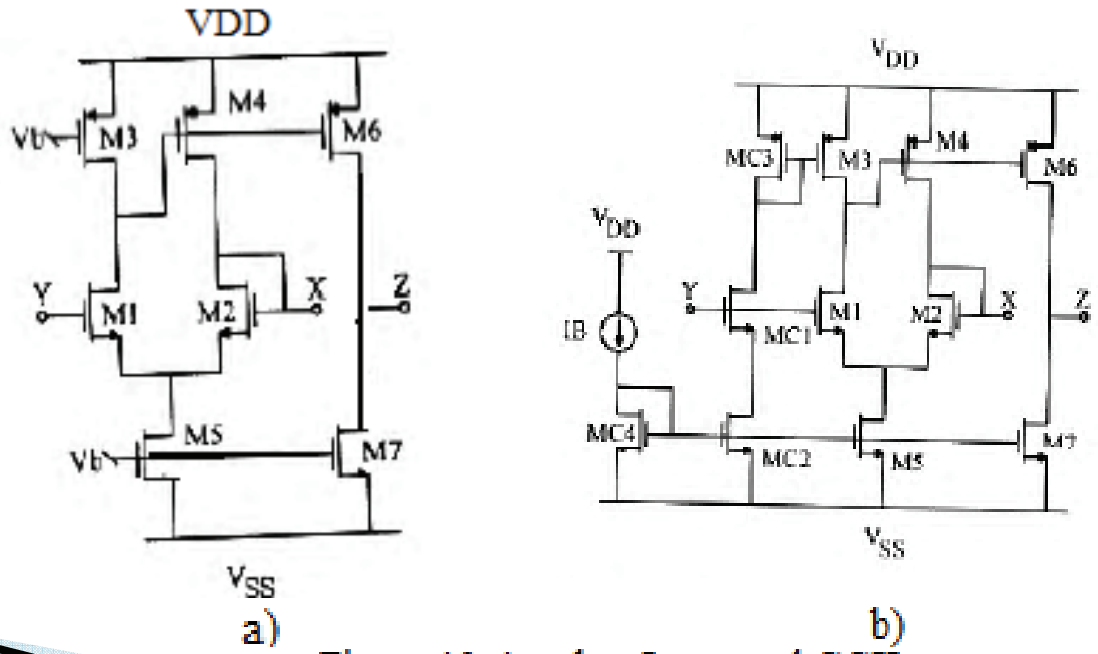


Figure 10-Another Improved CCIIs

$$A_V = \frac{1}{1+\frac{1}{\frac{g_{m2}}{g_{d2}}}}$$

$$r_X = \frac{g_{d1,2} + 2g_{d4}}{g_{m1,2}g_{m4}}$$

Class AB Input Stages

- Although class A input stages provide high accuracy, good frequency response, class AB topologies are often preferred due to their better slew rate performance and output swing is not limited by the quiescent current and also better SNR is obtained.
- Two Class AB voltage follower implementations are given below. They provide well controlled bias currents and output voltages and also they have same output impedance.

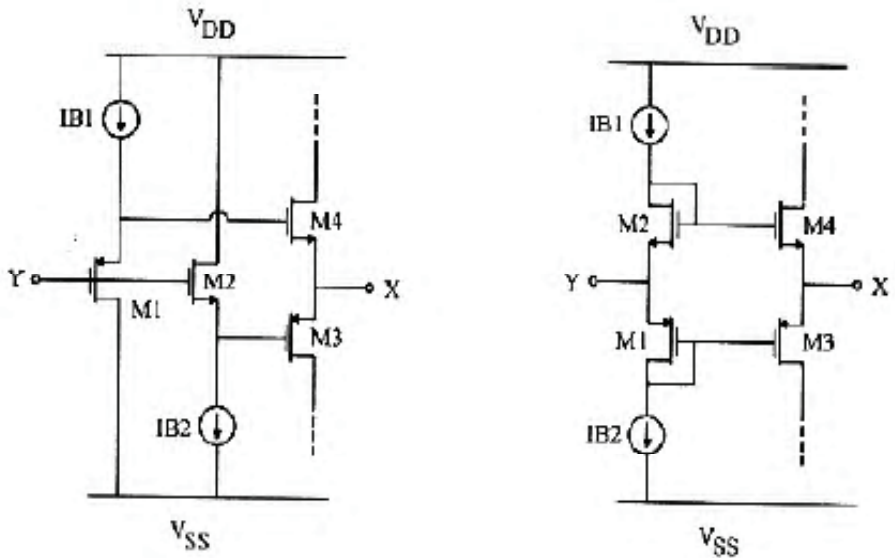


Figure 11- Two Class AB voltage follower implementations

Class AB Input Stages

- By setting $I_{B1}=I_{B2}=I_B$ and choosing aspect ratios as following:

$$\frac{(W/L)_3}{(W/L)_1}=\frac{(W/L)_4}{(W/L)_2}=n$$

M1, M3 and M2, M4 acquire the same gate to source voltages, with the current in M3 and M4 being set to $n.I_B$. Assuming transistors have same source-bulk voltages, M1-M4 provide a translinear loop which reflects DC voltage of Y on terminal X.

The input resistances are same as equation at terminal X. Fig 11a exhibits infinite input resitance, while Y resistance of b is the parallel combination of the output resistances of current sources I_{B1} and I_{B2}.

The circuit in (a) needs twin well process to equal source to bulk voltages of n channels or p channel transistors. In contrast, (b) is not affected by this problem since M1-M3 and M2-M4 transistors must be placed in a well. Moreover, (b) needs good matching between current sources I_{B1} and I_{B2} in order to prevent systematic offset.

Class AB Input Stages

Complete Class AB CCII+ and CCII- are implemented using the circuit in Fig.12. Complementary current mirrors are used in CCII+, while two complementary folded cascode structures used for CCII-.

The circuit in a) is preferred, because its output current is not limited by any constant value. However, output current of the circuit in b) is limited by current sources.

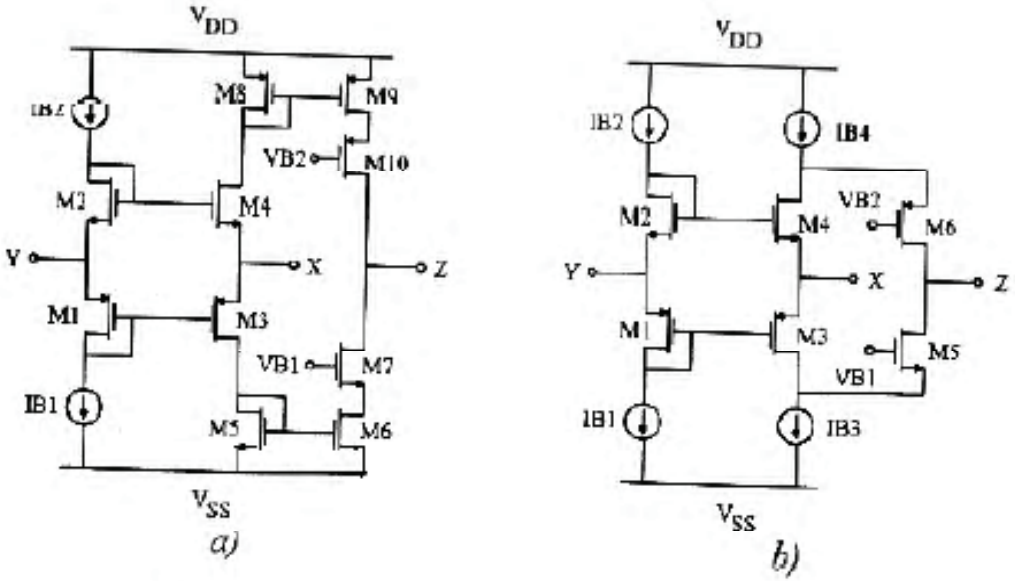


Figure 12-Class AB CCIIs; a)CCII+ and b)CCII-

$$A_V = \frac{V_X}{V_Y} = \frac{1}{1 + \frac{g_{d3} + g_{d4}}{g_{m3} + g_{m4}}}$$

$$r_{in} = \frac{1}{g_{m3} + g_{m4}}$$

OUTPUT STAGES

- Current mode amplifiers are different than voltage mode amplifiers. Output of voltage mode circuits can be used for both in feedback and driving load. However, current amplifiers have two different outputs, one for feedback and other for load. For this reason, output stages operate within feedback network so that load current is derived from feedback current.
- In this section Class A output stages will be examined due to their speed, accuracy and output resistance.

Output Stages for COAs

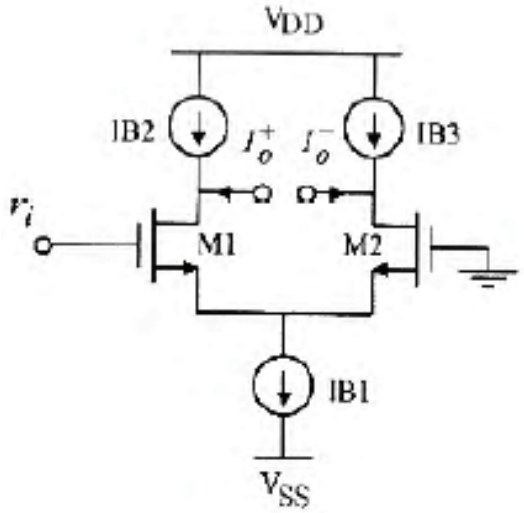


Figure 13-Simple current output stage

The simplest topology to implement a transconductance output stage is given in Figure 13. Equivalent transconductance is given below:

$$G_m = \frac{i_o^+}{V_i} = -\frac{i_o^-}{V_i} = \frac{1}{2} g_{m1,2}$$

Output Stages

- Differential transconductance:

$$G_{md} = \frac{i_o^+ - i_o^-}{V_i} = g_{m1,2}$$

Common mode transconductance :

$$G_{mc} = \frac{i_o^+ + i_o^-}{2V_i} = \frac{1}{2r_{b1}}$$

Common mode R.R:

$$CMRR = 2g_{m1,2}r_{b1}$$

Differential output resistance:

$$r_{od} = 2(r_{d1,2} // r_{b2,b3})$$

Common mode output resistance:

$$r_{oc} = r_{b2,b3} //(2g_{m1,2}r_{d1,2}r_{b1})$$

Both of the resistances are dependent to r_b resistances. Common mode resistance limits closed loop output resistance. If cascode current mirrors are used, r_{oc} increases but low voltage advantage of this circuit vanishes.

Output Stages

- **Arbel Current output stage**

$$G_m = \frac{i_o^+}{V_i} = -\frac{i_o^-}{V_i} = \frac{1}{2}(g_{m1,2} + g_{m3,4})$$

$$G_{mc} = \frac{i_o^+ + i_o^-}{2V_i} = \frac{1}{2r_{b1}} + \frac{1}{2r_{b2}}$$

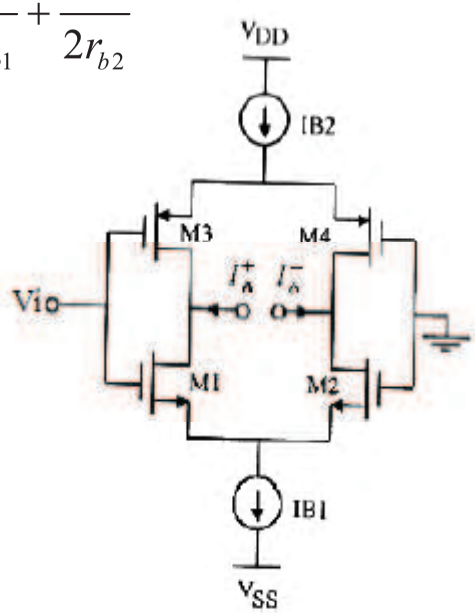


Figure 14- Arbel current output stage

$$G_{md} = \frac{i_o^+ - i_o^-}{V_i} = g_{m1,2} + g_{m3,4}$$

$$CMRR = 2\frac{g_{m1,2} + g_{m3,4}}{\frac{1}{r_{b1}} + \frac{1}{r_{b2}}}$$

$$r_{od} = 2(r_{d1,2} // r_{d3,d4})$$

$$r_{oc} = 2\left[(g_{m1,2} r_{d1,2} r_{b1}) // (g_{m3,4} r_{d3,4} r_{b2})\right]$$

Design Examples[1]

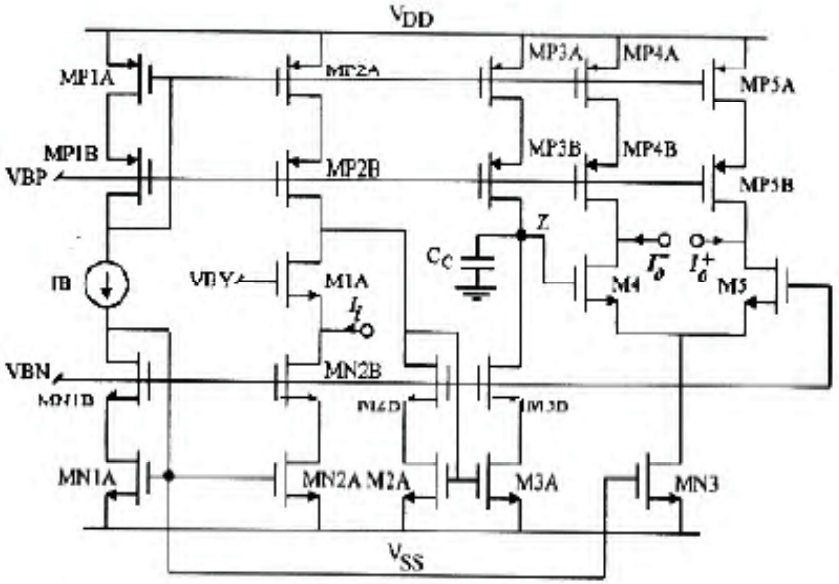


Figure 15- 1st Design example for COA

M1A implements input current follower, C_c is compensation capacitor. Class A input CCII+ limits slew rate, but it provides low voltage capability which is an advantage of this circuit to the other configurations.

Technology	2 μm
V_{DD}-V_{SS}	1.5 V
DC Power	≅40 μW
Gain	94 dB
GBW	65 MHz
M_ϕ	40 °

Design Examples [2]

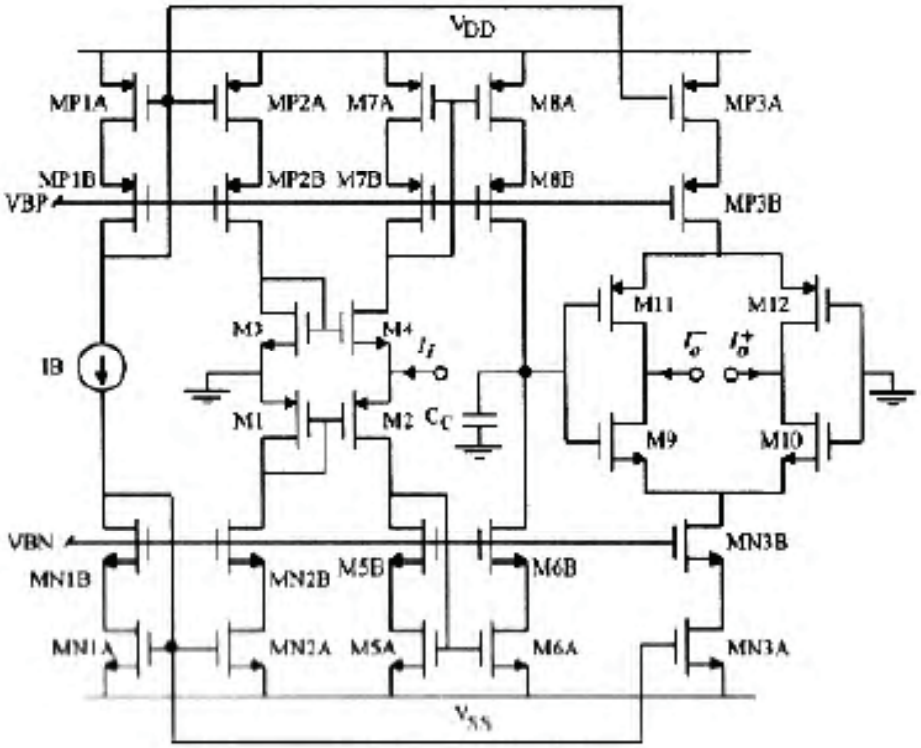


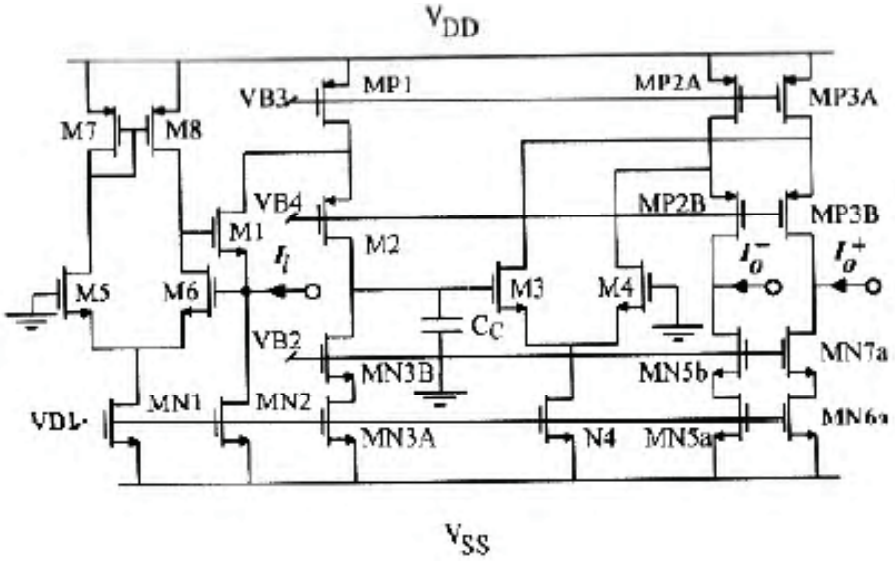
Figure 16- 2nd Design example for COA

Class AB input stage is used in this circuit. Thus, high slew rate is obtained. Output stage is Arbel type so that common mode resistance is better. Thus, accurate closed loop performance is ensured with respect to A class output stage.

Technology	2 µm
V_{DD}-V_{SS}	3 V
DC Power	≅90µW
Gain	96 dB
GBW	128 MHz
M_ϕ	---

Design Example[3]

- Another sample for COA is given in Fig.17. The use of current mirrors is avoided in this design. A common gate transistor M2 is used instead of it. Local feedback at the input decreases the input resistance. GBW of the feedback loop must be higher than that of the main loop to take this advantage. For this reason, circuit must be compensated with a high capacitors. The circuit consists of A class input and output stages. Output stage is a folded cascode transconductance stage which introduces another non dominant pole and this must be taken into account for a good phase margin.



Technology	1.2 μm
V_{DD}-V_{SS}	6 V
DC Power	4.5 mW
Gain	70 dB
GBW	210 MHz
M_ϕ	45°

Figure 17- 3rd Design example for COA

Design Examples [4]

- VFCOA is given in Figure 18. This circuit consists of input CCII+ stage and CCII- output stage. The input is a class AB stage, but the output is not class AB stage. Performance of the circuit is also given below.

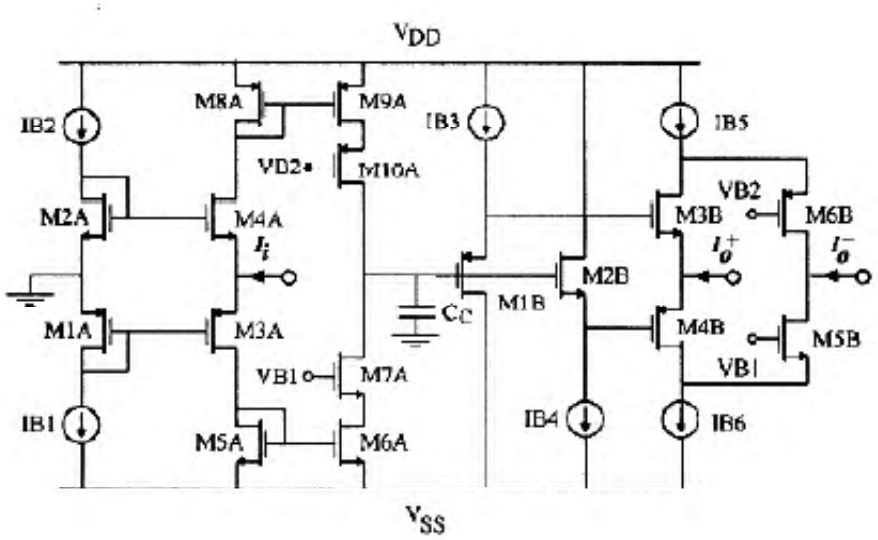


Figure 18-4th Design Example

Parameter	Value	
Technology	1.2 µm	
V_{DD}-V_{SS}	5 V	
DC Power	0.42 mW	
Gain	62 dB	
GBW	30 MHz	
M_ϕ (C_L=1pF)	53 °	
$T_{setti.}$ (0.1%)	35 ns	
THD	-70 dB	-60 dB
(i_{out})	(5mA)	(10mA)

Design Example [5]

The circuit consists of two AB CCII- stages. Cross coupled output section provides current inversion.

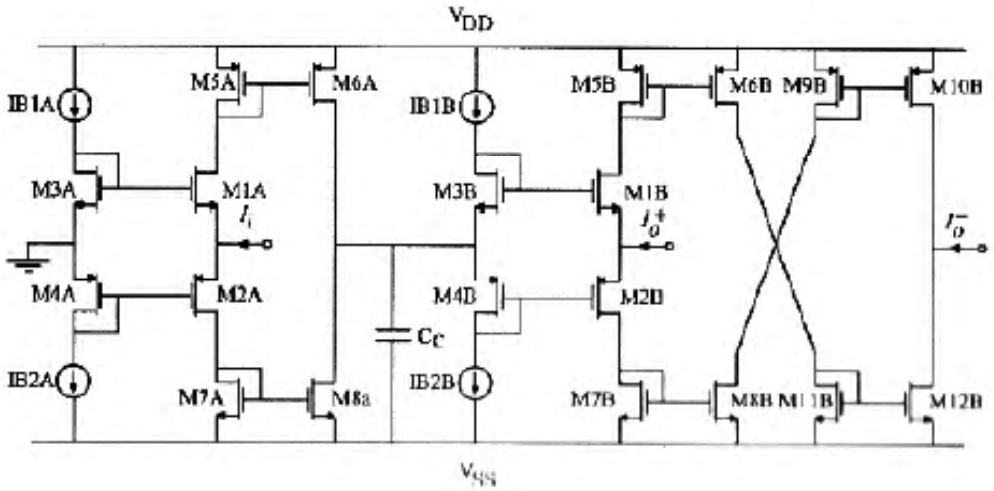


Figure 19-5th Design Example

Parameter	Value
Technology	2.4 μm
V_{DD}-V_{SS}	5 V
Gain	72 dB
GBW	3 MHz
M_ϕ	60 °
$T_{settl.}$(0.1%)	35 ns
Signal Range	± 700 μA

Current Comparators

- Current comparators can be used in applications such as Schmitt triggers, A/D converters, oscillators, etc. It detects the difference between two or more input currents and provides two level output current. Since current comparators interface digital circuits, voltage mode output is preferred.
- Current mirror comparator is given below. If i1>i2, output Vo goes to 1. Otherwise, it goes to 0.
- Both of the output transistors are not in saturation region M2-M4. One of them is in triode region and other one is in saturation. For this reason, its speed is not good.

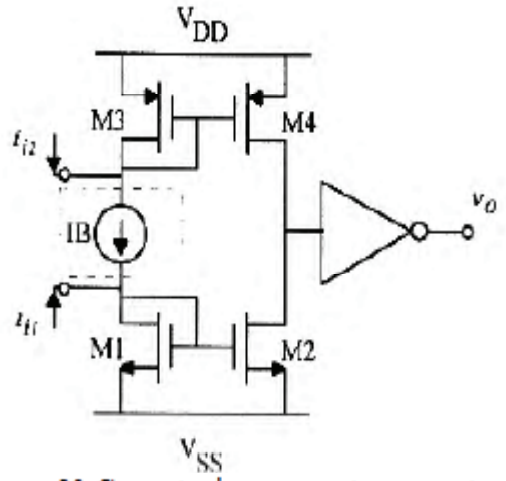


Figure 20-Current mirror current comparator

Current Comparators

Speed in comparators can be increased using pre-biasing method. It means setting operating point before compensation, so that circuit is put into best operating condition at the beginning. A switch shorts input and output of the inverter so that output of both comparator and inverter are set to $(V_{DD}+V_{SS})/2$. Use of cascode current sources increases the transresistance gain of the circuit.

Better frequency response can be obtained using of double folded cascode configuration as shown in Fig.21b. It uses common gate stages instead of current mirrors.

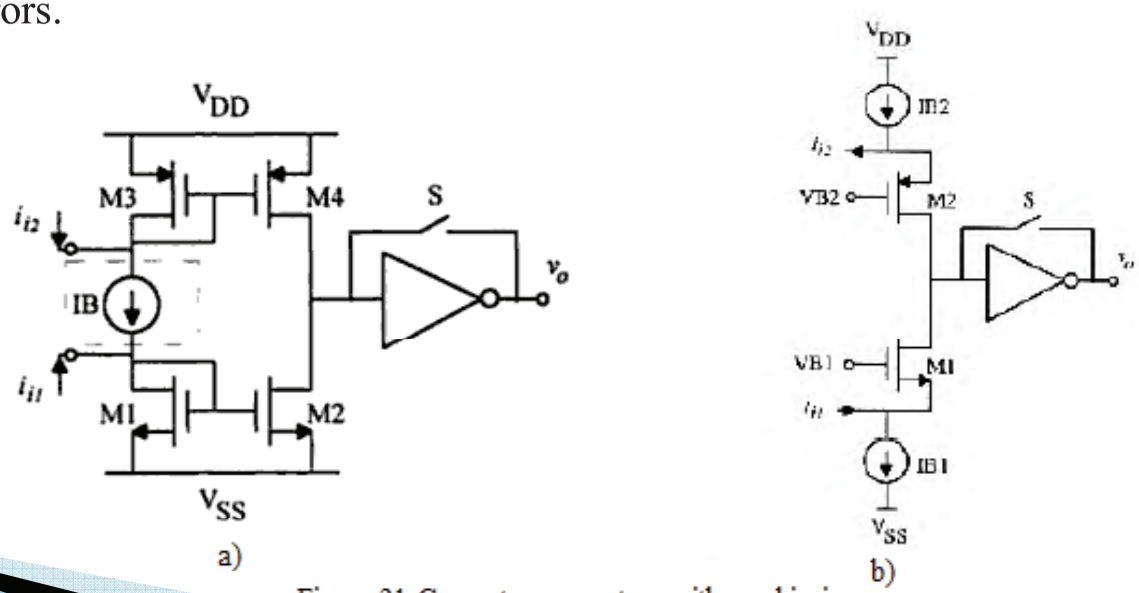


Figure 21-Current comparators with pre-biasing

Current Comparators

- **Design of Comparators**

- A well-defined low input reference is required to achieve high sensitivity.
- A well-defined input bias voltages is required in order to bias input generators to be properly biased.
- Well-controlled input and output bias currents are required in order to control time response and power consumption.

Offset Compensation

Offset is one of the most critical parameters in comparator design. High performance comparators are obtained using offset compensation techniques. Two different compensation techniques will be discussed next. Connecting compensation circuit in parallel or in series to uncompensated circuits together with charge injection error reduction methods are these techniques.

Current Comparators

- **Parallel connected compensation circuit**

Compensation circuit is based on hold capacitor, C_H, a switch SA and a transconductance stage that is connected in parallel to the uncompensated circuit.

Condition 1: SA is open, V_{CH}=0:

Output offset voltage: $V_{os} = (r_{o1} // r_{o2}) I_{os1} + g_m (r_{o1} // r_{o2}) V_{os2}$

Input offset current: $I_{os} = I_{os1} + g_m V_{os2}$

Condition 2: SA is closed: Transconductance stage is connected in unity gain configuration. Output offset voltage V_{osc} becomes:

$$V_{osc} = \frac{V_{os}}{1 + g_m r_o} \cong \frac{I_{os1}}{g_m} + V_{os2}$$

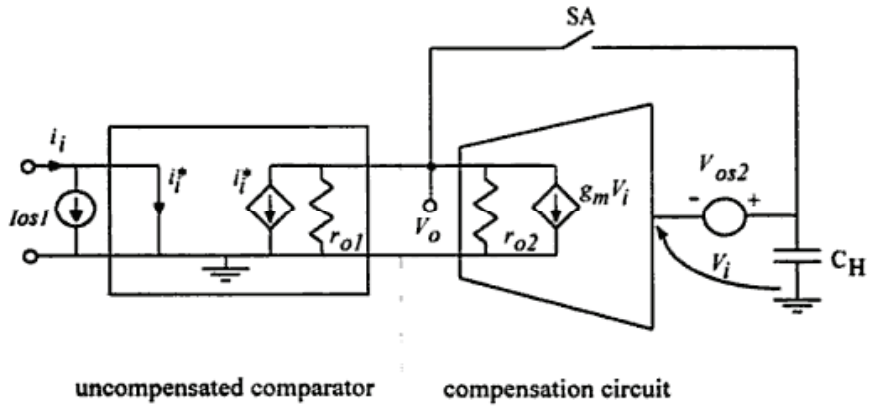


Figure 22-Block diagram of current comparator using parallel configuration

Current Comparators

- **Condition 3: SA is open:** $V_{CH} = V_{osc}$

Input offset current: $$I_{osc} = \frac{V_{osc}}{r_o} \cong \frac{I_{os}}{g_m r_o}$$

It is seen that input offset current I_{os} decreases after compensation. Input signal has to be fed after SA is opened. One sample to parallel compensation is given below where inverter is used as a gm stage and its input capacitance is used as C_H capacitor.

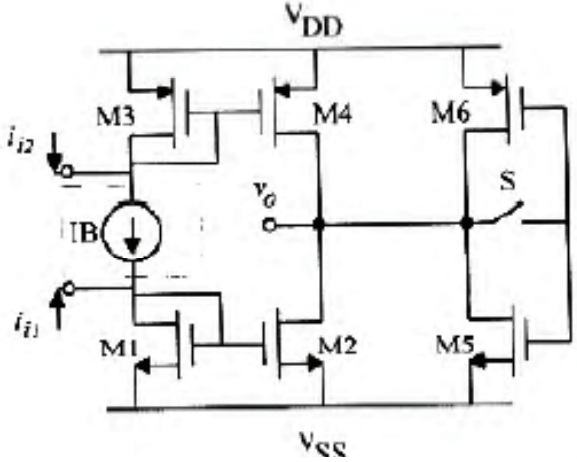


Figure 23- Current comparator circuit using parallel configuration

Current Comparators

- **Charge injection compensation:** When SA switch is opened, some charge is push into C_H capacitor. This charge gives rise to uncompensated offset. Charge injection error can be included in input offset current equation.

$$I_{osc} \cong \frac{I_{os}}{g_m r_o} + g_m \frac{\Delta Q}{C_H}$$

where ΔQ is the injected charge and $\frac{\Delta Q}{C_H}$ is the voltage at the input of transconductance stage due to charge injection.

An efficient solution is using differential transconductance stage as shown in Figure 24. For equal capacitances charge injection voltage is rejected by differential stage and it does not affect the comparator output.

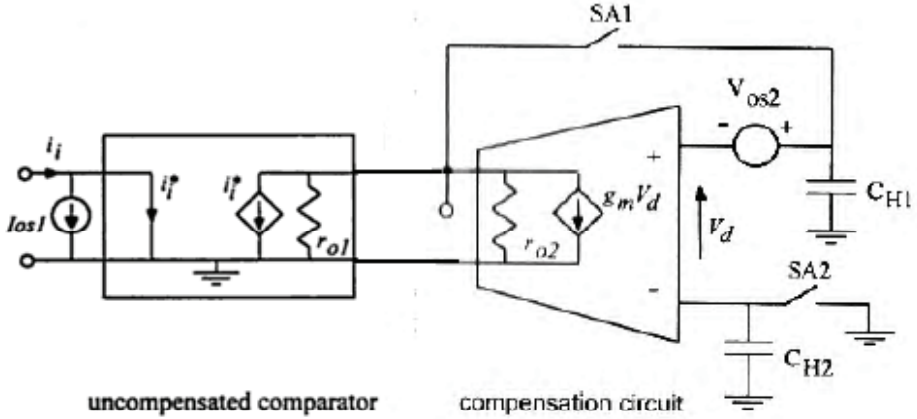
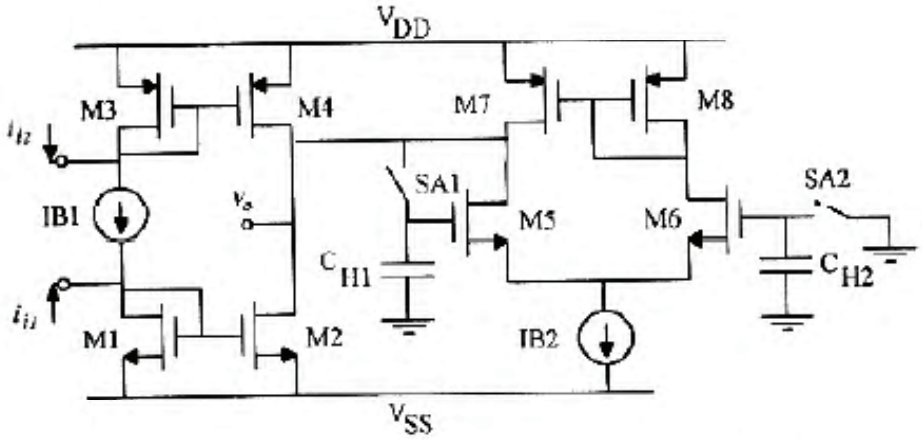


Figure 24-Block diagram of current comparator with offset and charge injection error compensation in parallel configuration

Current Comparators

- **An example circuit to parallel offset compensation:** In the first 20 ns, the circuit is uncompensated. During 20-60 ns switches are closed and offset is compensated. After 60 ns switches are opened and charge injection error occurs. Curve 2 shows the behavior of the charge injection compensated circuit. Curve 1 is the circuit without charge injection error compensation. In that circuit gate of M6 is connected to ground.



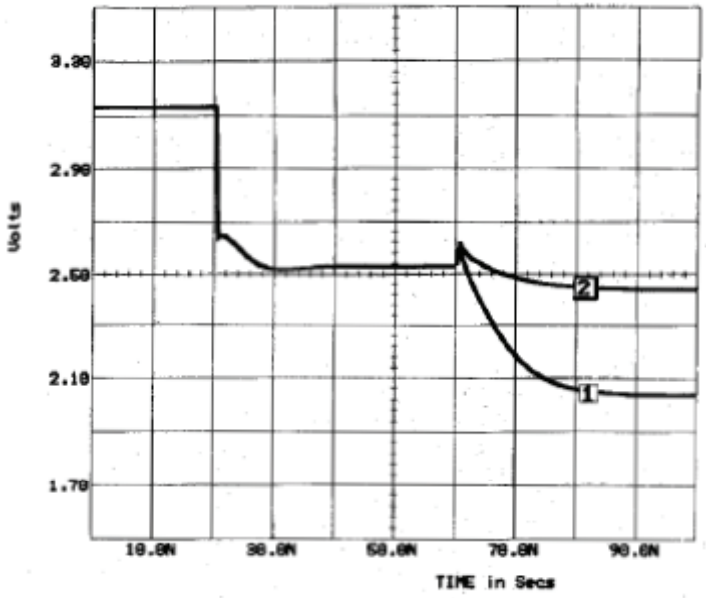


Figure 25-Offset and charge injection error compensated circuit in parallel configuration and its simulation result

Current Comparators

- **Series connected compensation**

In parallel configuration output resistance decreases and hence equivalent gain and sensitivity decreases. One approach is using high resistive output resistance and other one is series connected compensation circuit. In this configuration, MA transistor is used instead of transconductance element and A is an voltage amplifier. It is easy to obtain new equations. Transconductance in previous equations is replaced by $A_o g_{mA}$. New equations are given below.

Initial, SA is open: $$I_{os} = I_{os1} + A_o g_{mA} V_{os2}$$

After compensation, SA is open again: $$I_{osc} \cong \frac{I_{os}}{A_o g_{mA} r_o}$$

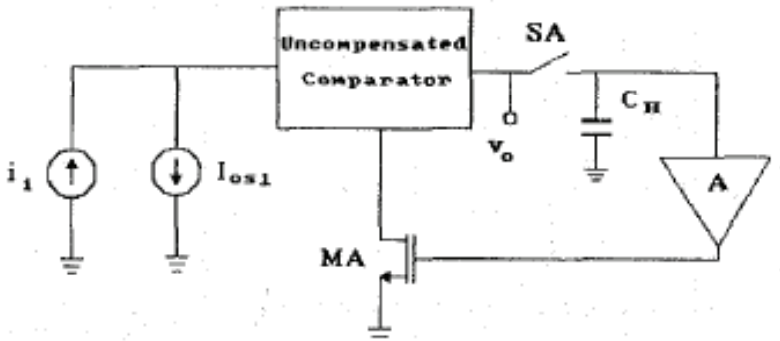


Figure 26-Block diagram of current comparator using series connected compensation circuit

Current Comparators

- **Series connected compensation example**

Block A in Fig.26 can be implemented with a source follower since the gain $g_{mA}r_o$ is high enough. Double folded cascode current comparator is used in this example.

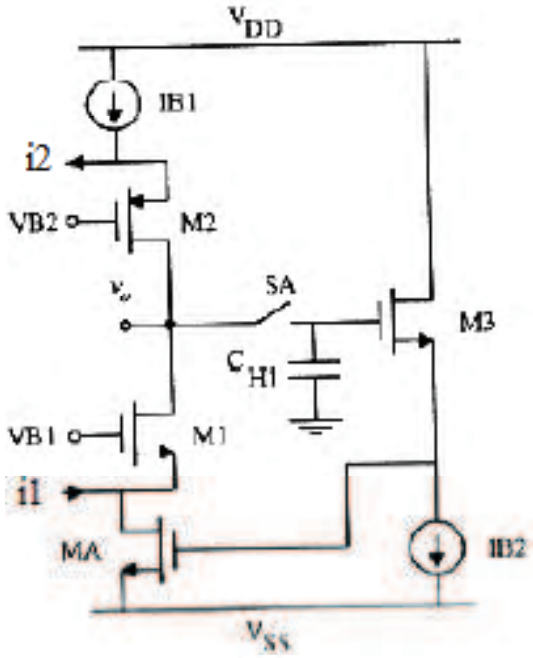


Figure 27-Current comparator circuit using series offset compensation

Current Comparators

- **Charge injection solution to series compensation**

  Charge injection problem discussed before can be solved using differential amplifier instead of block A shown before.

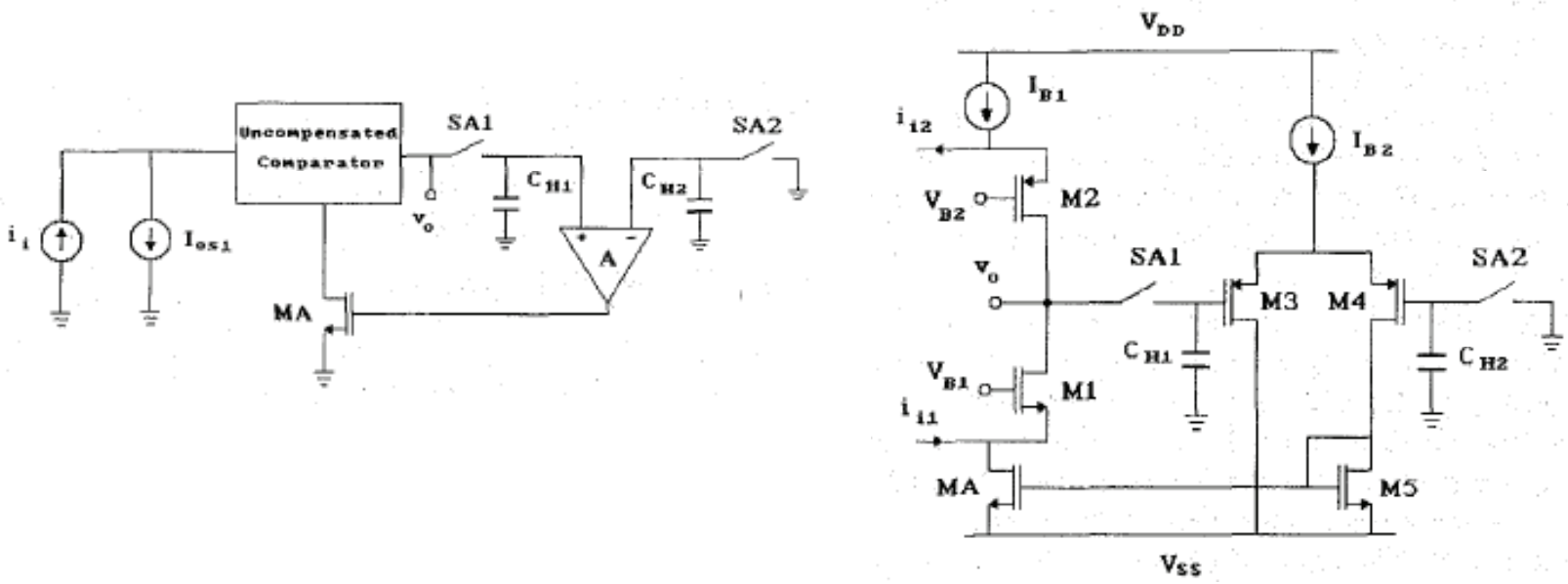


Figure 28-Block and transistor level implementations of offset and charge injection error compensated current comparator using series configuration

Comparator Design Examples[1]

In this example, input current is compared to 0. It consists of a transresistance amplifier M1-M19 and a series offset compensation circuit M20-M21, switch SA and hold capacitor C_H. Its operation principle is the same that was discussed before. Simulation time diagram consists of T1-T5 time intervals. At the beginning, SA is open. In T1 interval, comparator is uncompensated and output is in high position. In T2 interval SA is closed and comparator is compensated. Output goes to $(V_{DD}+V_{SS})/ 2$. In T3 interval, negative input current is applied. Output goes to low position. Then compensation is applied again and in T5 high input current is applied and output goes to high.

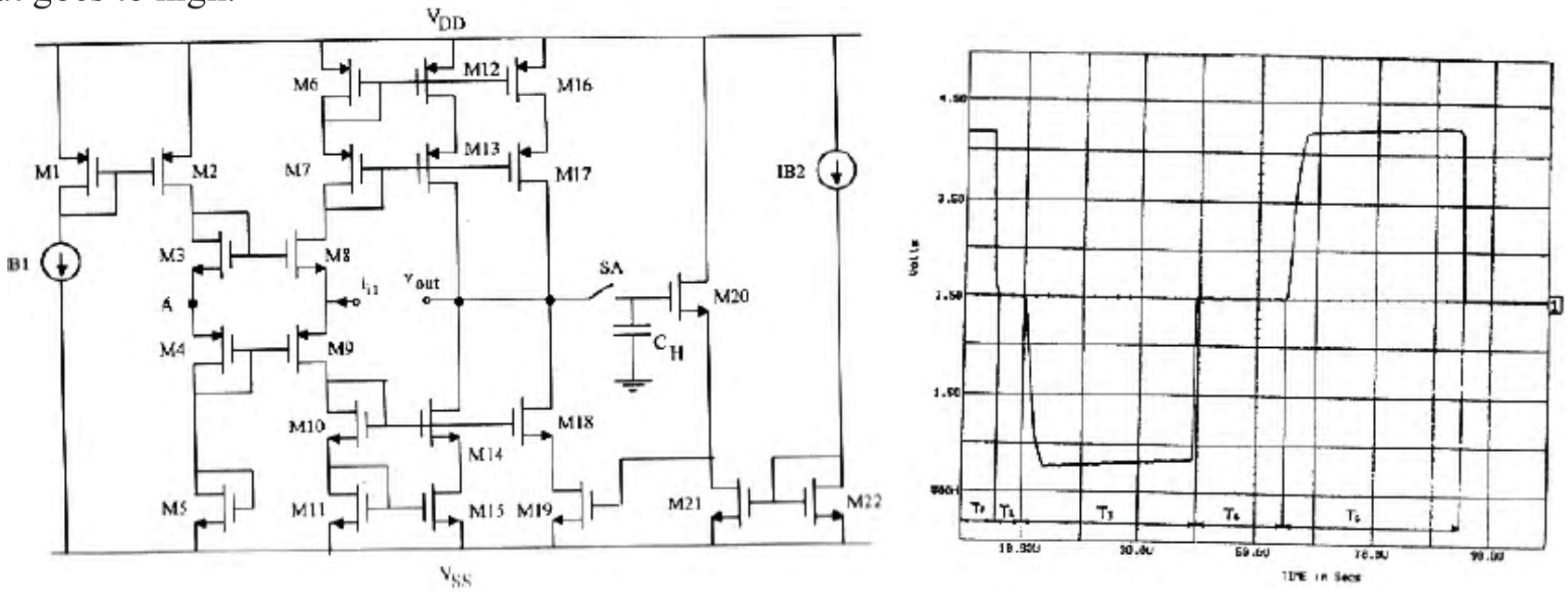


Figure 29-Current comparator design example 1 and its simulation result

Comparator Design Examples [2]

- **Fully differential comparator:** It is based on double folded cascode structure and includes a compensation circuit with offset and charge injection compensation.
- Compensation circuit consists of differential amplifier M9-M10, I_{B3}, hold capacitors and SA and SB switches. Uncompensated comparator is made up of M3-M6 transistors, M7-M8 current source transistors. M1-M2 and IB1-IB2 set input bias current and voltage.

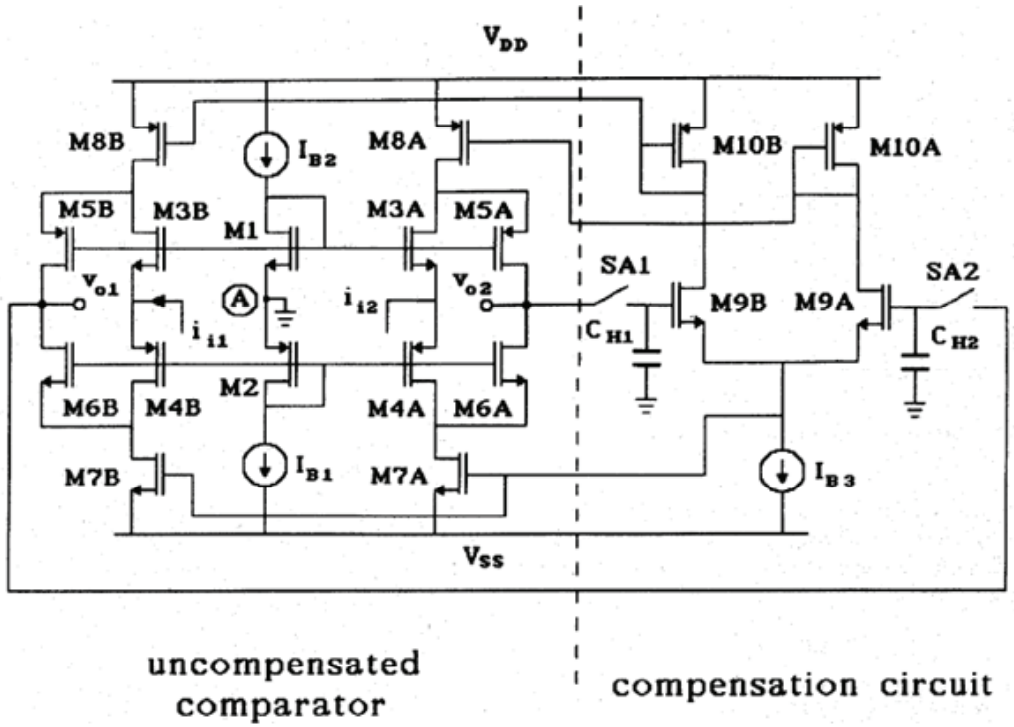


Figure 30-Current comparator design example 2

Comparator Design Examples [2]

- When SA and SB switches are opened, common mode output level and offset voltage are kept in hold capacitors. Charge injection error is also compensated, because it appears as a common mode signal. After compensation, input offset current is given as in the following equation:

$$I_{osc} \cong \frac{g_{m10}}{g_{m9}} \frac{I_{os}}{g_{m8} r_o}$$

$A=g_{m9}/g_{m10}$ and $g_{mA}=g_{m8}$

Simulation result for this circuit is given below where curve 1 is input current and curve 2 is output voltage.

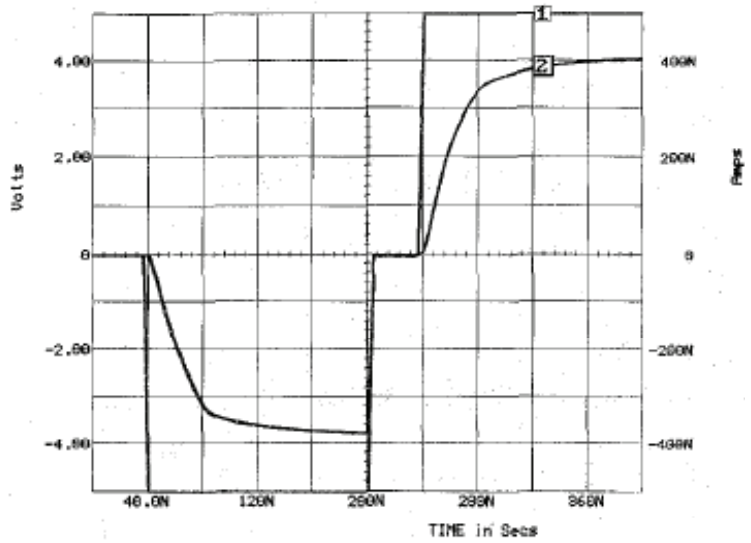


Figure 31-Simulation result of the circuit in Fig.30

References

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[2] E. A. M. Klumperink, H. J. Janssen, “Complementary CMOS Current Gain Cell”, Electronics Letters, Vol.27, pp.38-40

[3] Z. Wang, “Wideband Class AB Current Amplifier in CMOS Technology, ” Electronics Letters, Vol. 26, No:3, pp. 543-545, Apr. 1990.

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