High Frequency Transconductors

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High Frequency Transconductors

Current mode signal processing circuits have recently demonstrated many advantages over their voltage mode counterparts including increased bandwidth, higher dynamic range, and better suitability for operation in reduced supply environments (e.g. 3.3V). In addition, current mode processing often leads to simpler circuitry and lower power consumption.

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Traditionally, however, most analog signal processing has been accomplished using voltage as the signal variable. In order to maintain compatibility with voltage processing circuits, it is often necessary to convert the input and output signals of a current mode signal processor (CMSP) to voltages. Figure 5.1 shows a block diagram of a CMSP with the necessary interface circuits.

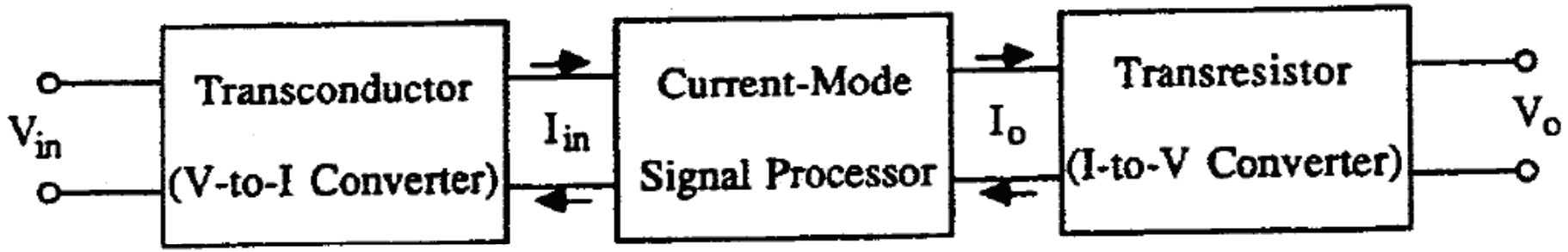

Figure 5.1: Current mode signal processing system

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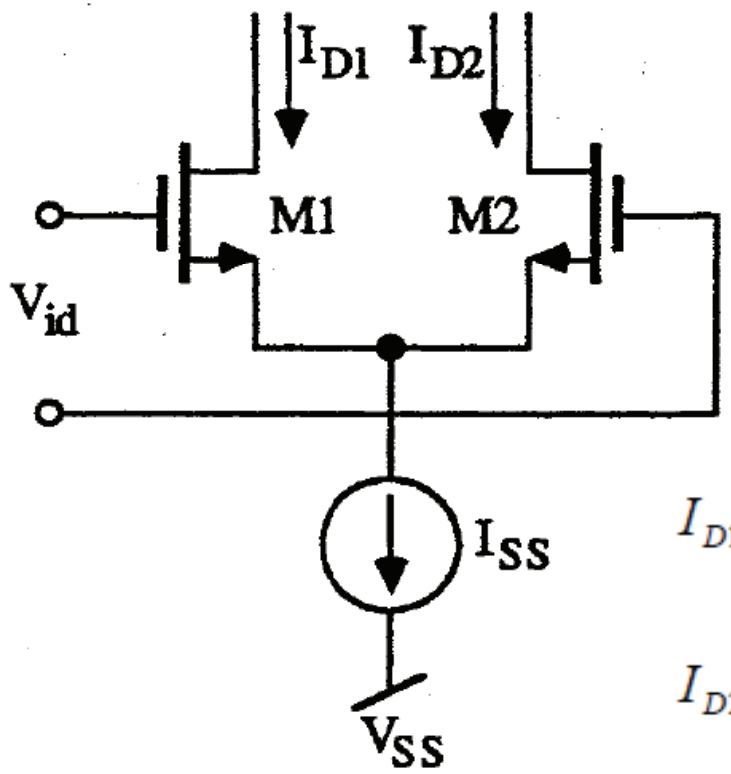

Figure 5.2: Differential pair transconductor

$$I_{D1} = \frac{\mu . C_{OX}}{2}\left(\frac{W}{L}\right)_1 \left[V_{GS1} - V_T\right]^2$$

$$I_{D2} = \frac{\mu . C_{OX}}{2}\left(\frac{W}{L}\right)_2 \left[V_{GS2} - V_T\right]^2$$

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Using the simplified square-law relationship for a MOSFET (described in Appendix B) in the saturation region and assuming M1 and M2 are perfectly matched, the output current is given by [1]

$$I_o = I_{D1} - I_{D2} = \begin{cases} \sqrt{2I_{SS}K}\, V_{id} \sqrt{1 - \frac{K}{2I_{SS}} V_{id}^2} & |V_{id}| \le \sqrt{\frac{I_{SS}}{K}} \\ I_{SS}\, \mathrm{sgn}(V_{id}) & |V_{id}| \ge \sqrt{\frac{I_{SS}}{K}} \end{cases} \qquad (5.1)$$

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The percent deviation in the transconductance from the small signal value of g_m is often used as a measure of linearity as well. The relationship between g_m and V_{id} can be developed by taking the derivative of (5.1) with respect to V_{id}, yielding

$$g_m = \frac{\sqrt{2I_{SS}K}\left[1 - \frac{KV_{id}^2}{I_{SS}}\right]}{\sqrt{1 - \frac{KV_{id}^2}{2I_{SS}}}}. \qquad (5.3)$$

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$$G_m = \left(\frac{d\Delta I_D}{d\Delta V_I}\right)_{\Delta V_I=0}$$

$$\frac{d\Delta I_D}{d\Delta V_I} = \frac{1}{2}\mu.C_{OX}\left[\frac{W}{L}\right].\sqrt{\frac{2I_{SS}}{\mu.C_{OX}\left[\frac{W}{2.L}\right]} - (\Delta V_I)^2}$$

$$-\frac{1}{2}\mu.C_{OX}\left[\frac{W}{L}\right].\frac{(\Delta V_I)^2}{\sqrt{\frac{2I_{SS}}{\mu.C_{OX}\left[\frac{W}{2.L}\right]} - (\Delta V_I)^2}}$$

$\Delta V_I = 0$

$$G_m = g_{m1} = g_{m2} = \sqrt{I_{SS}\,\mu.C_{OX}\left[\frac{W}{L}\right]}$$

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Nonlinearity

$$I_o = \sqrt{2I_{SS}K}\, V_{id} + 0 - \frac{1}{2\sqrt{2}} \frac{K^{3/2}}{\sqrt{I_{SS}}} V_{id}^3 + 0 - \ldots$$

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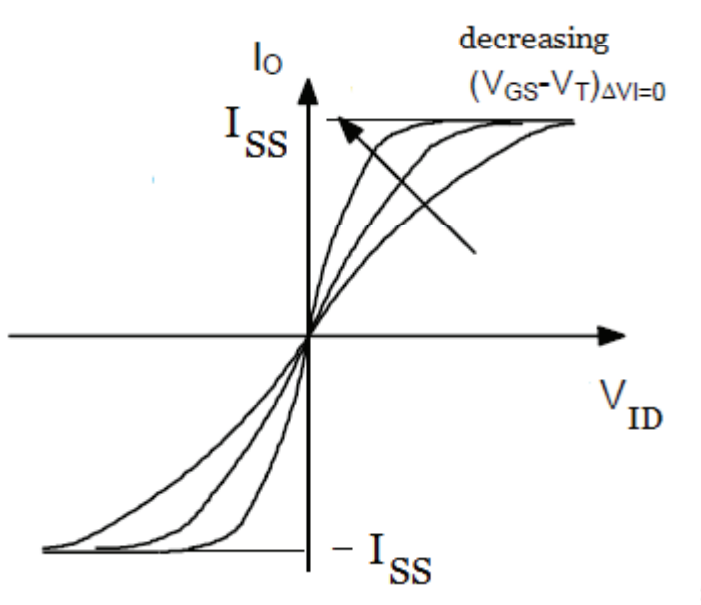

$$-\sqrt{\frac{2I_{SS}}{\mu.C_{OX}\left[\frac{W}{L}\right]}} \leq V_{ID} \leq \sqrt{\frac{2I_{SS}}{\mu.C_{OX}\left[\frac{W}{L}\right]}}$$

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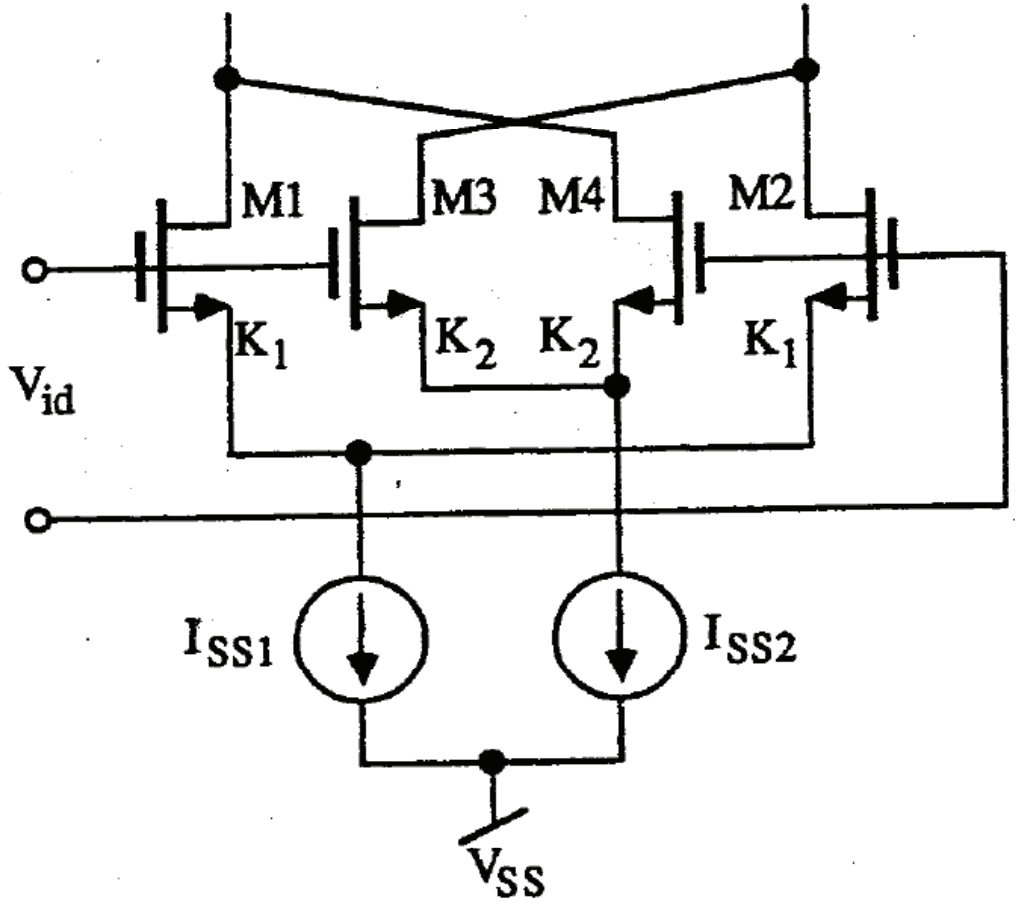

Figure 5.7: Cross-coupled differential pairs

5.2.5 *Cross-Coupled Differential Pairs*

A substantial increase in linearity can be obtained by simply cross-coupling two differential pairs [2] as shown in Figure 5.7. By properly scaling the ratio of W/L's and bias currents, approximate cancellation of the remaining odd order nonlinearities can be achieved.

$$\left[\frac{(W/L)_1}{(W/L)_2}\right]^{3/2} = \left[\frac{I_{SS1}}{I_{SS2}}\right]^{1/2} \tag{5.12}$$

providing $(W/L)_1 \neq (W/L)_2$ and $I_{SS1} \neq I_{SS2}$. This makes the coefficient of the nonlinear term identical for both pairs but the coefficient of the linear term different. The same result can be obtained directly from (5.1) by using the approximation $\sqrt{1-x^2} \approx 1-x^2/2$. When the output currents are subtracted, the nonlinear terms cancel resulting in a linear transconductance given by

$$g_m = g_{m1} - g_{m2} = \sqrt{2I_{SS1}K_1} - \sqrt{2I_{SS2}K_2}\,. \tag{5.13}$$

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5.3 Adaptively Biased Transconductors

5.3.1 Basic Principles

The concept of adaptive biasing can be best understood by referring back to the characteristic equation of the differential pair given in (5.1). Let the constant bias current I_{SS} be replaced by a voltage dependent bias current of the form

$$I_{SS} = I_{DC} + k' V_{id}^2 \qquad (5.16)$$

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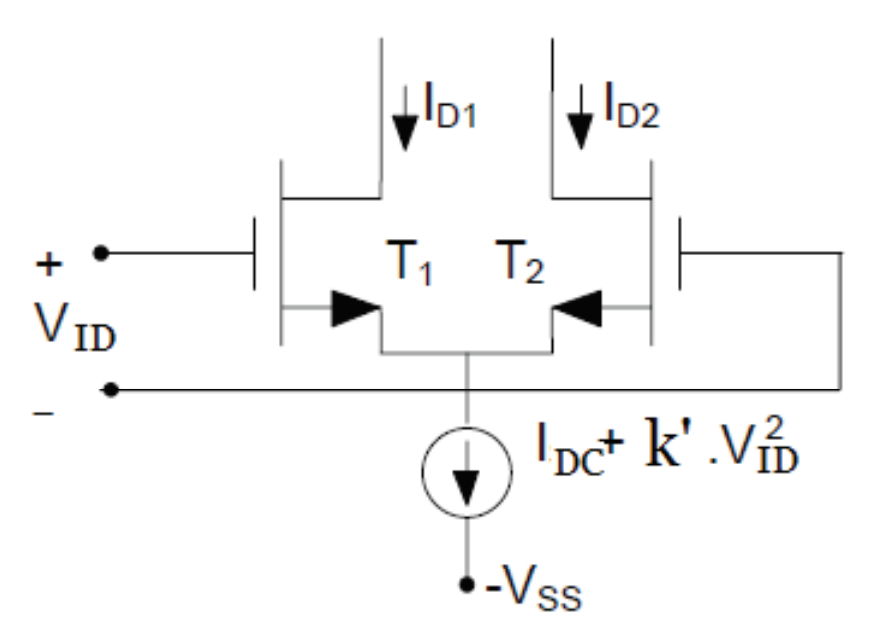

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$$I_o = I_{D1} - I_{D2} = \begin{cases} \sqrt{2I_{DC}K}\, V_{id} \sqrt{1 - \dfrac{K - 2k'}{2I_{DC}} V_{id}^2} & |V_{id}| \le \sqrt{\dfrac{2I_{DC}}{K}} \\ I_{DC} + k' V_{id}^2 & |V_{id}| \ge \sqrt{\dfrac{2I_{DC}}{K}} \end{cases} \qquad (5.17)$$

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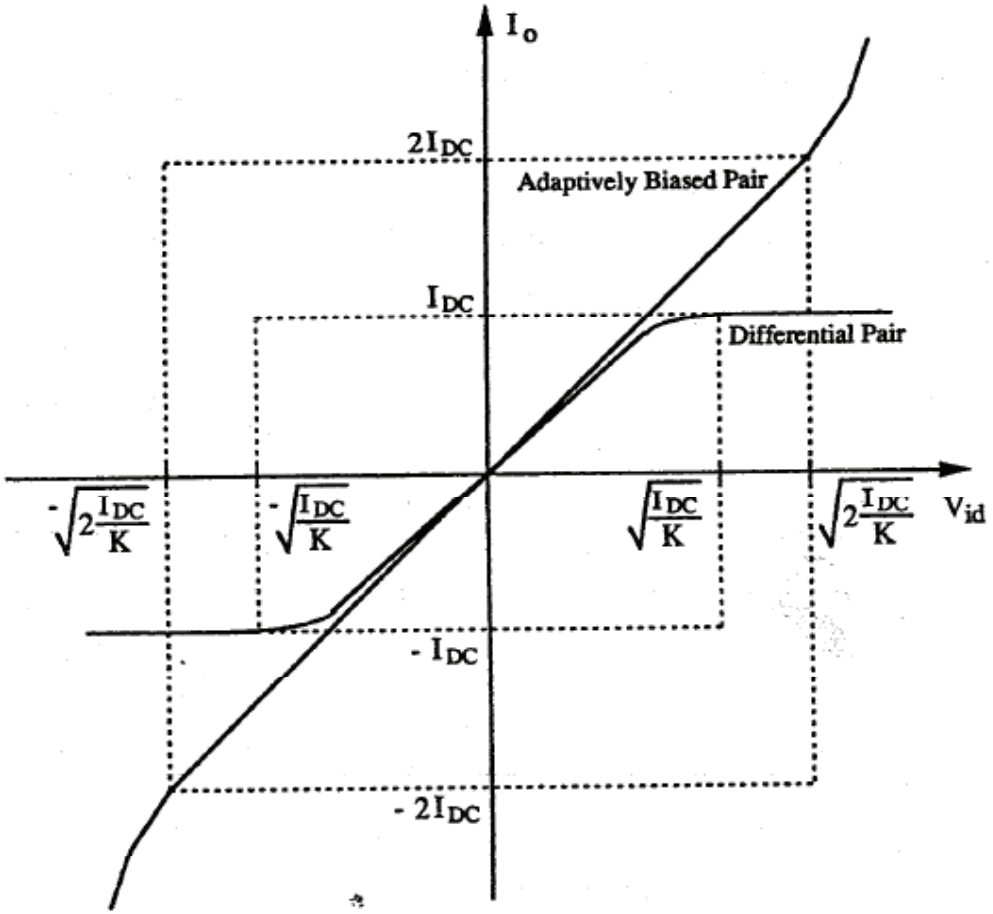

Figure 5.9: Transfer characteristics of differential pair with and without adaptive biasing

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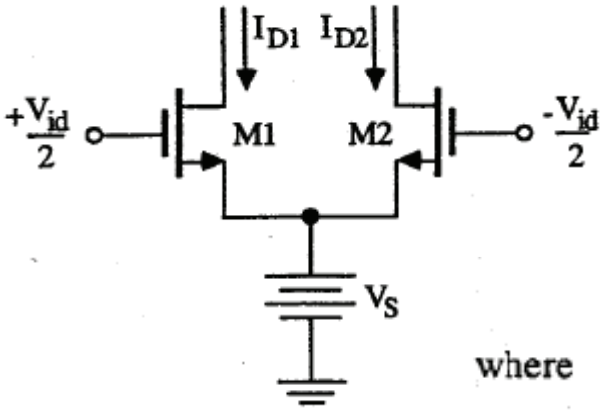

$$I_{D1} + I_{D2} = 2K\left(V_{CM} - V_T\right)^2 + \frac{K}{2}V_{id}^2 \qquad (5.21)$$

where

$$V_{CM} = V_{ic} - V_S \qquad (5.22)$$

provided both transistors remain active (i.e. $|V_{id}| \leq 2(V_{CM}-V_T)$). Note that (5.21) has the same form as (5.16), with

$$I_{DC} = 2K\left(V_{CM} - V_T\right)^2 \qquad (5.23)$$

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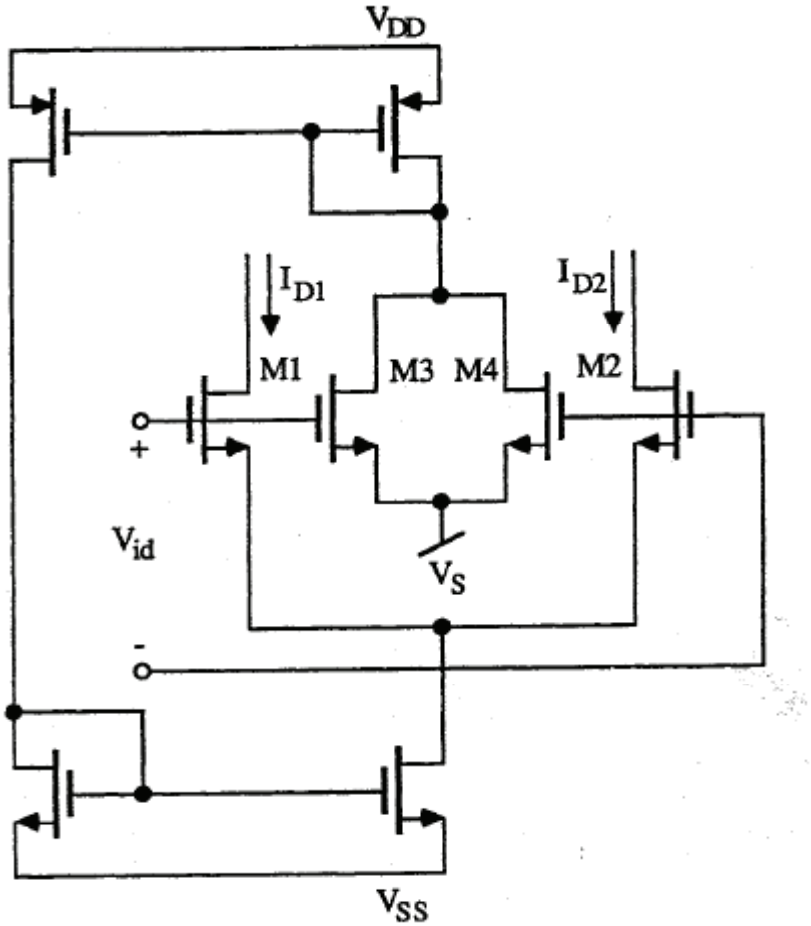

Figure 5.12: Adaptively biased differential pair using two transistor squaring circuit

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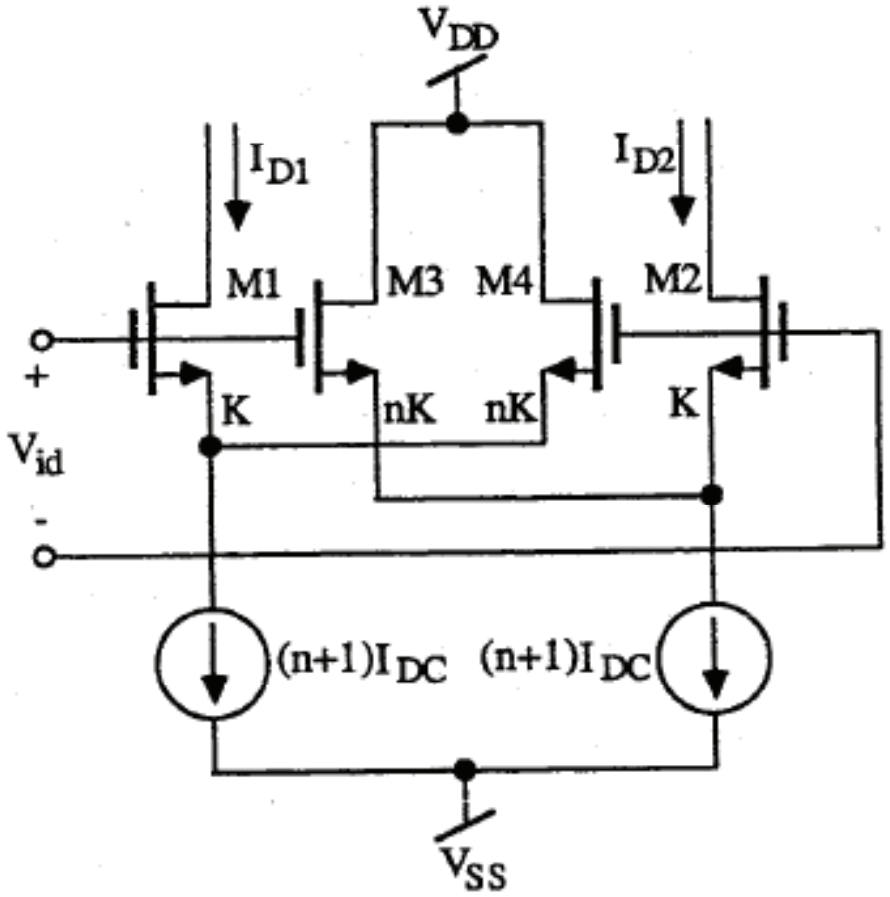

Figure 5.15: Cross-coupled quad cell

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5.3.3 *The Cross-Coupled Quad Cell*

Another popular circuit for the generation of a square law bias current is the cross-coupled quad cell shown in Figure 5.15 [5]. The circuit consists of two unbalanced differential pairs, each with one transistor n times larger than the other. The output is taken as the sum of the drain currents in the two smaller transistors. Assuming all devices are operating in the saturation region, these drain currents are

$$I_{D1} = I_{DC}\left[1 + \gamma x^2 + \frac{\alpha}{2} x \sqrt{1 - \beta x^2}\right] \tag{5.28}$$

$$I_{D2} = I_{DC}\left[1 + \gamma x^2 - \frac{\alpha}{2} x \sqrt{1 - \beta x^2}\right]$$

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where $x=V_{id}/\sqrt{I_{DC}/K}$ is the normalized input voltage and the remaining constants are defined as

$$\alpha = \frac{4n}{n+1}$$

$$\beta = \frac{n}{(n+1)^2}$$

$$\gamma = \frac{n(n-1)}{(n+1)^2} \qquad (5.29)$$

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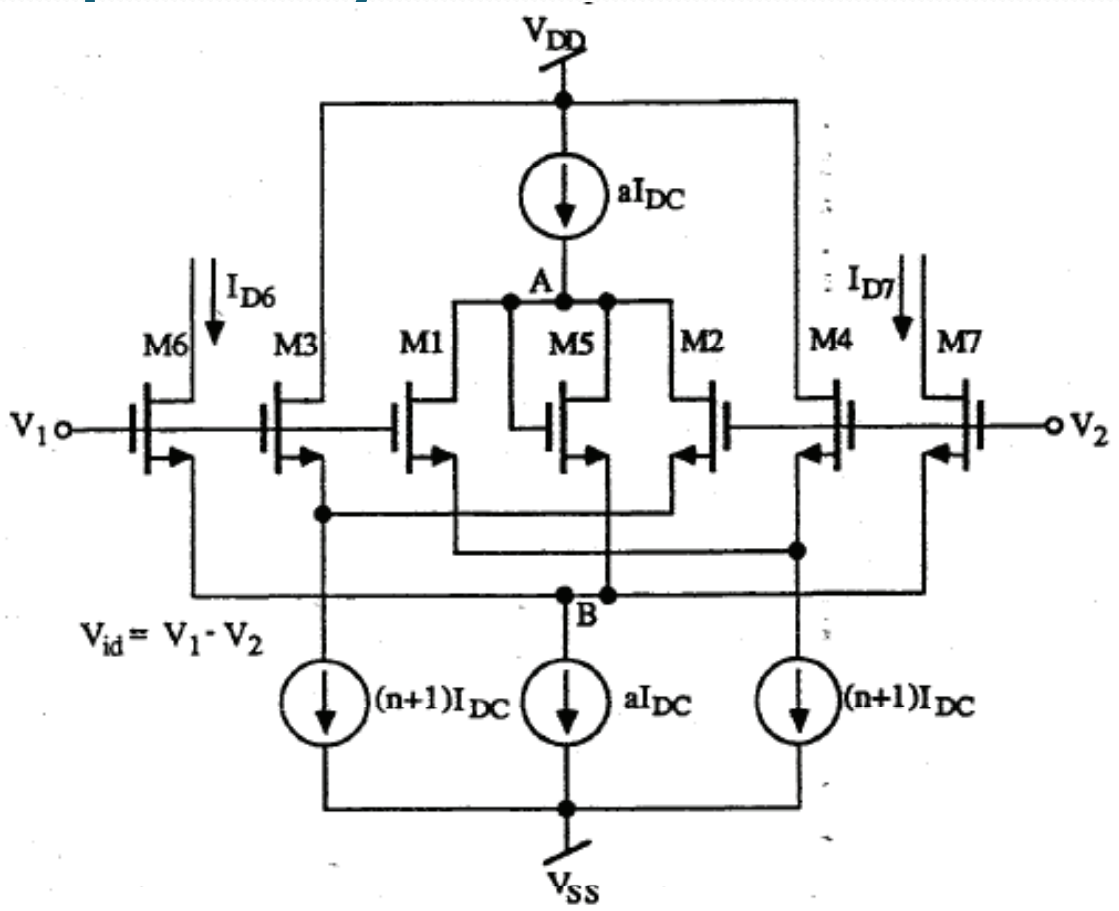

Figure 5.16: Adaptively biased differential pair using cross-coupled quad cell

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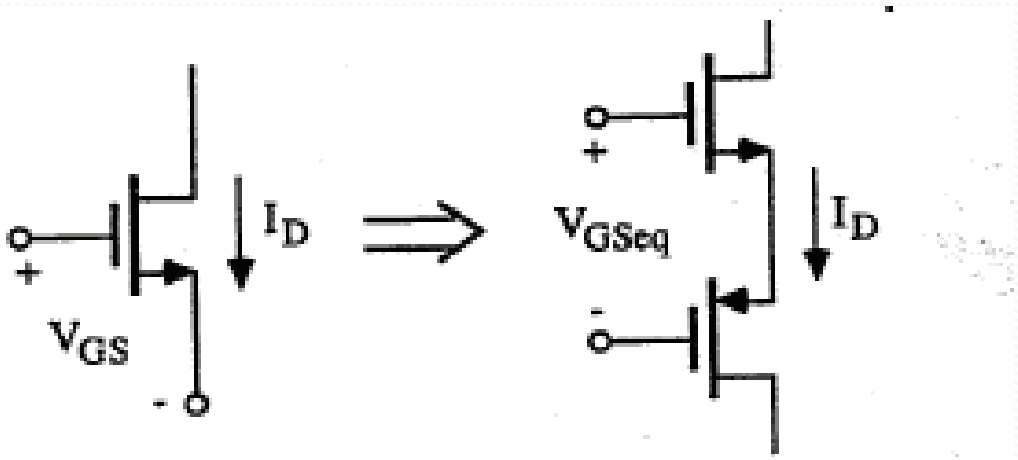

Figure 5.23: Replacing single transistor by CMOS double pair

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5.4.3 CMOS Double Pair

The class-AB mode of operation has been restricted to single channel MOS thus far due to the requirement of matched transistors. This limitation can be overcome by replacing each transistor with the CMOS double pair shown in Figure 5.23 [12]. Using the simple quadratic MOS model (see Appendix B), the gate-to-source voltage of each transistor is given by

$$V_{GSi} = \sqrt{\frac{I_D}{K_i}} + V_{Ti} \tag{5.44}$$

where V_{Ti} is the bulk dependent threshold voltage (see (B.5)). The equivalent gate-to-source voltage $V_{GSeq}=V_{GSN}+V_{GSP}$ of the CMOS double pair is then given by

$$V_{GSeq} = \left(\frac{1}{\sqrt{K_N}} + \frac{1}{\sqrt{K_P}}\right)\sqrt{I_D} + V_{TN} + |V_{TP}| \tag{5.45}$$

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$$= \sqrt{\frac{I_D}{K_{eq}}} + V_{Teq}$$

where

$$V_{Teq} = V_{TN} + |V_{TP}| \tag{5.46}$$

$$K_{eq} = \frac{K_N K_P}{\left(\sqrt{K_N} + \sqrt{K_P}\right)^2}.$$

Therefore, a pair of opposite polarity MOS transistors acts as a single transistor with an equivalent threshold voltage and transconductance parameter given by (5.46).

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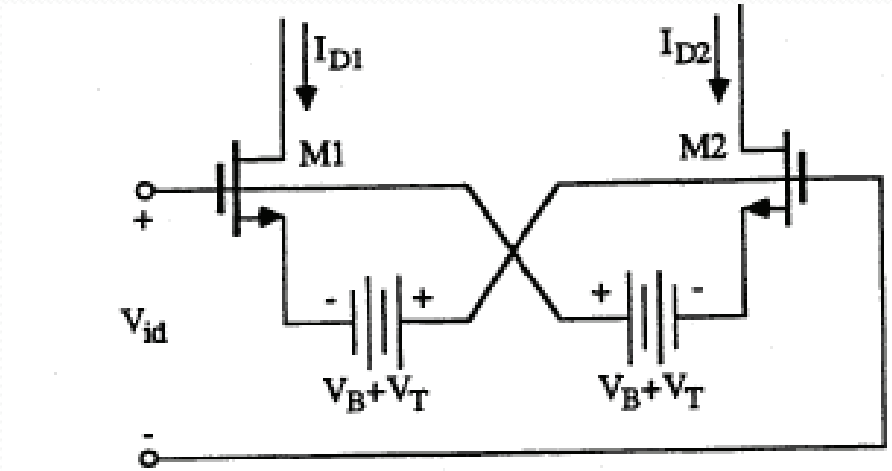

Figure 5.25: Linear MOS transconductor circuit principle

$$V_{GS1} + V_{GS2} = 2(V_B + V_T)$$

$$V_{GS1} - V_{GS2} = 2V_{id}.$$

$$I_o = I_{D1} - I_{D2} = (4KV_B)V_{id}.$$

The transconductance $g_m = 4KV_B$ is perfectly linear and can be tuned by changing the bias voltage V_B.

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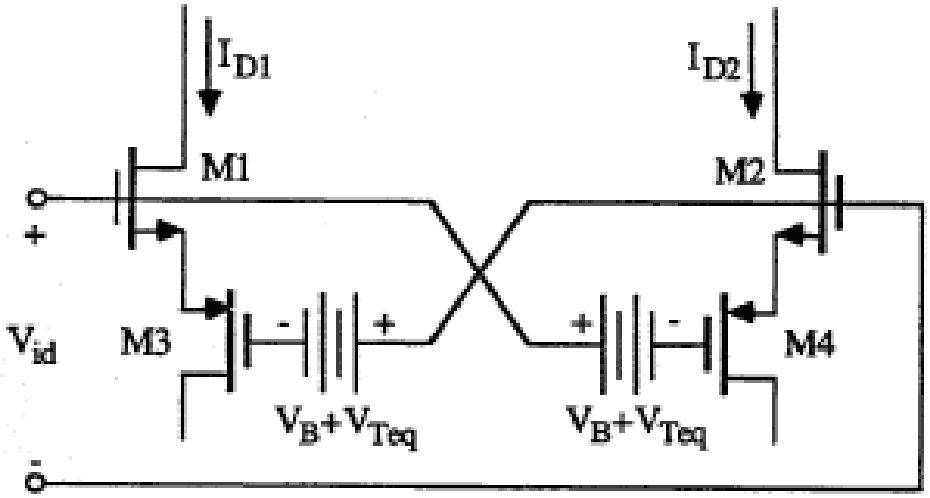

Figure 5.26: Replacing input transistors by CMOS double pairs

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$$V_B = \sqrt{\frac{I_B}{K_{eq}}}$$

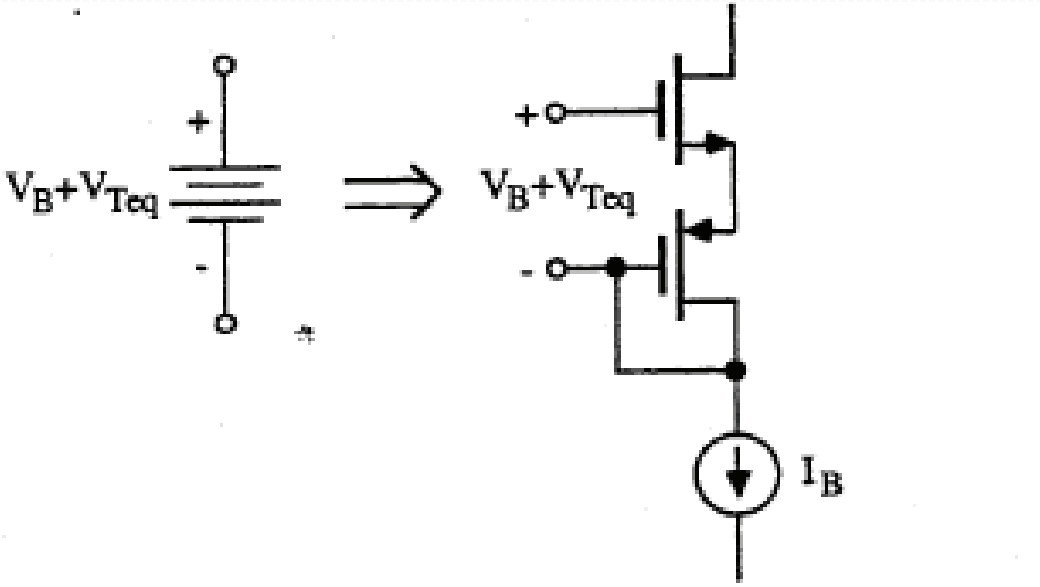

Figure 5.27: Double pair implementation of a floating voltage source

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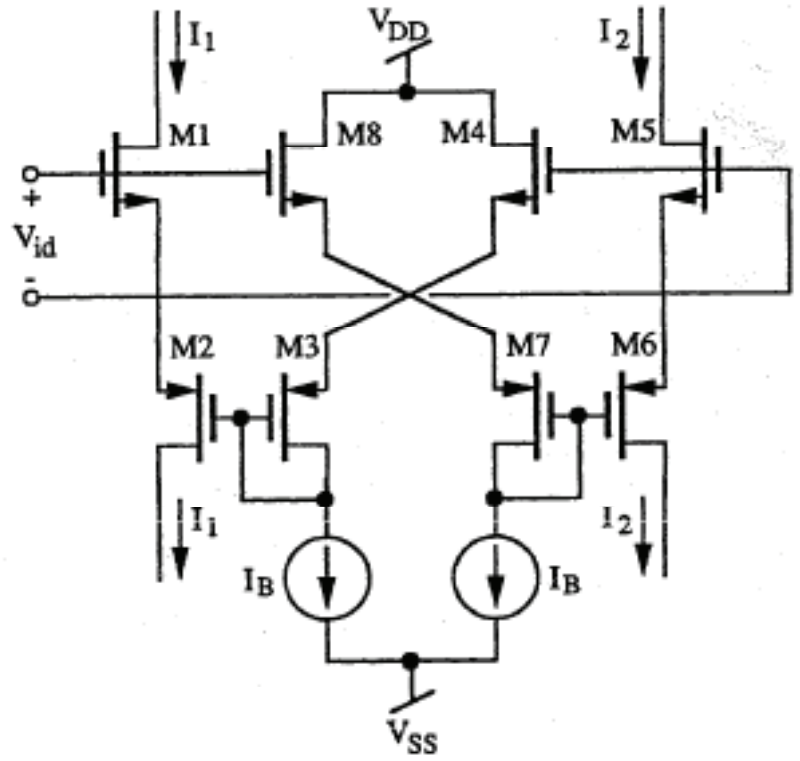
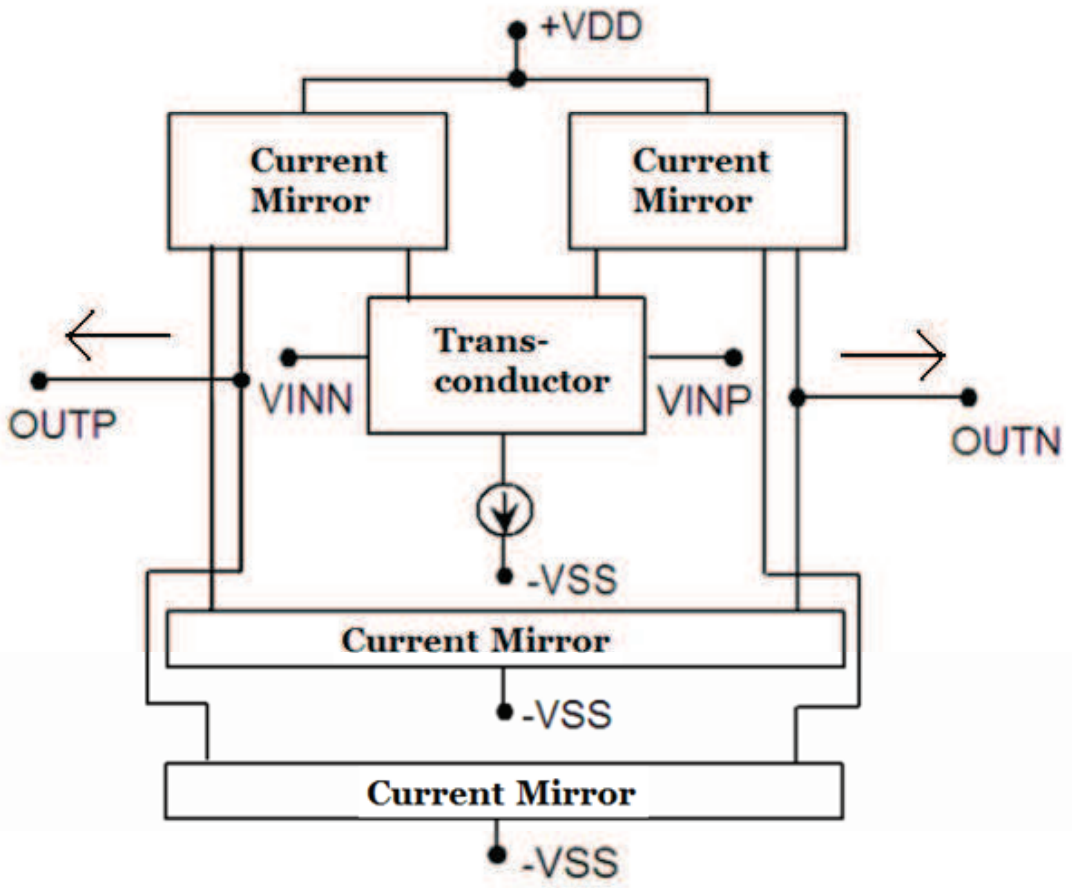


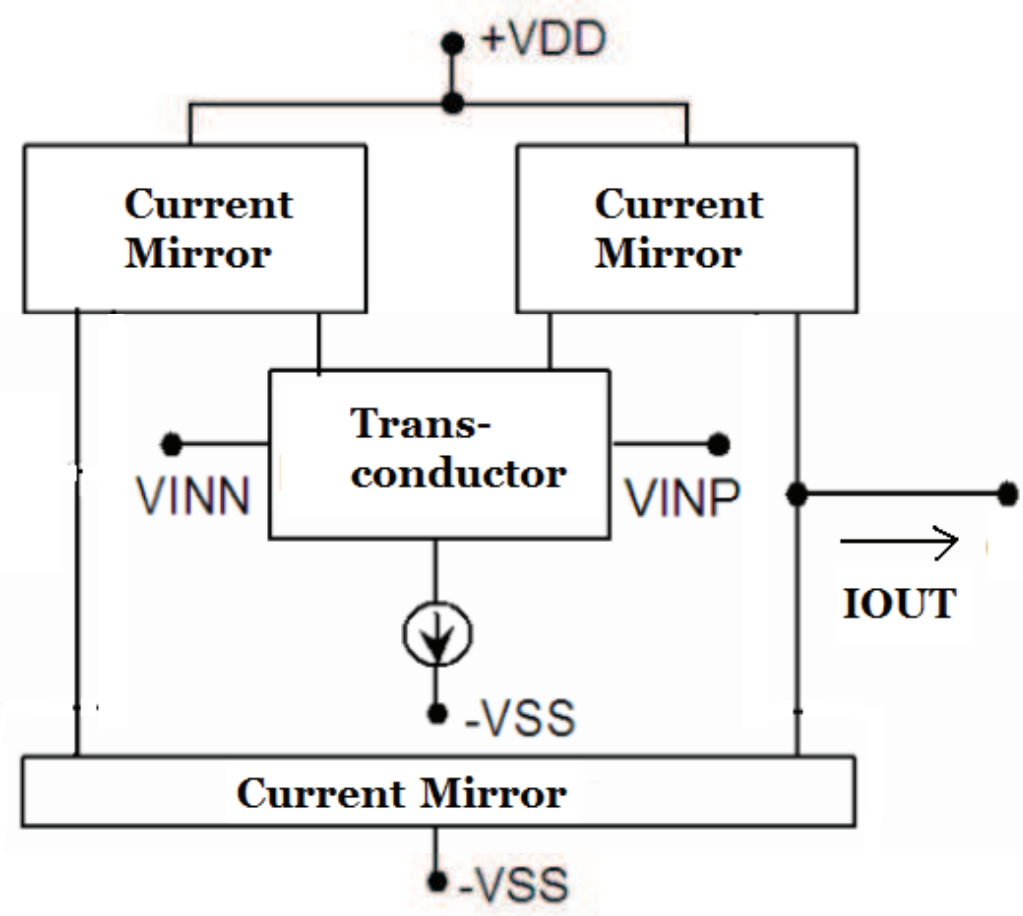
Figure 5.28: Cross-coupled double quad transconductor

$$I_o = I_1 - I_2 = 4\sqrt{I_B K_{eq}}\, V_{in} \qquad |V_{in}| \le \sqrt{\frac{I_B}{K_{eq}}}\,.$$

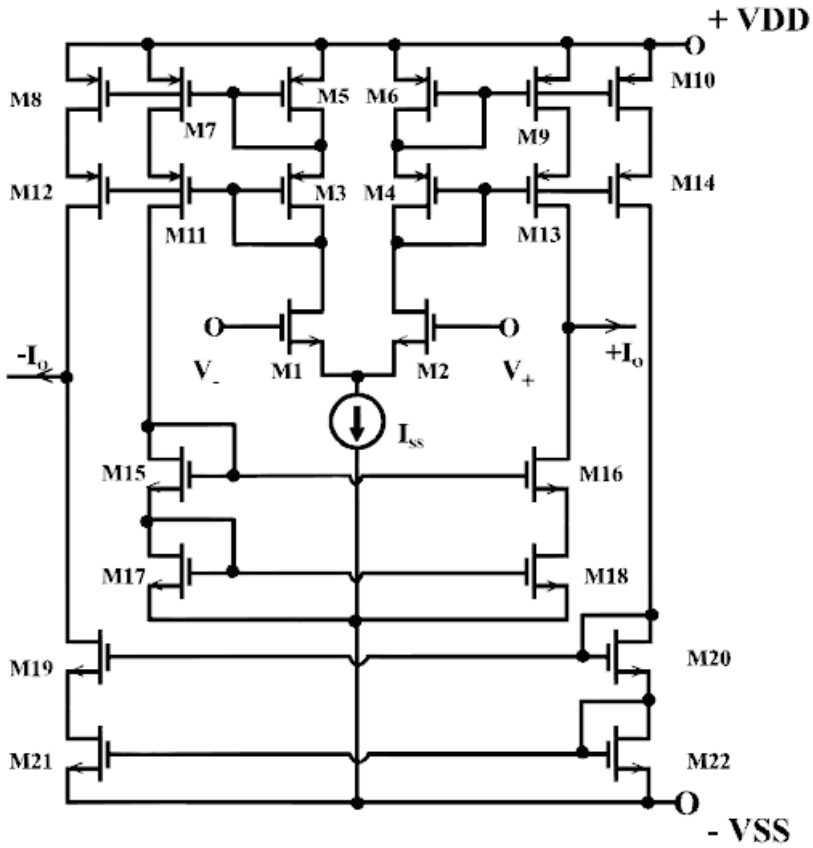
Conversion to single-end



Conversion to single-end

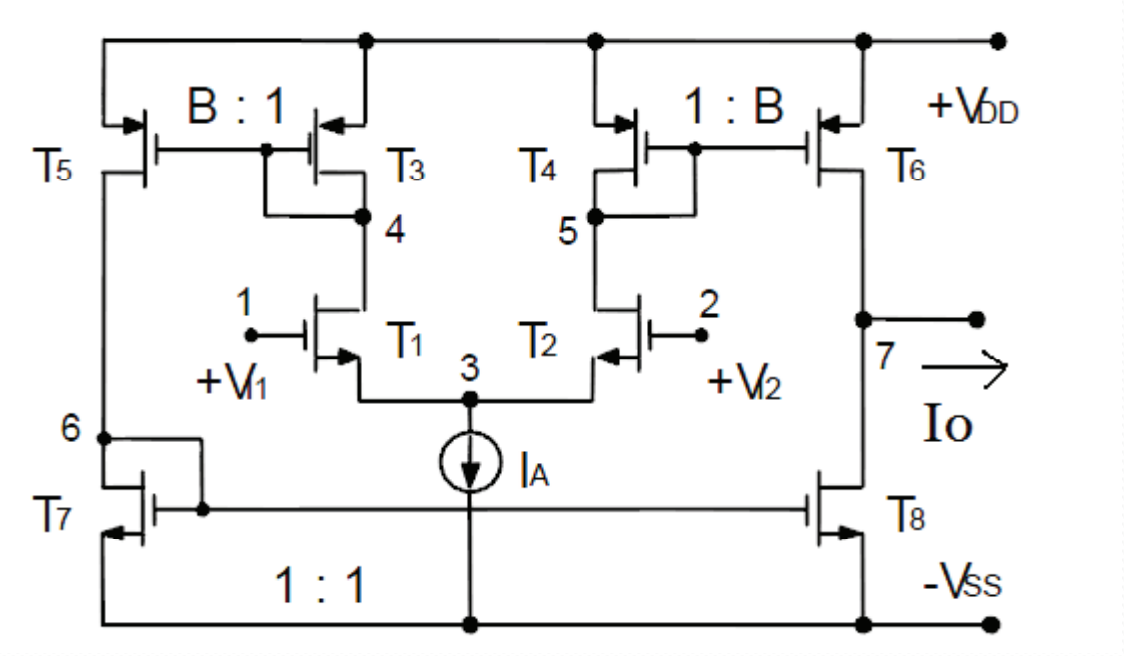


Examples, CMOS Cascode-DOTA



CMOS cascode DO-OTA structure

Examples, CMOS OTA



References

- 1. C. Toumazou, F.J. Lidgey, D.G. Haigh (ed.), Analog IC design: the current-mode approach, Peter Peregrinus Ltd., 1998.

  2. P.R. Gray, P.J. Hurst, S.H. Lewis, R.G. Meyer, Analysis and design of analog integrated circuits, John Wiley & Sons, Inc., 2001.

- 3. G. Palmisano, G. Palumbo, S. Pennisi, CMOS current amplifiers, Kluwer Academic Publishers, 1999