High Drive Current Amplifiers

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Current Mode Analog Circuit Design

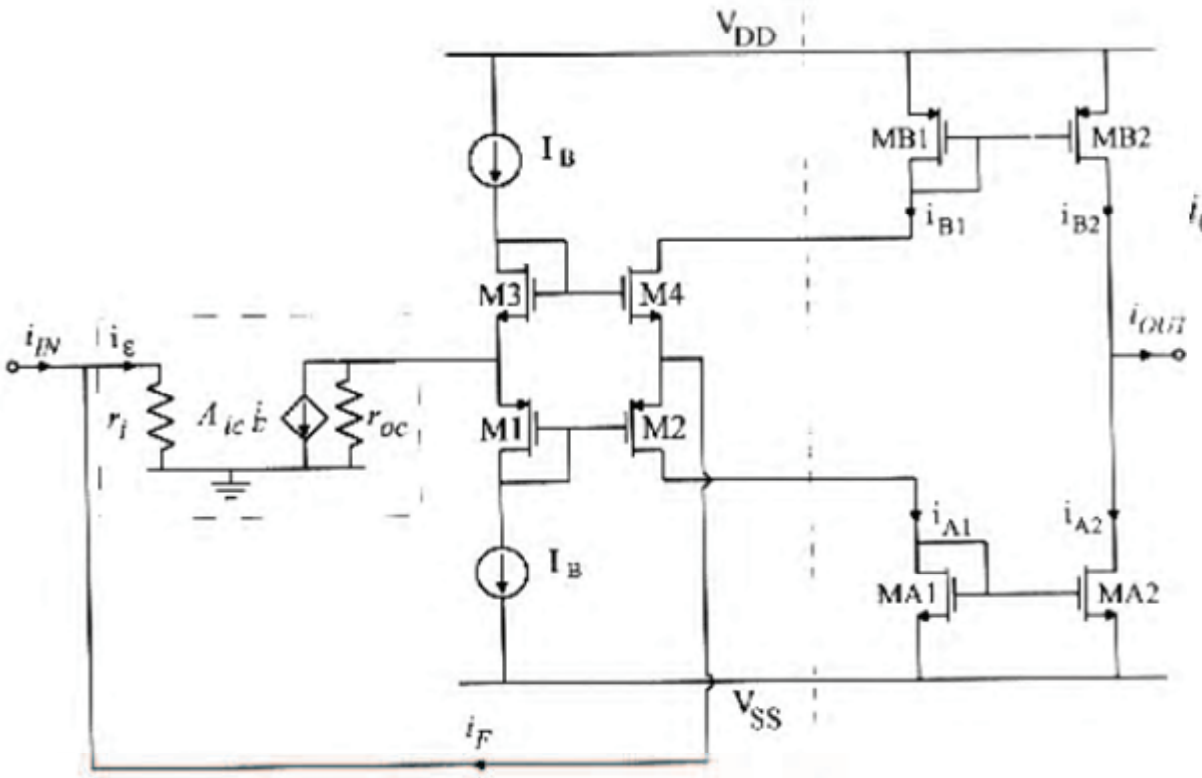
Overview

- Class AB Current Output Stages
- Harmonic Distortion Due to Channel Length Modulation
- Harmonic Distortion Due to Mismatches
- Design Examples

Class AB Output Stages

- Current mode power amplifiers use a current output stage (COS) which is able to drive a grounded load.
- COS is the most critical block for implementing a high drive current amplifier.
- In brief a current amplifier is made up of a transresistance amplifier low input resistance and high gain and a class AB COS which has to provide high drive capability and high output resistance.

Class AB Output Stages – General Current Amplifier Structure



$$i_{OUT} = i_{B2} - i_{A2}$$

$$i_{OUT} = i_{B1} - i_{A1} = i_F \cong -i_{IN}$$

Transresistance Amplifier COS

Figure-1

Class AB Output Stages – Nonidealities

- A COS has two main sources of non-ideality which cause deviation from, the ideal DC transfer characteristic and affect linearity
  - The channel-length modulation error of the mirroring transistor (MA2 MB2 in Fig. 1);
  - The mismatches between the transistors in the current mirror.
- Channel-length modulation is caused by differences in the drain-source voltage of the transistors. It can be reduced by increasing their channel length, however, this means larger chip area and worse frequency response.
- Mismatch errors affect any topology and can only be eliminated with a careful layout.

Class AB Output Stages – Configurations

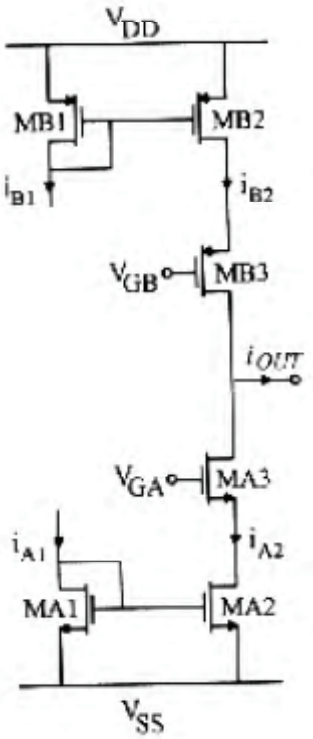


Figure - 2

- COS based on regular cascaded mirrors.
- The circuit exhibits high output resistance and swing, but any strategy allowing the drain voltage to track the gate voltage in the output transistors (MA2 and MB2) is lacking. Channel length modulation still limits linearity.

Class AB Output Stages – Configurations

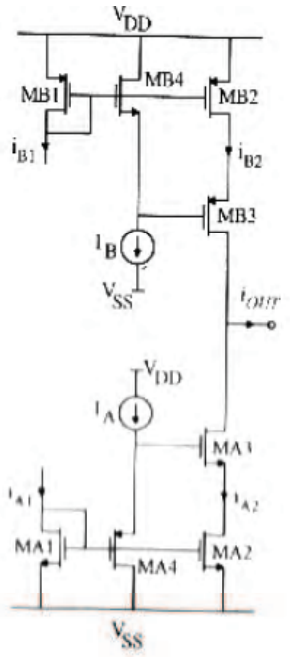


Figure - 3 *Cascoded current output stage with dynamic matching*

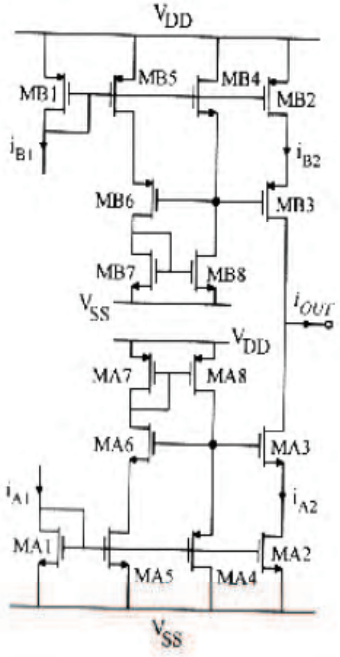


Figure - 4 *Cascoded current output stage with improved dynamic matching*

A first solution which reduces channel-length modulation is using the cascoded mirror with dynamic matching shown in Fig. 2. It exhibits a reduced non-linearity by a factor of 2 thanks to the following action of common drain MA4 (MB4).

A better solution for reducing harmonic distortion due to channel length modulation is achieved by implementing the COS using a current mirror with improved dynamic matching as in Fig. 3.

Class AB Output Stages – Configurations

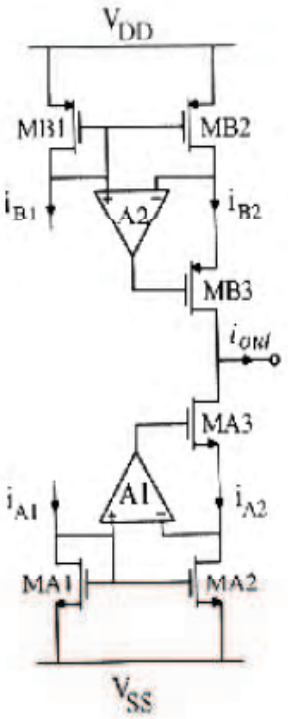


Figure - 5

Gain-boosted cascoded current output stage

- Final COS is made up of two complementary active-gain enhanced mirrors which base their performance on a principle quite similar to the gain-boosting technique. The two current mirrors are composed of transistors MA1-MA3 and MB1–MB3 and two auxiliary voltage amplifiers, Al and A2. Thanks to these, the drain voltages of MA1, MA2 and MB1, MB2 are almost equal even for large currents. Thus, a COS with high linearity performance is achieved. The use of A1 and A2 also provides a very high output resistance.

$$r_o \cong \left(g_{mA3} r_{dA2} r_{dA3} A_1\right) \| \left(g_{mB3} r_{dB2} r_{dB3} A_2\right)$$

Harmonic Distortion Due to Channel Length Modulation – Regular Cascoded COS

- Harmonic distortion due to channel length modulation is obtained for regular cascoded current mirror assuming all transistors are matched.

$$HD_2 \cong \frac{\lambda_N - \lambda_P}{4}\sqrt{\frac{I_Q}{\beta}}\left(\frac{3}{2}\sqrt{\frac{I_M}{I_Q}} - 1\right)$$

I_M => Magnitude of Sinusoidal Input Current

I_Q => Quiescent Current

$$HD_3 \cong \frac{\lambda_N + \lambda_P}{8}\sqrt{\frac{I_Q}{\beta}}\left(\sqrt{\frac{I_M}{I_Q}} - 1\right)$$

Harmonic Distortion Due to Channel Length Modulation – Regular Cascoded COS

- As expected from current mirrors with ideally matched transistors and equal transconductance gain, the even-order harmonic distortion is very low. In fact, it is proportional to the difference between the two channel-length modulation parameters. Therefore, third-order harmonic distortion becomes the dominant contribution.
- Harmonic distortions HD2 and HD3 are dependent upon the relative magnitude of the input signal and λp and λn. They can be reduced by increasing the transconductance gain and/or the channel length of the transistors.
- For dynamic matching type cascoded COS, HD2 and HD3 terms are reduced by a factor of 2

Harmonic Distortion Due to Channel Length Modulation –Cascoded COS with Improved Dynamic Matching

- HD2 is proportional to the channel-length modulation coefficients and to the differences between V_{TN} and V_{TP}.
- The improved dynamic matching makes third order harmonic distortion term almost negligible.

$$HD_2 \cong \frac{2}{3\pi}\left[\lambda_N\left(\left|V_{TP\,A4}\right| - V_{TN\,A3}\right) - \lambda_P\left(V_{TN\,B4} - \left|V_{TP\,B3}\right|\right)\right]$$

$$\frac{2}{3\pi}\left(\lambda_N + \lambda_P\right)\left(\left|V_{TP}\right| - V_{TN}\right)$$

$$HD_3 \cong 0$$

Harmonic Distortion Due to Channel Length Modulation- Gain Boosted Cascoded COS

- HD2 and HD3 depend on the difference and the sum of λp and λn respectively. However the topology provides a very low-distortion COS because HD2 and HD3 are greatly reduced by the amplifier gain.

$$HD_2 \cong \frac{\lambda_N - \lambda_P}{8(1+A)\sqrt{\beta}}\left(\frac{2I_M - I_Q}{\sqrt{I_M}}\right)$$

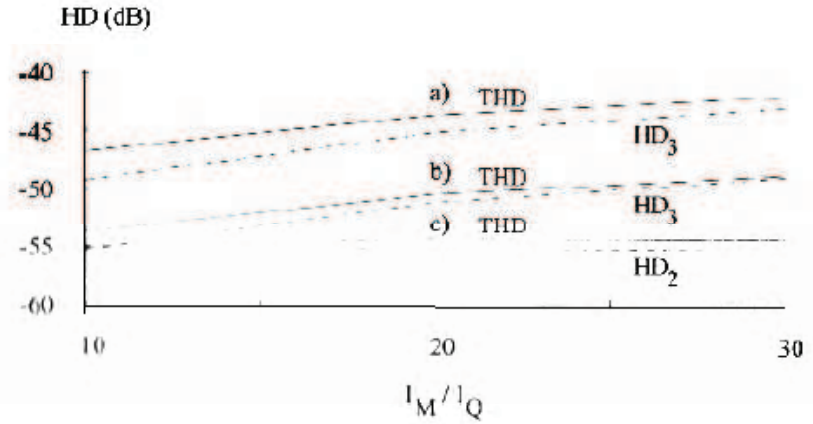
$$HD_3 \cong \frac{\lambda_N + \lambda_P}{24(1+A)}\sqrt{\frac{I_Q}{\beta}}\left(2\sqrt{\frac{I_M}{I_Q}} - 1\right)$$

I_M => Magnitude of Sinusoidal Input Current

I_Q => Quiescent Current

A => Amplifier Gain

Harmonic Distortion Due to Channel Length Modulation- Simulation Results



a) Regular Cascoded COS (Figure-2)
b) Cascoded COS with dynamic matching (Figure-3)
c) Cascoded COS with improved dynamic matching (Figure-4)
d) COS Based on Gain Boosted Cascoded Mirrors (Figure-5)

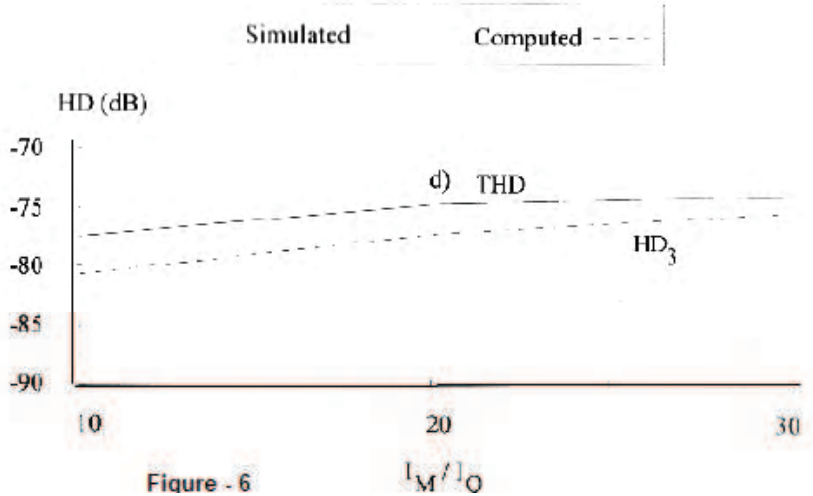


Figure - 6

Transistor aspect ratios of the circuits

Transistors	W/L (μm/μm)
MA1, MA2, MA3	600/1.4
MA4	200/1.4
MA5, MA6	60/1.4
MA7, MA8	60/3
MB1, MB2, MB3	1500/1.4
MB4	20/1.4
MB5, MB6	150/1.4
MB7, MB8	20/3

Harmonic Distortion Due to Mismatches- Threshold Voltage Mismatches

- Neglecting the channel-length modulation and any other source of non-linearity, except that caused by mismatches in V_T, second and third order harmonic distortion formulas can be obtained.

$$HD_2 = \frac{1}{8}\sqrt{\frac{\beta}{I_M}}\left(\Delta V_{TN} - \Delta V_{TP}\right)$$

$$HD_3 = \frac{1}{24}\sqrt{\beta}\left(\frac{1}{\sqrt{I_M}} - \frac{1}{\sqrt{I_Q}}\right)\left(\Delta V_{TN} + \Delta V_{TP}\right)$$

I_M => Magnitude of Sinusoidal Input Current
I_Q => Quiescent Current

$$\Delta V_{TN} = V_{TN\,A1} - V_{TN\,A2}$$

$$\Delta V_{TP} = V_{TP\,B1} - V_{TP\,B2}$$

Harmonic Distortion Due to Mismatches- Transconductance Mismatches

- A second mismatch error which gives rise to harmonic distortion is the mismatch of the transconductance gain of the mirroring transistors.
- The second-order harmonic distortion is independent of the signal amplitude and is proportional to the difference between the relative transconductance mismatches. The third-order harmonic distortion is about equal to zero.

$$\Delta\beta_N = \beta_{N\,A2} - \beta_{N\,A1}$$

$$\Delta\beta_P = \beta_{P\,B2} - \beta_{P\,B1}$$

$$HD_2 \equiv \frac{1}{8}\left(\frac{\beta_{N\,A2}}{\beta_{N\,A1}} - \frac{\beta_{P\,B2}}{\beta_{P\,B1}}\right) \cong \frac{1}{8}\left(\frac{\Delta\beta_N}{\beta_{N\,A1}} - \frac{\Delta\beta_P}{\beta_{P\,B1}}\right)$$

Design Examples

- In this section we will discuss some implementations of current amplifiers based on the output stage in Fig. 6, which proved to be the best solution for minimizing harmonic distortion due to channel-length modulation.

A VFCOA (Voltage Feedback *Current* Operational *Amplifier) - Schematic*

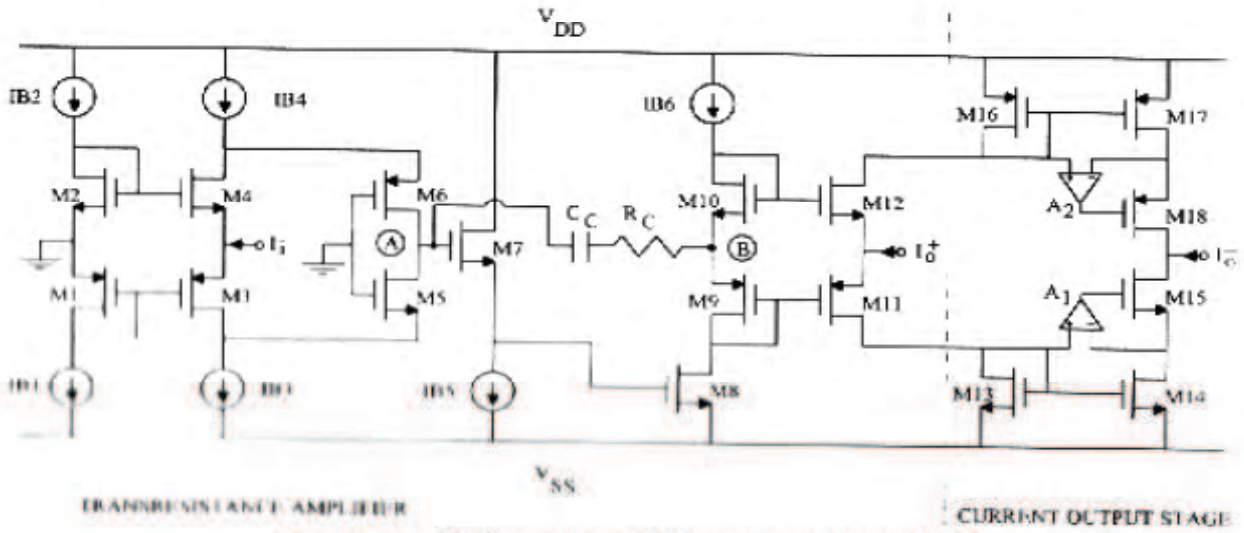


Figure - 7 *Schematic of the current amplifier*

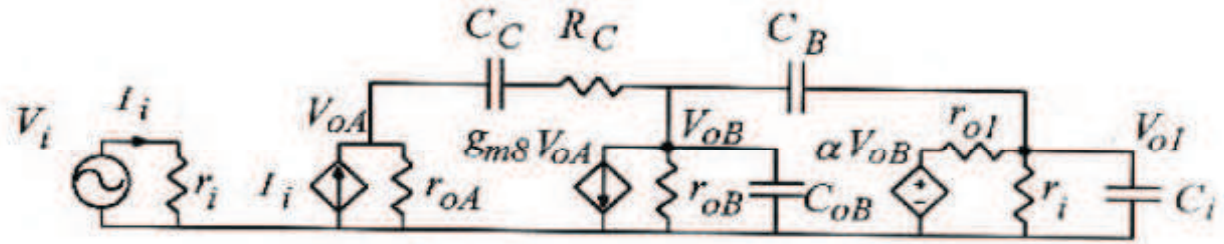


Figure - 8 *Small-signal equivalent model of the amplifier*

A VFCOA (Voltage Feedback *Current* Operational *Amplifier) - Structure*

- The transresistance amplifier is composed of transistors M1-M12 and includes, as main blocks, a folded cascode amplifier. a common source amplifier and a class AB voltage follower. The folded caseodc amplifier is made up of transistors M3-M6. The common source amplifier is made up of transistor M8 and current generator IB6. It is connected to the first stage by the common-drain M7 which provides a proper level shift. The common source amplifier drives the class AB voltage follower which is composed of transistors M9-M12. Diode-connected transistors M9 and M10 accurately set the current in M11 and M12 to a multiple of IB6.

A VFCOA (Voltage Feedback *Current* Operational *Amplifier) - Design Equations*

- DC transresistance

$$A_r(0) \cong r_{oA} g_{m8} r_{oB}$$

- Input and output resistances

$$r_i \cong \frac{1}{g_{m3} + g_{m4}} \qquad r_{o1} = \frac{1}{g_{m11} + g_{m12}}$$

- Transfer function

$$T(s) \cong \frac{A_r(0)}{r_i + r_{o1}} \frac{1}{1 + s r_{oA} C_C g_{m8} r_{oB}}$$

- Gain bandwidth product

$$f_{GBW} \cong \frac{1}{2\pi (r_i + r_{o1}) C_C}$$

A VFCOA (Voltage Feedback *Current* Operational *Amplifier) - Performance*

Transistor aspect ratios

Transistors	W/L (μm/μm)
M1, M3	160/1.4
M2, M4	80/1.4
M5	8/1.4
M6	5/1.4
M7	3/1.4
M8	90/1.4
M9	500/1.4
M10	200/1.4
M11	1000/1.4
M12	400/1.4
M13, M14, M15	600/1.4
M16, M17, M18	1500/1.4
MN1, MN2	120/2
MN3, MN4	10/4
MN5, MN6	20/2
MP1, MP2	300/2
MP3, MP4	20/4
MP5, MP6	80/2

Main amplifier performance

Parameter	Value
Open-Loop Gain	100 dB
GBW	10 MHz
Phase Margin	> 60°
Max. Output Current	±7 mA
Input Offset Voltage	≈ 5 mV
Output Offset Current	≈ 4.5 μA
Settling Time	165 ns
Slew Rate (A_I = 1)	0.2 mA/ns
THD (1 kHz, Iout = 7mA RL = 100 Ω)	< -55 dB
DC Power Dissip.	4 mW

Bias currents

Current Sources	μA
IB1, IB2,IB5	20
IB3, IB4	40
IB6	100
IN1, IN2, IP1, IP2	20
IN3, IP3	40

A COA (Current Operational Amplifier) - Schematic

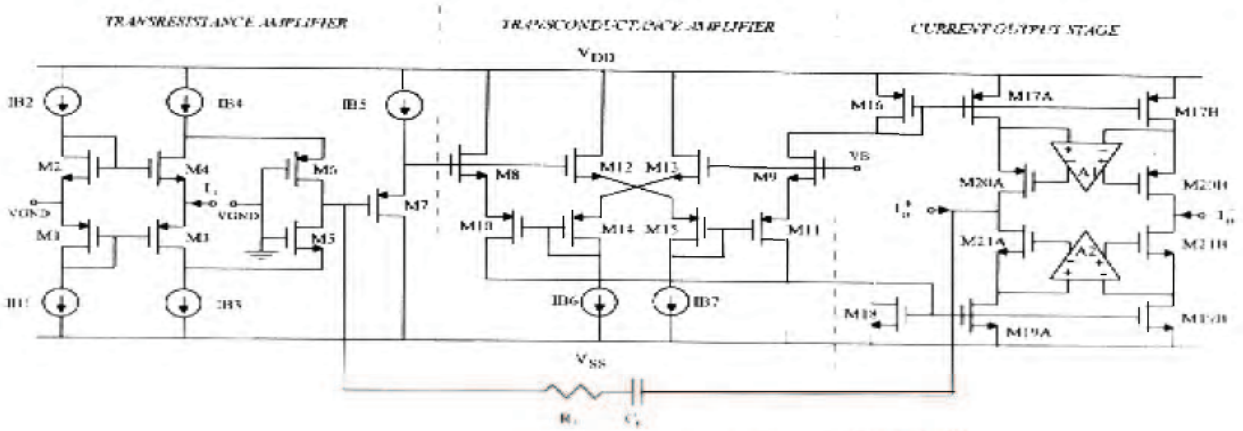


Figure - 9 *Schematic of the class AB COA*

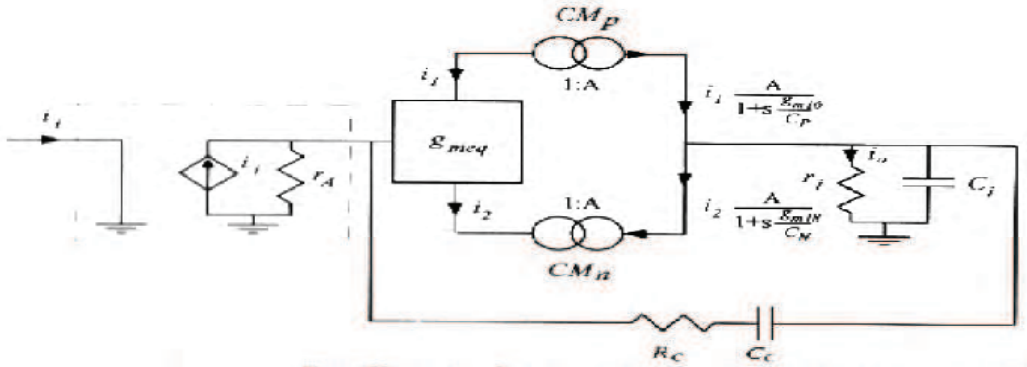


Figure - 10 *Small-signal equivalent model of the amplifier*

A COA (Current Operational Amplifier) - Structure

- The circuit contains three main blocks: a transresistance amplifier, a transconductance amplifier and a COS.
- The transresistance amplifier is made up of transistors M1-M7 and is based on a folded cascode amplifier. It makes the main contribution to the open-loop gain of the overall amplifier. In addition, common drain M7 provides the proper bias voltage to the following stage.
- The. transconductance amplifier is composed of transistors M8-M19 and works in class AB fashion. It constitutes a cross-coupled differential stage.
- Frequency compensation of the main amplifier is achieved by Miller capacitance C_C and nulling resistor R_C.
- This circuit can easily be converted to fully differential version by simply adding a replica of the input stage (here biased at VB)

A COA (Current Operational Amplifier) – Design Equations

- Transconductance gain

$$g_{meq} = \frac{i_{d8}}{v_{in}} = \frac{g_{m8} + g_{m10}}{g_{m8} g_{m10}}$$

- Total transconductance gain

$$G_T = 2 g_{meq} A_1$$

- Transfer function

$$T(s) = G_T r_A \frac{1 - \frac{C_C}{G_T}\left(1 - G_T R_C\right)s - \frac{C_C C_M}{g_{mM} G_T} s^2}{\left(1 + \frac{s}{G_T r_A r_i C_C}\right)\left(1 + \frac{C_i}{G_T} s + \frac{C_M C_i}{g_{mM} G_T} s^2\right)}$$

- Gain bandwidth product

$$f_{GBW} \cong \frac{1}{r_i C_C}$$

A COA (Current Operational Amplifier) – Performance

Transistor aspect ratios

Transistors	W/L (μm/μm)
M1, M3	160/1.4
M2, M4	80/1.4
M5, M6	8/1.4
M7	10/1.2
M8, M9, M12, M13	150/1.2
M10, M11, M14, M15	350/1.2
M16	250/1.4
M17, M20	2500/1.4
M18,	100/1.4
M19, M21	1000/1.4

Main amplifier performance

Open-Loop Gain	95 dB
GBW	8 MHz
Phase Margin	> 60°
Max. Output Current	±14 mA
Output Current Offset	< 20 μA
Settling Time (0.1%)	260 ns
Slew Rate	0.7 mA/ns
THD (1 kHz, *Iout* = 14 mA R_L = 100 Ω)	< -55 dB
DC Power Dissipation	15 mW

Bias currents

Bias Currents	μA
IB1, IB2	20
IB3, IB4	40
IB5	20
IB6, IB7	100

Use of Fully Differential COA as Current amplifier

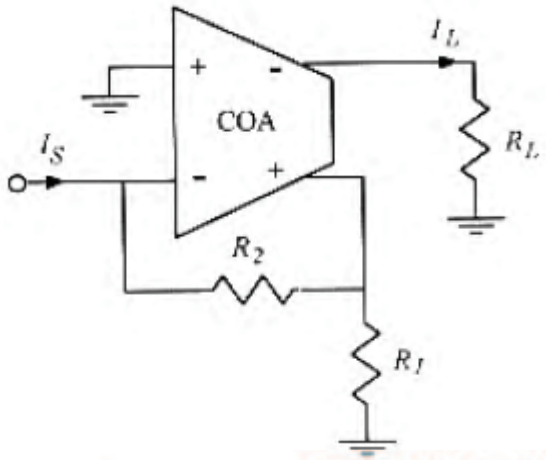


Figure - 11 *Current amplifier block diagram*

$$\frac{I_L}{I_S} = \left(1 + \frac{R_2}{R_1}\right)$$

Use of Fully Differential COA as Transconductance amplifier

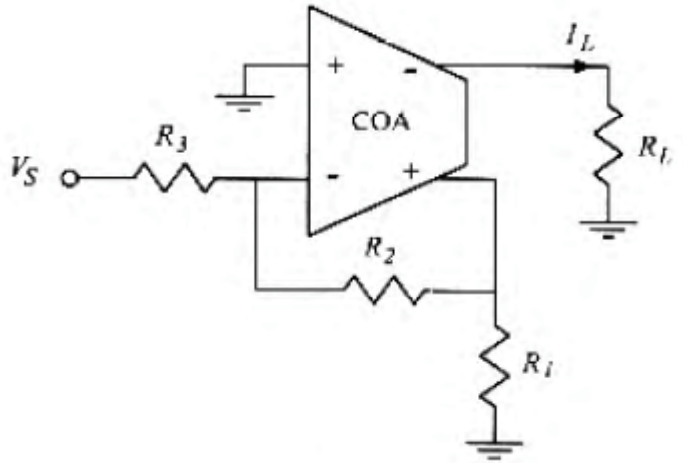


Figure - 12 *Transconductance amplifier block diagram*

$$\frac{I_L}{V_S} = \frac{1}{R_3}\left(1 + \frac{R_2}{R_1}\right)$$

Use of Fully Differential COA as Voltage amplifier

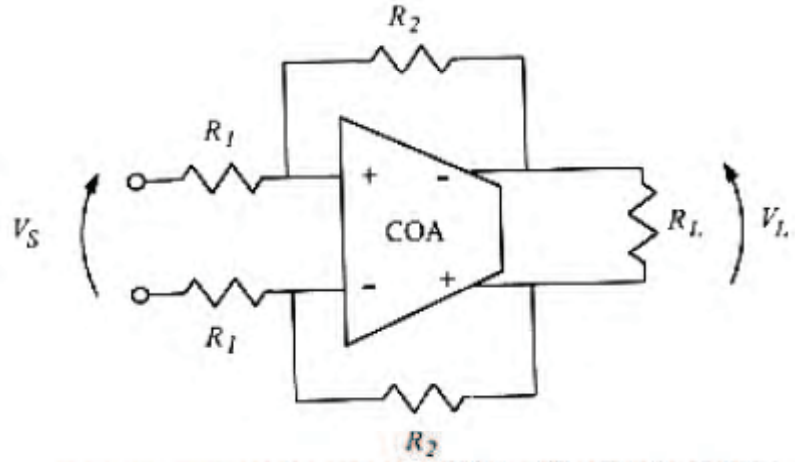


Figure - 13 *Voltage amplifier block diagram*

$$\frac{V_L}{V_S} = -\frac{R_2}{R_1}$$

Use of Fully Differential COA as Transresistance amplifier

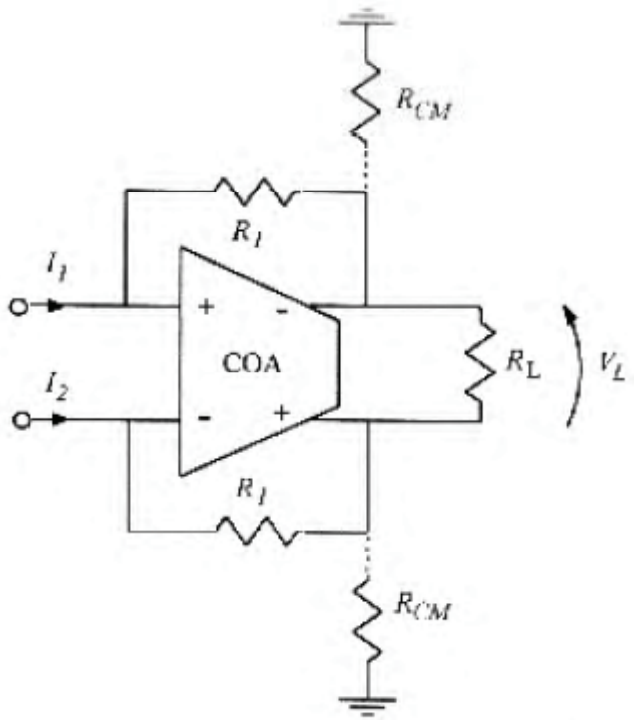


Figure - 14 *Transresistance amplifier block diagram*

$$\frac{V_L}{(I_1 \quad I_2)} = R_1$$

References

- G. Palmisano, G. Palumbo, S. Pennisi, CMOS current amplifiers, Kluwer Academic Publishers, 1999

Thank you