A New CMOS Electronically Tunable Current Conveyor and Its Application to Current-Mode Filters

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Summary

- Introduction
- Proposed CMOS high-performance electronically tunable second-generation current conveyor (ECCII)
- Application of a current-mode CC based filter with proposed ECCII
- Simulation results of the application

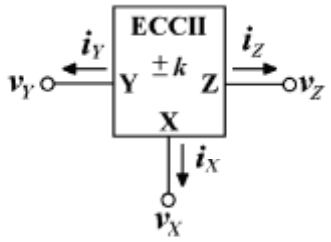
Introduction

- In the article, a new CMOS high-performance electronically tunable second-generation current conveyor (ECCII), and application of a second order current filter realization with ECCII is given with SPICE simulation results.
- Although there are other methods like OTAs or DCCC realizations for tunning , with the proposed ECCII there will be no suffer from limited output voltage swing like the OTAs or complicated structure and oversize area consumption like DCCC's that uses CDNs

Proposed CMOS ECCII Structure

- Proposed ECCII's equtaion matrix is given as below

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm k & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}.$$

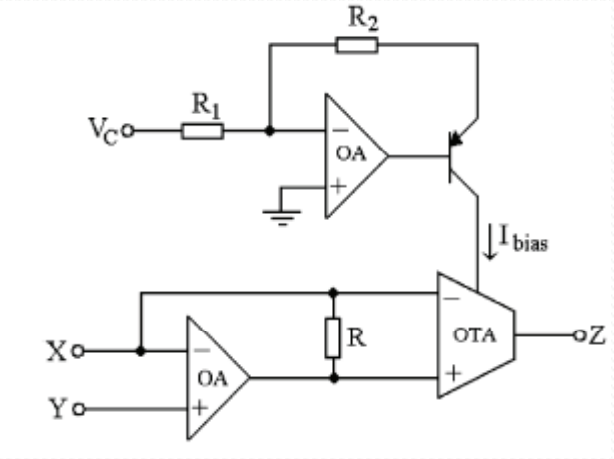


electrical symbol of ECCII

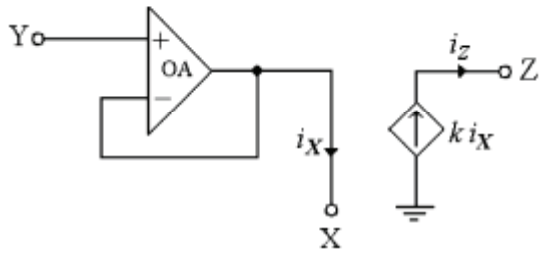
- According to equation between X and Y terminals there is a unity voltage gain and a tuneable ±k current gain between terminals X and Z.
- Y and Z terminals shows a high impedance level, and the X terminal have low impedance

Proposed CMOS ECCII Structure

- ± sign of k gives us the type of ECCII if it is positive or negative type of ECCII.
- Representations of ECCIIs can be simply shown as



or



Proposed CMOS ECCII Structure

(CA implementation used in proposed CMOS ECCII)

- Tunable small signal current amplifer

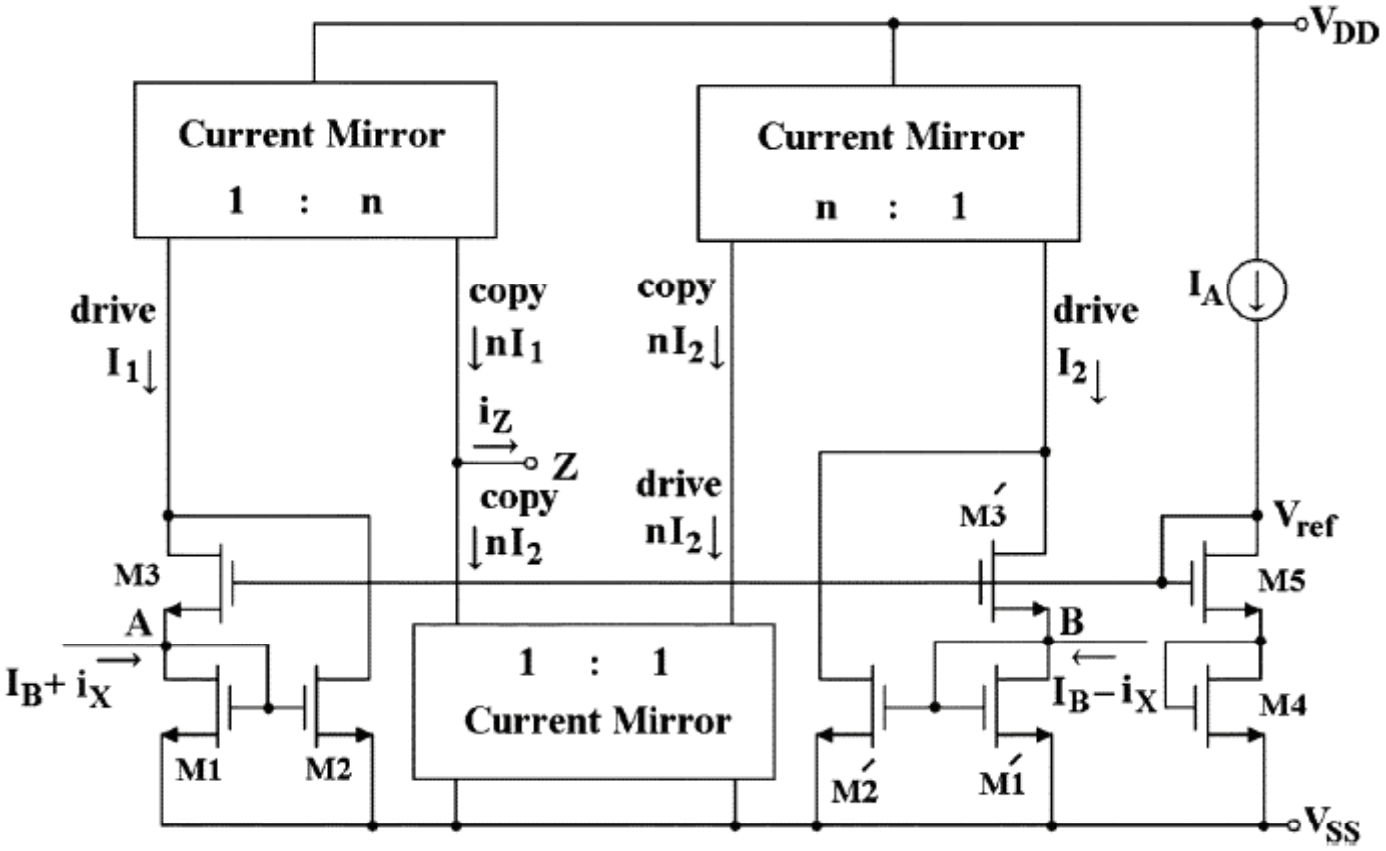


Fig. 1. Small signal amplifier

Proposed CMOS ECCII Structure

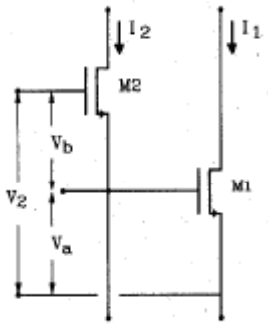
(CA implementation used in proposed CMOS ECCII)

- M1,M2,M3 and M1',M2',M3' transistors group form a current squaring circuit with A and B input ports.
- Diode connected transistors M4, and M5, and the current source I_A, form a current-controlled bias circuit, which supplies the bias voltage V_{REF} to M3 and M3'.
- Assumed that all the transistors in the circuit are characterised by the square-law model of an MOS transistor operating in the saturation region.

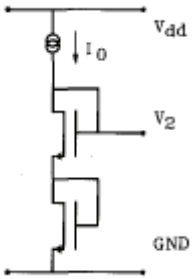
Proposed CMOS ECCII Structure

(CA implementation used in proposed CMOS ECCII)

- Simply from these equations I1 and I2 can be found.[3]



$$I_1 = K(V_a - V_t)^2$$
$$I_2 = K(V_b - V_t)^2$$
$$V_b = V_2 - V_a.$$
$$I_1 - I_2 = K(V_2 - 2V_t)(V_a - V_b).$$
$$I_1 + I_2 = \frac{1}{2}K(V_2 - 2V_t)^2 + \frac{(I_1 - I_2)^2}{2K(V_2 - 2V_t)^2}.$$



$$I_0 = \frac{1}{4}K(V_2 - 2V_t)^2$$
$$I_{out} = 2I_0 + \frac{I_{in}^2}{8I_0}.$$

Fig. 2. Equations forming the I1 and I2 [3]

Proposed CMOS ECCII Structure

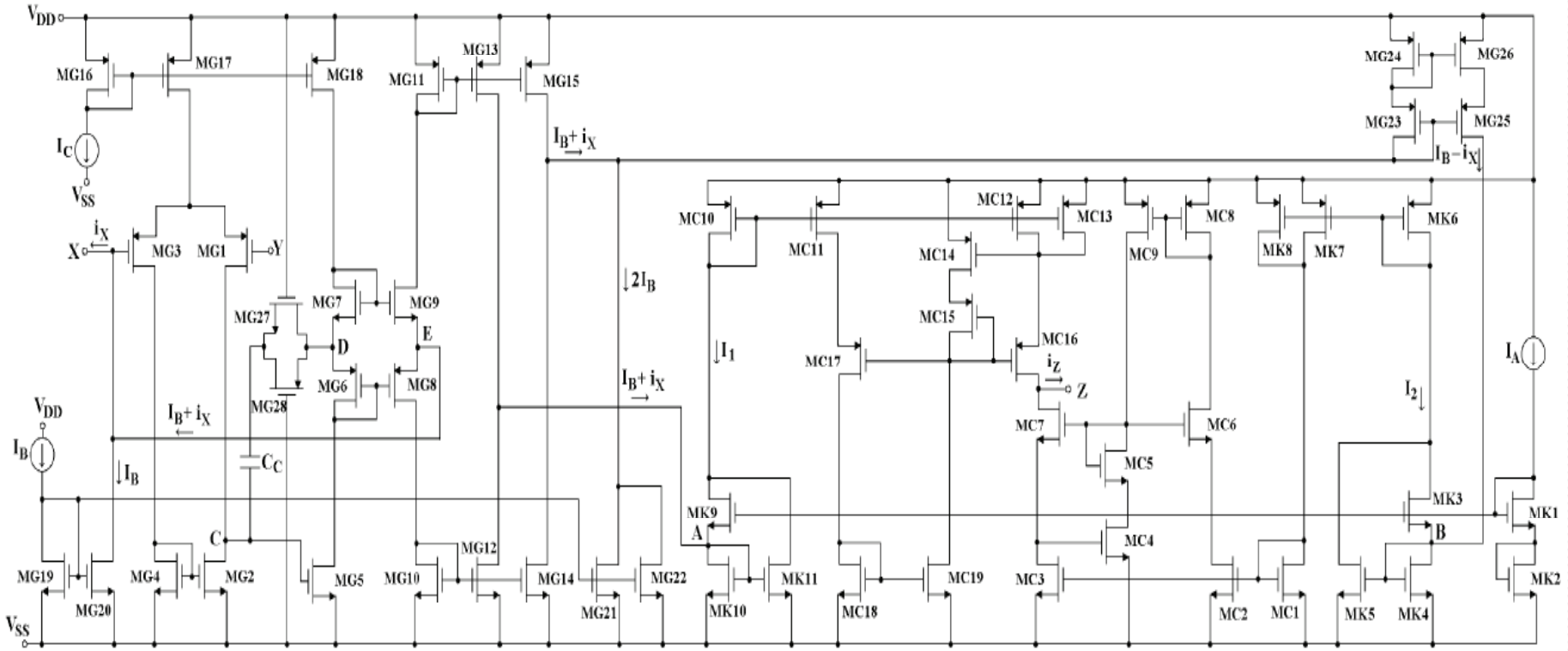
(CA implementation used in proposed CMOS ECCII)

- I1 and I2 given as $I1=2I_A+(I_B+i_X)^2/8I_A$ and
- $I2=2I_A+(I_B-i_X)^2/8I_A$
- As long asKeeping $|I_B|+|i_X| \leq 4I_A$ at currents I1 and I2 are multiplied n times by the upper current mirrors in fig.1, so the output current of the circuit i_z equals nI1-nI2 which is $n(I_B/2I_A)\, i_X = ki_X$
- Where $k=n(I_B/2I_A)$ is the controlled small signal gain by the dc bias currents of the I_B and I_A .f
- Dynamic range of the gain k can be increased because the maximum value of k limited by $k \leq 2n$.

Proposed CMOS ECCII Structure (OA part)

- Using the CA described before proposed ECCII implementation is given as fig.3.
- First part of the circuit is a high perpormance two stage OA with output buffer.
- First stage of the OA is a differential amplifier consist of MG1-MG4 with voltage gain of $A_{v1}=-g_{MG1}(r_{oMG1} \,||\, r_{oMG2})$ where g_{MG1} and r_{oMG1} , r_{oMG2} are the small signal transconductance gain and output resistances

Proposed CMOS ECCII Structure



- Fig.3. Proposed ECCII+

Proposed CMOS ECCII Structure (OA part)

- Second stage of the OA is MG5 source amplifier transistor buffered by MG6-MG9 transistors which is a Class-AB output stage.
- Gain of this second stage A_{V_2} is given as

$$A_{v2} = -g_{m_{\mathrm{MG5}}} \times \left(\left(\frac{r_{o_{\mathrm{MG5}}} + r_{o_{\mathrm{MG6}}} + g_{m_{\mathrm{MG6}}} r_{o_{\mathrm{MG5}}} r_{o_{\mathrm{MG6}}}}{1 + g_{m_{\mathrm{MG6}}} r_{o_{\mathrm{MG6}}}} \right) \Bigg\| \left(\frac{r_{o_{\mathrm{MG7}}} + r_{o_{\mathrm{MG18}}} + g_{m_{\mathrm{MG7}}} r_{o_{\mathrm{MG7}}} r_{o_{\mathrm{MG18}}}}{1 + g_{m_{\mathrm{MG7}}} r_{o_{\mathrm{MG7}}}} \right) \right)$$

$$\cong -g_{m_{\mathrm{MG5}}} \left(r_{o_{\mathrm{MG5}}} \| r_{o_{\mathrm{MG18}}} \right).$$

Proposed CMOS ECCII Structure (OA part)

- Then overall gain of the OA can be calculated as $A_V=A_{V1}xA_{V2}$. Assuming that Class-AB output stage has a unity gain.
- Using Miller compensation in the OA between C and D, C_C capacitance and transistors MG27,MG28. Node A can follow I_B+i_X current entering the X node even at high frequencies.
- f_d can given as

$$f_d = \frac{1}{2\pi\left(r_{o_{MG1}} \| r_{o_{MG2}}\right)\left(C_{nC} + (1+|A_{v2}|)C_C\right)} \cong \frac{1}{2\pi\left(r_{o_{MG1}} \| r_{o_{MG2}}\right)|A_{v2}|C_C}$$

Proposed CMOS ECCII Structure (OA part)

- Where C_{nC} is the parasitic capacitance between C node and the ground, it is given by

$$C_{nC} \cong C_{gd\mathrm{MG1}} + C_{db\mathrm{MG1}} + C_{gd\mathrm{MG2}} + C_{db\mathrm{MG2}} + C_{gs\mathrm{MG5}}$$

- C_{gdMG5} is ignored because it is too small compared to the C_{nC}.
- Gain-bandwidth of the OA is $\mathrm{GBW} = A_v \cdot f_d \cong \frac{g_{m_{\mathrm{MG1}}}}{2\pi C_C}$
- Transistors MG27 and MG28 are used to locate a zero at $s_0 = \frac{1}{C_C\left(\frac{1}{g_{m_{\mathrm{MG5}}}} - R\right)}$

Proposed CMOS ECCII Structure (OA part)

- where R is resistance produced by the MG27 and MG28. If R selected greater than 1/ g_{mMG5} phase margin can be improved.
- Negative feedback going from the MG5 ensures the unity gain of the VX/VY function and feedback at X node provides the low impedance terminal.Which is

$$R_x \cong \frac{\left(\frac{1}{g_{m_{\mathrm{MG8}}}} \left\| \frac{1}{g_{m_{\mathrm{MG9}}}}\right.\right) \times \left(\frac{1}{g_{m_{\mathrm{MG1}}} g_{m_{\mathrm{MG5}}}}\right)}{\left(\left(\frac{r_{o_{\mathrm{MG5}}} + r_{o_{\mathrm{MG6}}} + g_{m_{\mathrm{MG6}}} r_{o_{\mathrm{MG5}}} r_{o_{\mathrm{MG6}}}}{1 + g_{m_{\mathrm{MG6}}} r_{o_{\mathrm{MG6}}}}\right) \left\| \left(\frac{r_{o_{\mathrm{MG7}}} + r_{o_{\mathrm{MG18}}} + g_{m_{\mathrm{MG7}}} r_{o_{\mathrm{MG7}}} r_{o_{\mathrm{MG18}}}}{1 + g_{m_{\mathrm{MG7}}} r_{o_{\mathrm{MG7}}}}\right)\right.\right) \times \left(r_{o_{\mathrm{MG1}}} \| r_{o_{\mathrm{MG2}}}\right)}$$

Proposed CMOS ECCII Structure (OA part)

- And the impedance at node Y is $$|Z_Y| \approx \frac{1}{\eta W_{MG1} L_{MG1} C_{ox} \omega}$$
- Where η is a constant parameter, W channel witdh and L is channel length of the MG1 transistor C_{OX} is the gate oxide capacitance and ω is the operation frequency.
- And using current mirrors MG11,MG13,MG14; MG10,MG12,MG15; MG19,MG21,MG22 and MG23,MG24,MG25,MG26 I_B+i_X and I_B-i_X currents transferred to the A and B nodes of the small signal current amplifier.

Proposed CMOS ECCII Structure (CA part)

- The second part of the proposed ECCII+ circuit is the small signal current amplifier of Fig.1 constructed with high-performance current mirrors known as IAFCCMs in its output stage.
- IAFCCMs used because the output conductance and the feedback capacitance are 100 times lower than the standard current mirror circuit .
- The output resistance at terminal Z of the proposed ECCII+ is $$R_{oz} = [g_{m_{MC7}} g_{m_{MC4}} r_{o_{MC3}} r_{o_{MC7}} (r_{o_{MC4}} \| r_{o_{MC9}})] \| [g_{m_{MC16}} g_{m_{MC14}} r_{o_{MC16}} \times (r_{o_{MC12}} \| r_{o_{MC13}})(r_{o_{MC14}} \| r_{o_{MC19}})] .$$

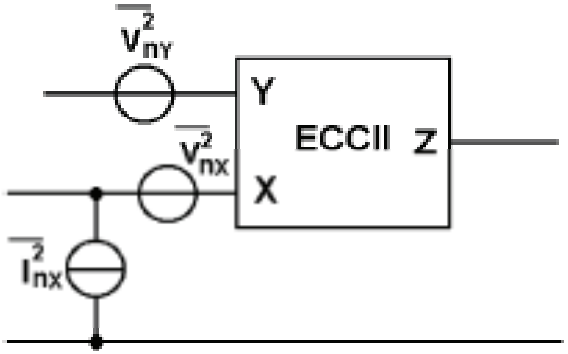
Proposed CMOS ECCII Structure (CA part)

- From Fig.3, it can be seen that the value of parameter n=2 because transistors MC12,MC13and MK7,MK8 are used in parallel. So this circiuts maximum current gain is k_{MAX}=4.
- Also type of our positive ECC can be changed to negative ECC by applying currents I_B+i_X and I_B-i_X into terminals B and A of the small signal current amplifier.

Proposed CMOS ECCII Structure (Noise performance)

- Noise can be modeled by three sources V^2_{nY}, V^2_{nX} and I^2_{nX} .Because of the high gain of the input stage other input-referred noise contribtions became unsignificant so V^2_{nY}, V^2_{nX} and I^2_{nX} power-spectral densities can be given as below.(γ ,noise factor of transistor channel length and bias)

$$\overline{V_{nY}^2} \approx 4kT\gamma\left(g_{m_{MG1}} + g_{m_{MG2}}\right)\cdot\frac{1}{g_{m_{MG1}}^2}$$
$$= 4kT\gamma\left(\frac{1}{g_{m_{MG1}}} + \frac{g_{m_{MG2}}}{g_{m_{MG1}}^2}\right)$$
$$\overline{I_{nX}^2} \approx 4kT\gamma g_{m_{MG20}}$$
$$\overline{V_{nX}^2} \approx 4kT\gamma\left(g_{m_{MG3}} + g_{m_{MG4}}\right)\cdot\frac{1}{g_{m_{MG3}}^2}$$
$$= 4kT\gamma\left(\frac{1}{g_{m_{MG3}}} + \frac{g_{m_{MG4}}}{g_{m_{MG3}}^2}\right)$$



A Filter application of The ECCII

- There many voltage and current-mode CC based filters available in the literature but most of them lack of electronic tunability. Tunability can be obtained by using a CCCII instead of ECCII but it used as a tool for adjusting the resonant frequency or quality factor of the filter circuits, but not the gain. To control gain ECCII provides better solution.

A Filter application of The ECCII

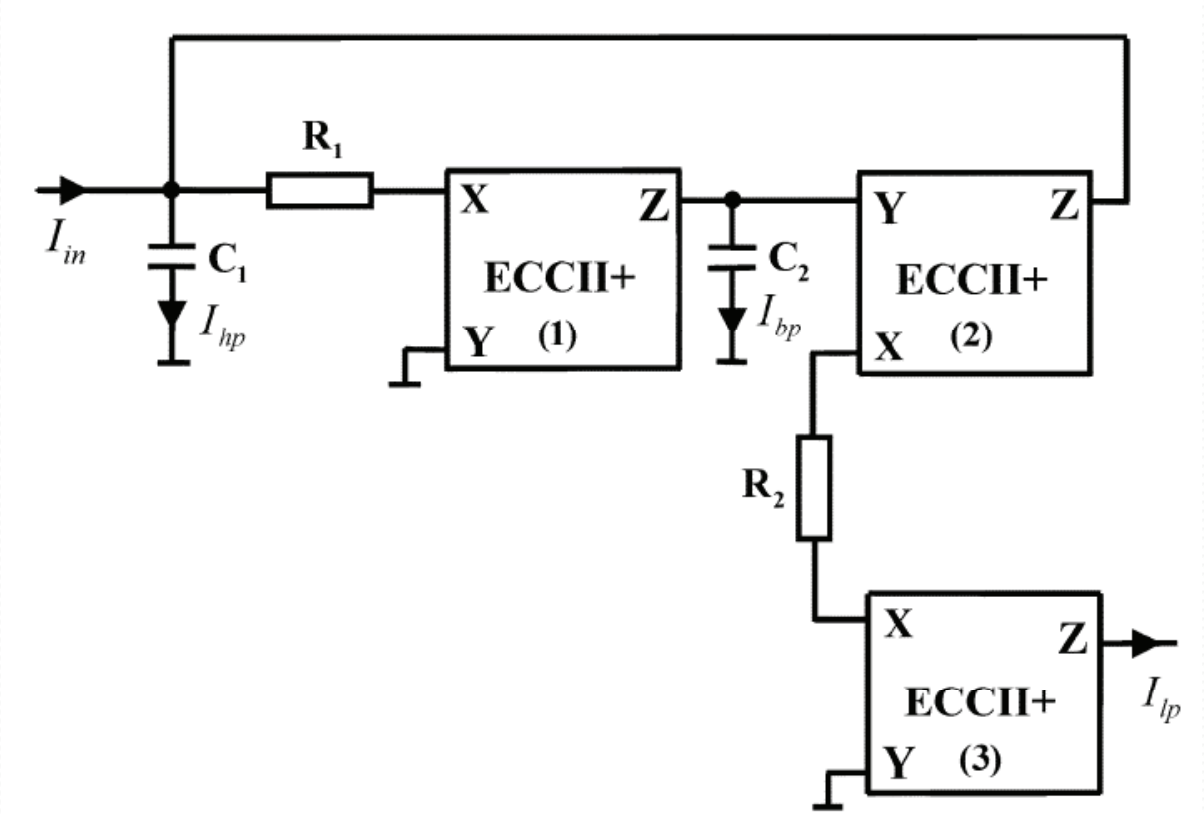


Fig. 4. An universal current-mode filter using ECCII+s.

A Filter application of The ECCII

- Analysing the circiut in fig.4 the low-pass, high-pass, and bandpass transfer functions can be given as

$$\frac{I_{\mathrm{lp}}}{I_{\mathrm{in}}} = \frac{\frac{k_1 k_3}{C_1 C_2 R_1 R_2}}{s^2 + \frac{1}{C_1 R_1} s + \frac{k_1 k_2}{C_1 C_2 R_1 R_2}}$$

$$\frac{I_{\mathrm{hp}}}{I_{\mathrm{in}}} = \frac{s^2}{s^2 + \frac{1}{C_1 R_1} s + \frac{k_1 k_2}{C_1 C_2 R_1 R_2}}$$

$$\frac{I_{\mathrm{bp}}}{I_{\mathrm{in}}} = \frac{-\frac{k_1}{C_1 R_1} s}{s^2 + \frac{1}{C_1 R_1} s + \frac{k_1 k_2}{C_1 C_2 R_1 R_2}}$$

- Where ki is current gain of ith ECCII.The gains of the filter is G1p=(k3/k2),Ghp=1,Gbp=-k1 respectively.

A Filter application of The ECCII

- Extra ECCIIs can be used to obtain tunable gains.
- ωo and Q values given as

$$\omega_o = \sqrt{\frac{k_1 k_2}{C_1 C_2 R_1 R_2}} \quad Q = \sqrt{\frac{k_1 k_2 C_1 R_1}{C_2 R_2}}.$$

- It can be seen that low pass gain can tuned by k3 without changing ωo or Q ,also k2 and k1 used to change the ωo and Q parameters.

A Filter application of The ECCII

- Also the filters ωo and Q sensivities given as;

$$S_{k_3}^{G_{\mathrm{lp}}} = -S_{k_2}^{G_{\mathrm{lp}}} = S_{k_1}^{G_{\mathrm{bp}}} = 1$$

$$S_{k_1}^{G_{\mathrm{lp}}} = S_{k_1}^{G_{\mathrm{hp}}} = S_{k_2}^{G_{\mathrm{hp}}} = S_{k_3}^{G_{\mathrm{hp}}} = S_{k_2}^{G_{\mathrm{bp}}} = S_{k_3}^{G_{\mathrm{bp}}} = 0$$

$$S_{k_1}^{\omega_o} = S_{k_2}^{\omega_o} = S_{k_1}^{Q} = S_{k_2}^{Q} = \frac{1}{2}$$

$$S_{k_3}^{\omega_o} = S_{k_3}^{Q} = 0$$

- Which are not more than 1 in magnitude.

Simulation Results

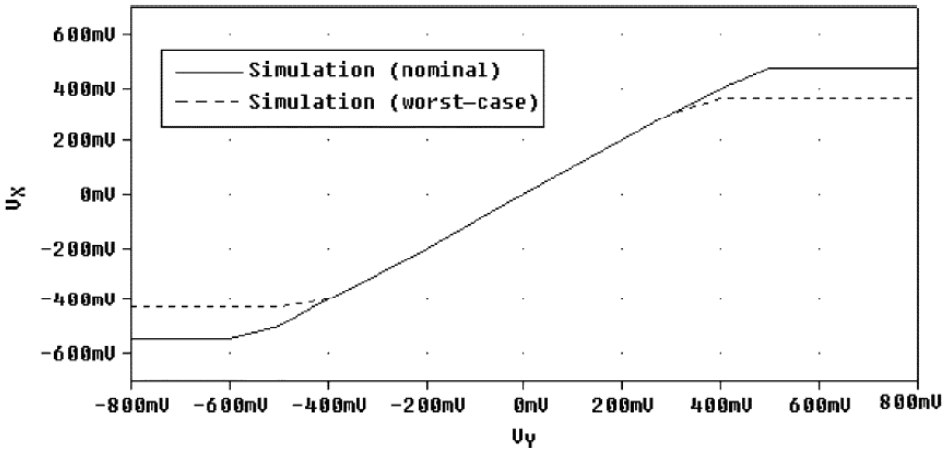
- The performance of the proposed ECCII is verified using the SPICE simulation program. The MOS transistors are simulated using TSMC 0.35-µm CMOS process model parameters V_{THN}=0.54 V, V_{THP}=-0.71 V, μ_N=436 cm²/V-s, μ_P=212 cm²/V-s, T_{OX}=7.9 nm and dimensions as in table below

Transistor	W/L (µm)
MG1, MG3	47.25/0.7
MG2, MG4	8.75/0.7
MG6, MG8	70/1.4
MG5, MG7, MG9-MG28 MC1-MC19, MK6-MK8	28/1.4
MK1-MK5, MK9-MK11	35/0.7

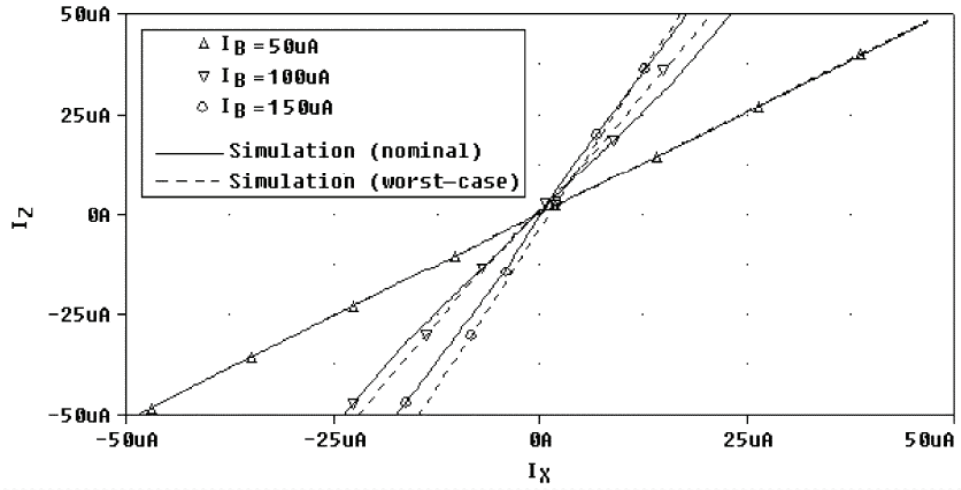
Simulation Results

- Using the selected values
- Vsupply=±1.5V
- $I_A=I_B=50\ \mu A$
- $I_C=100\ \mu A$
- $C_C=4.3pF$
- Two simulation configurations performed. Voltage follower input voltage on Y, output on X with an infinite load at X. And current follower input current on X, output current on Z with Z grounded.

Simulation Results

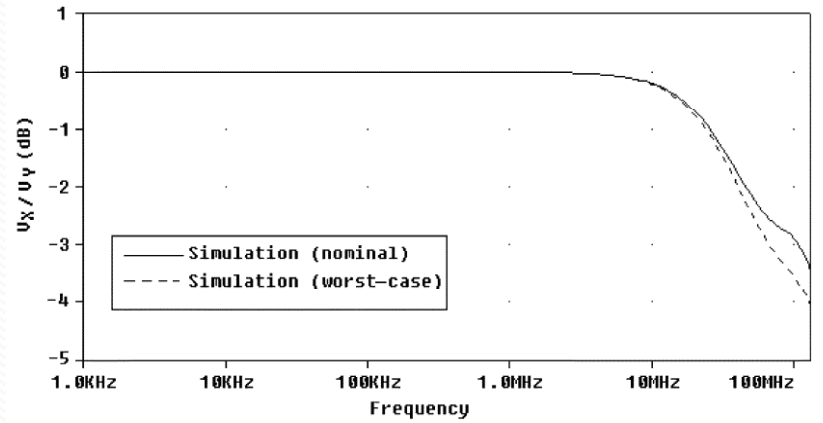


V_x-V_y dc transfer characteristic of the proposed ECCII+

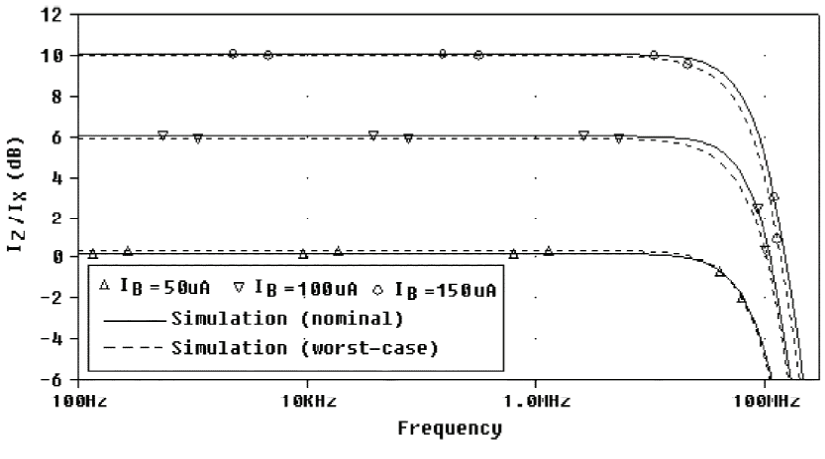


I_z-I_x dc characteristic of the proposed ECCII+ for different values of I_B .

Simulation Results



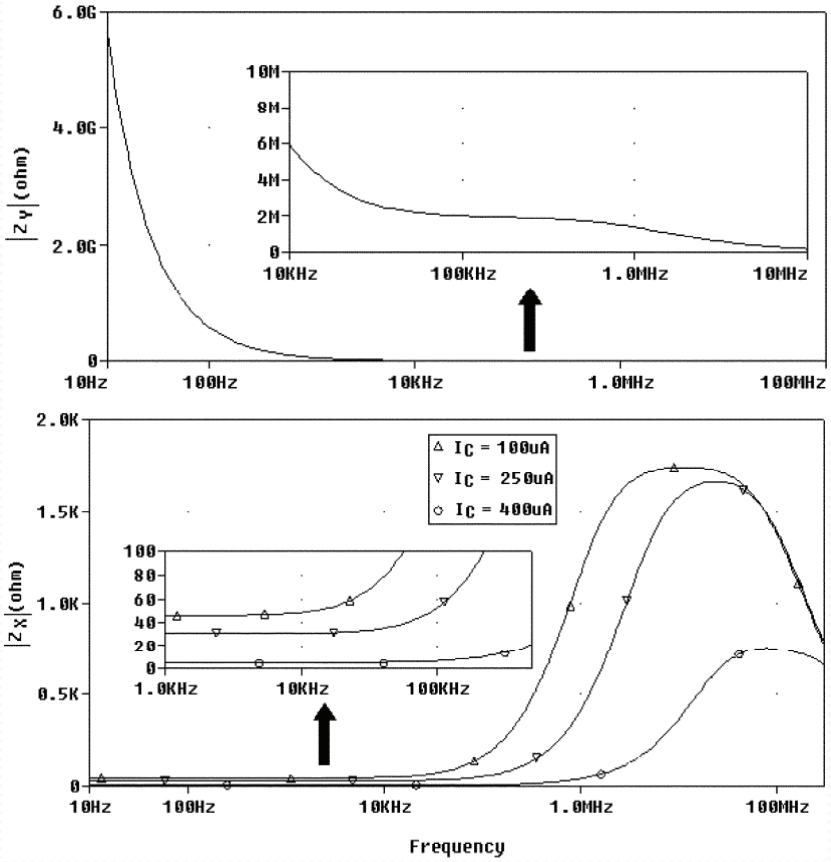
Frequency response of the voltage follower V_X/V_Y.



Frequency response of the current follower I_Z/I_X.

Cut off frequencies are 107 and 77 MHz, respectively.

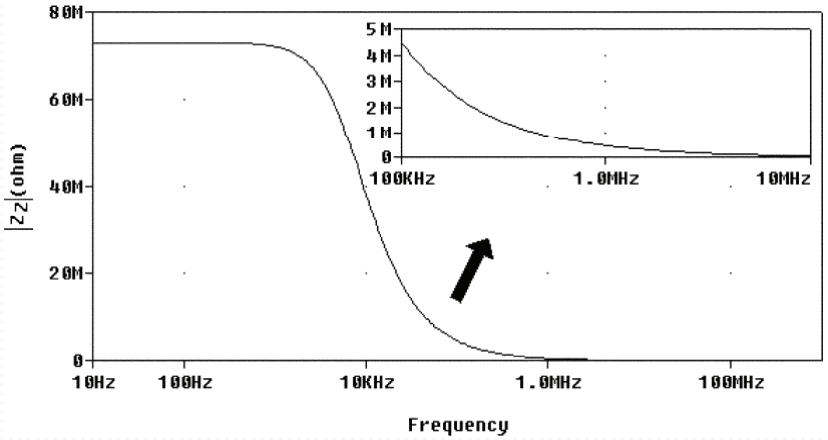
Simulation Results



The frequency response of the impedance at terminal Y.

Frequency response of the impedance at terminal X for different values of biasing current I_C .

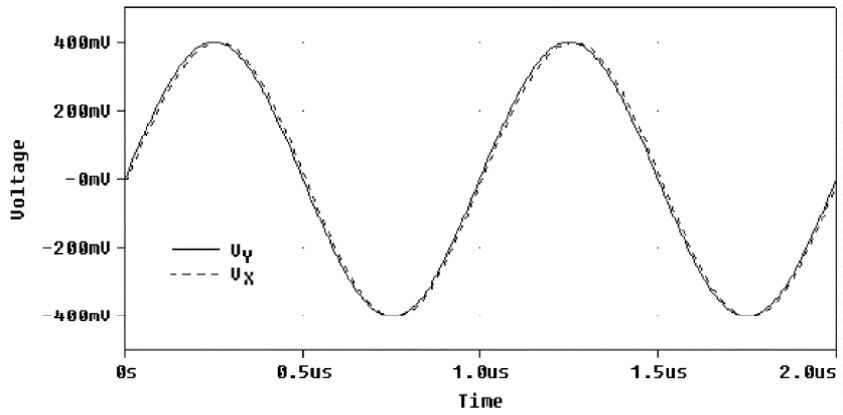
Simulation Results



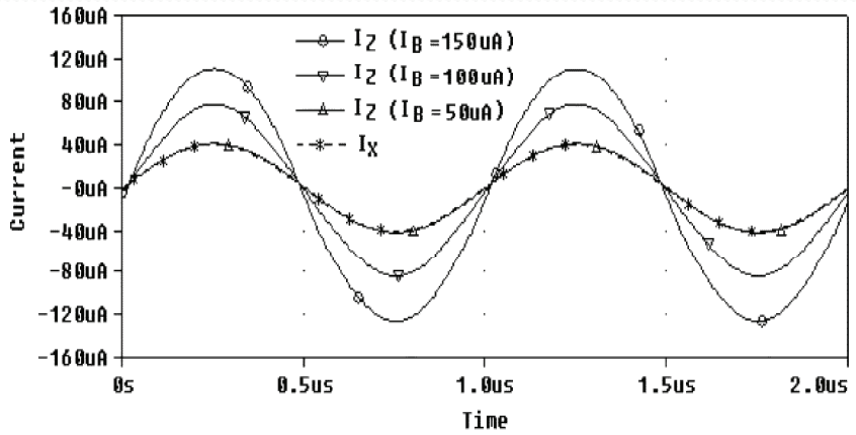
Frequency response of the impedance at terminal Z.

- The terminal Z has very high impedance because of using IAFCCM in the output stage of the ECCII.
- Impedance values of 73 MΩ , 38.2 M Ω , and 448 k Ω are found for the terminal Z at frequencies of 10 Hz, 10 kHz, and 1 MHz, respectively.

Simulation Results

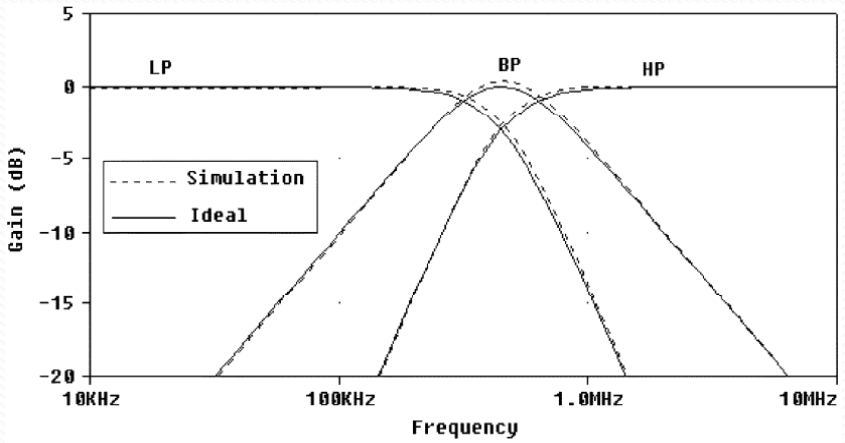


Response of the voltage follower to a sinusoidal signal at 1 MHz.

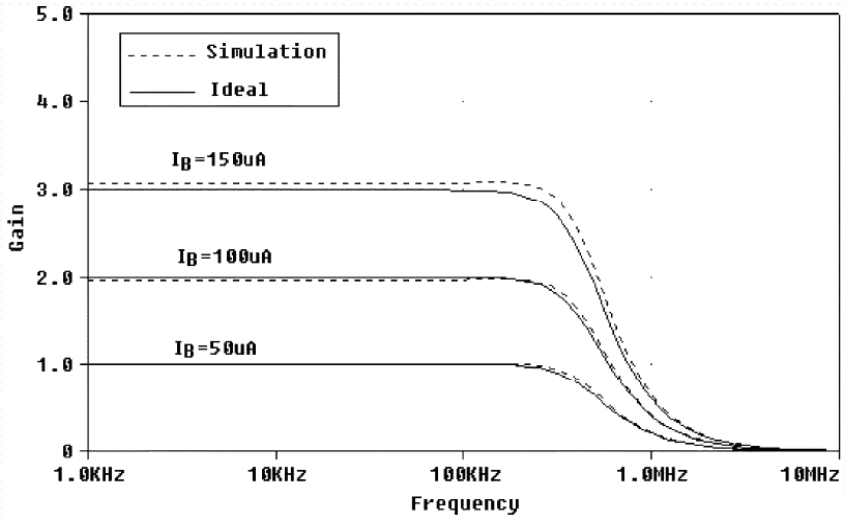


Response of the current follower to a sinusoidal signal at 1 MHz for different values of I_B .

Simulation Results



Frequency responses of the second-order current-mode filter. (f_o=450kHz,Q=0.707)



Tuning of the gain of the low-pass response.

Simulation Results

- The model of the ECCII taking parasitics into account is shown in Fig. 5.

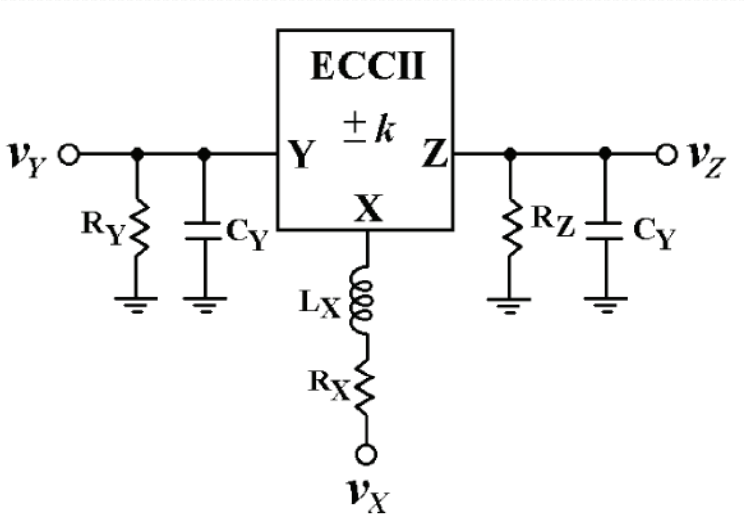


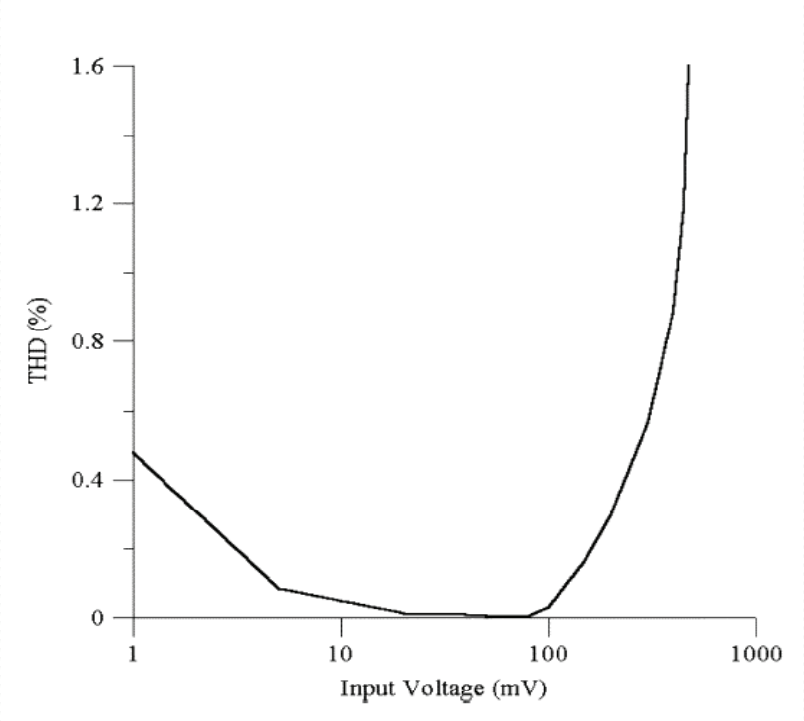
Fig. 5. Model of the ECCII including parasitic elements.

Simulation Results

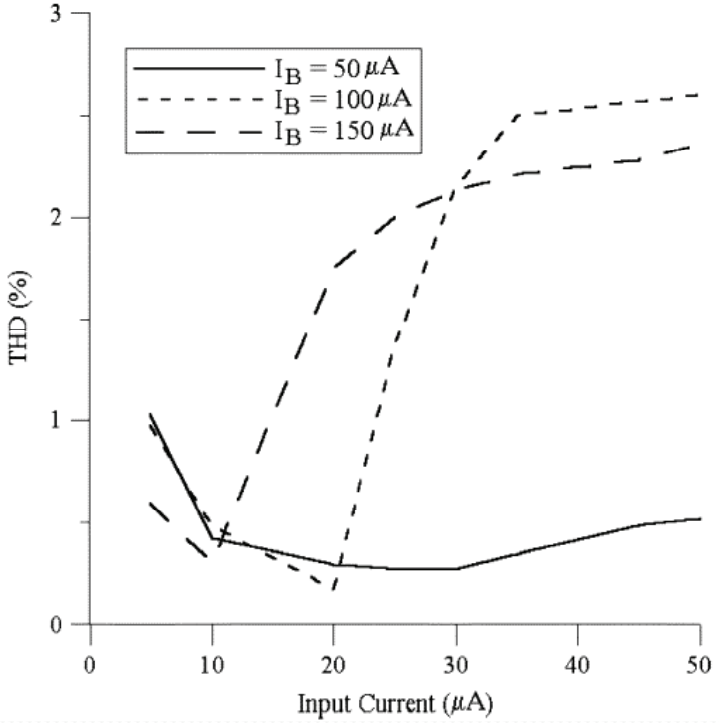
- The large-signal behavior of the circuit is tested by investigating the total harmonic distortion (THD) for sinusoidal input signals at 1 MHz. The THD graps given for voltage follower and current follower configurations for the parasitic values at terminals X, Y, and Z of the proposed ECCII are given in table below

Parasitic	Value		
R_X, L_X	46Ω, 240µH @ I_C=100µA	31Ω, 67µH @ I_C=250µA	4.7Ω, 6.6µH @ I_C=400µA
R_Y, C_Y	∞, 2.7pF		
R_Z, C_Z	73MΩ, 0.35pF		

Simulation Results



THD of the voltage follower.



THD of the current follower for different values of I_B .

Conclusion

- A new ECCII, whose current-transfer ratio can be varied by electronic means, is proposed in this paper.
- Which has very high output impedance, which makes it suitable for cascading.
- Also implementation of a second-order current-mode universal filter with the proposed ECCII is given which realizes BP,HP,LP responces.
- Simulations shows a very good performance of the ECCII in terms of output resistance, linearity, frequency response, noise, and tunability.

References

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