ELE509E
Current-Mode Analog Circuit Design
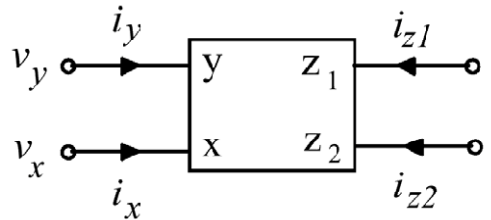### Homework 3 (16.11.2009)

Figure 1. Circuit symbol of DOCCII.

A dual output current conveyor (DOCCII) is described by

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ k & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_X \\ V_Y \\ V_{Z1} \\ V_{Z2} \end{bmatrix}$$

$k = \pm 1$. For $k = 1$ a DOCCII with two noninverting Z outputs is obtained. For $k = -1$ the Z_2 terminal yields an inverted output signal.

Design a CMOS dual output current conveyor with inverting and noninverting outputs.
1. Terminal input and output resistances R_{Z1}, R_{Z2}, $R_Y > 10$ M.Ohms, $R_X < 10$ Ohms.
2. Voltage tracking error $\varepsilon_V < 0.1\%$, current tracking error $\varepsilon_I < 0.1\%$,
3. BW of the voltage gain ($A_V = v_x/v_y$) $f_{V3db} > 10$ MHz,
4. BW of the current gain ($AI1 = i_{z1}/i_x$, $A_u = i_z2/i_x$) $f_{I3db} > 50$ MHz,

Choose an adequate CMOS realization technology. The model parameters of the MOS transistors can be obtained from the WEB site.

    a- Specify the CMOS DOCCII structure, determine transistor dimensions. Using SPICE simulation results
    b- draw the the plots of V_X against V_Y, I_{Z1} and I_{Z2} against I_X,
    c- specify the limits of the operation region,
    d- draw the frequency response of the voltage gain and determine the bandwidth,
    e- draw the frequency response of the current gain and determine the bandwidth,
    f- draw the plot of the terminal impedances against the frequency,
    g- investigate the large signal behaviour of the DOCCII by applying to Y terminal a sinusoidal input voltage in the passband and observing the total harmonic distortion THD at the X, Z_1 and Z_2 terminals for different input levels; draw the plot of THD against ii_n for each terminal. (Connect adequate load resistances to the X, Z_1 and Z_2 terminals.
    h- Give a detailed evaluation of your results.