Extracting your circuit:

After creating your DRC clean layout, you should extract the layout into a netlist and run post layout simulations with your extracted netlist.

1) Save your layout. If you don't change the directory, it will probably be saved in your Home directory.

You can browse to your home directory in a clean intall easily. If you are using Windows Subsystem, browse to:

C:\Users***your_windows_username***\AppData\Local\Packages

Locate the Canonical Group Ubunutu package (exact name of the package may change depending on the version you have installed)

Under the Ubunutu folder you will browse to

\LocalState\rootfs\home***your_linux_username***

The complete path should look like the following

C:\Users***your_windows_username***\AppData\Local\Packages\CanonicalGroupLimited.Ubuntu18.04onWindows_79rhkp1fndgsc\LocalState\rootfs\home***your_linux_username***

2) Type
   :extract
   The command window will tell you extraction is completed. A new file with ".ext" will be generated.
   This file is not a SPICE competible netlist. You should create a SPICE competible netlist from this .ext file.
3) Before creating a SPICE competible netlist, you should set the parasitic extraction threshold for MAGIC. If you just try to create a SPICE netlist, it iwll ignore any capacitance less than 1fF. Therefore, we will set the parasitic threshold to 0.
   Type
   :ext2spice cthresh 0
4) Create the spice compatible netlist
   Type
   :ext2spice
   Command window will tell you extraction to SPICE is completed.
5) Go to the location you saved the layout and go through the .spice file. It should contain all the transistors you created and parasitic capacitances between your nodes.
6) Now you can proceed with simulations as described in video tutorials.