LVAICD FINAL PROJECT

RAIL TO RAIL OPAMP DESIGN

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1. Introduction

In this project, a rail to rail CMOS operational amplifier is designed. Two constant Gm-rail to rail input stages were designed in the previous project and a rail to rail output stage is designed in this project. Square root circuit is chosen as the input stage of the OPAMP. OPAMP is designed in Cadence Spectre simulator with UMC 018 process technology and BSIMv3 parameters are used in simulations.

2. Class AB Output Stage

Monticelli [1] Class AB output stage is chosen as the output stage of the OPAMP as shown in Figure 1. It is widely used in low voltage designs. Minimum current of the output transistors is not zero so they do not go into cutoff region. According to direction of the current i, some current is pushed to output or pulled from the output. Minimum supply voltage requirement of this structure is $2V_T+3V_{DS(SAT)}$.

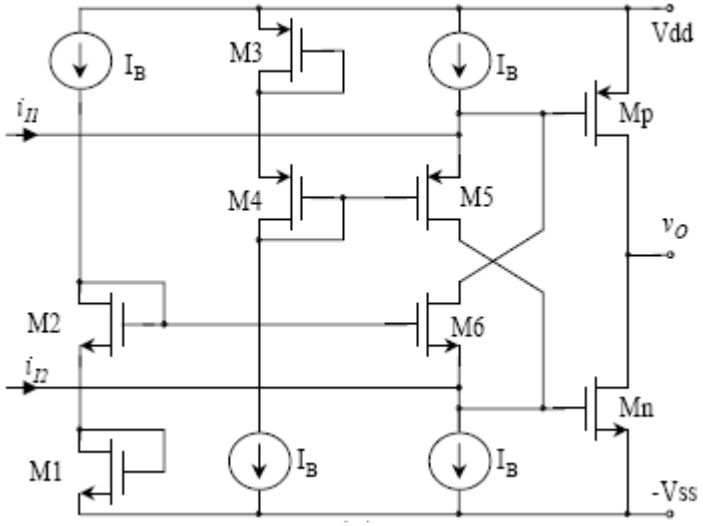

Figure 1: Class AB output stage

Analysis of this structure is given in [2]. It is obvious that if the aspect ratios of M2 and M4 are chosen twice as M6 and M5 respectively. In that case, in the quiescent situation, V_{GS} of M2 and M6 and of M4 and M5 is equal, hence, V_{GS} of Mn and Mp is equal to M1 and M3. The aspect ratios of M_n and M_p can be made n times larger with respect to M1 and M3, then the quiescent current in output transistors becomes nIb.

In Figure 2, connection of the input stage to the output stage is shown. Connection is realized over cascode current mirrors. Drains of the NMOS and PMOS differential inputs M1-M4, which were connected to the ground and V_{DD} when the input stage was designed, are connected to low voltage cascode current mirrors [3].

In Figure 3, complete circuit except the input stage G_m control circuit is given. The transistors M11-M12 and M7-M8 realize two bias current sources of the output stage and they also provide signal injection to the output stage. For this reason, their output resistance is expected high. A large gain is obtained if the output resistance of the cascode current mirror is high. Moreover, output transistors with high g_m values and high output resistances provide larger gain.

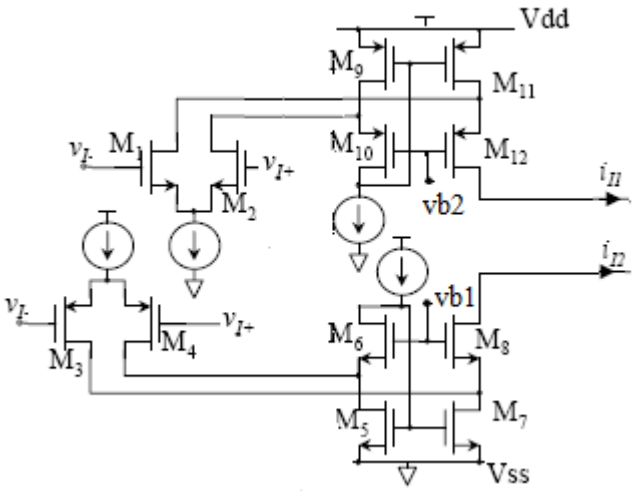

Figure 2: Connection of the input stage to output stage

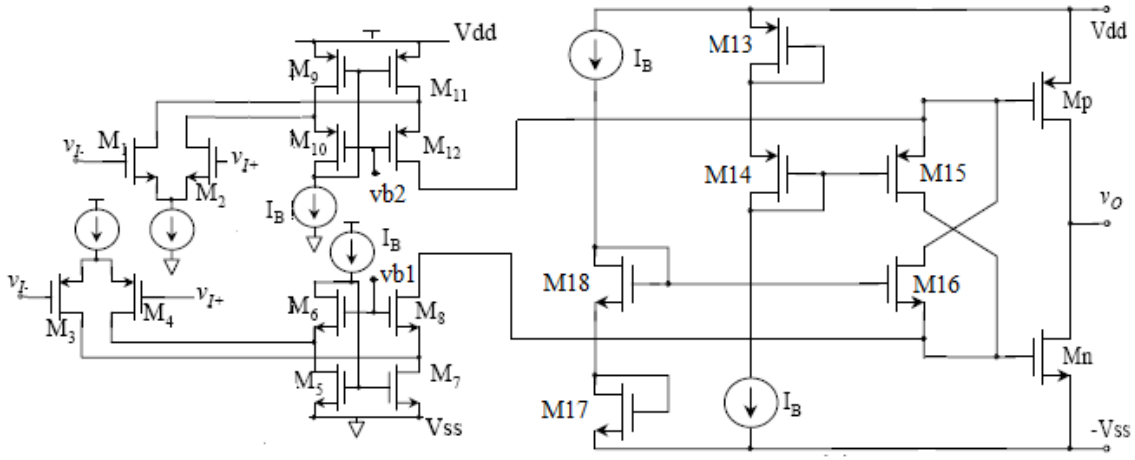

Figure 3: Complete circuit except input stage constant G_m control circuit

3. Design of the Circuit

Maximum tail current of the input stage was 80µA. For this reason, I_B current must be equal or higher than the tail current in order not to make output current zero [2]. I_B is also chosen 80µA to keep power consumption low.

Channel lengths of the devices are not chosen minimum due to channel length modulation effects and matching problems. High gain can be obtained if channel length is chosen large, but there is a trade of between gain and speed. For this reason, channel length is chosen 0.5µm which provides gain above 90dB.

Dimensions of the cascode current mirrors are chosen such that they are away from triode region. $V_{DS(sat)}$ is chosen 100mV for this design.

As it was mentioned before, M18 and M14 are chosen twice of M16 and M15. Aspect ratios M_n and M_p are chosen n times of M17 and M13.

GBW product of the circuit can be given as G_m/C_c where C_c is the compensation capacitor and G_m is the transconductance of the input stage. Since it is nearly constant, GBW product is expected nearly constant for whole input common mode range.
First dominant pole comes from the gate of the output transistors; cascode current mirrors and compensation capacitor C_c decreases this pole.
Second pole comes from the output node which has the value $g_{m,n,p}/(C_{tot})$ where C_{tot} is the total equivalent capacitance at the output.
If C_c is reduced, dominant pole increases and GBW also increases. However, dominant and second pole approach each other. Thus, phase margin decreases. For this reason, second pole must be pushed away to increase phase margin. This can be done by increasing g_m values of the output transistors. This may be done by increasing n value, but this increases power consumption. Second method is increasing widths of the output transistors. However, second method increases parasitic capacitance values at the output this may decrease phase margin after some point.
For symmetry g_{mn} and g_{mp} are chosen equal so that there will be relationship between PMOS and NMOS transistors at the output. This also provides doing parametric sweep easily. Since current of the output transistors are equal, the ratio between the aspect ratios of these transistors will be μ_n/μ_p which is about 3.5 for UMC 018 process.
After choosing the arbitrary value of C_c, W_n or W_p values are swept in a limited range. Phase margin and GBW are plotted. If the obtained values are not enough, C_c value is changed and sweeping is repeated. If specs are not provided, then n value is increased keeping power consumption within acceptable limits and the same steps are repeated. Thus, the circuit is optimized.
With only C compensation, from the simulations it is seen that for n=1, GBW=23MHz for n=2 it is 30MHz and for n=3, GBW is about 36MHz. Increasing n also increases GBW, but it increases power consumption. Choosing n=3 gives good result. Worst case PM becomes 71º.

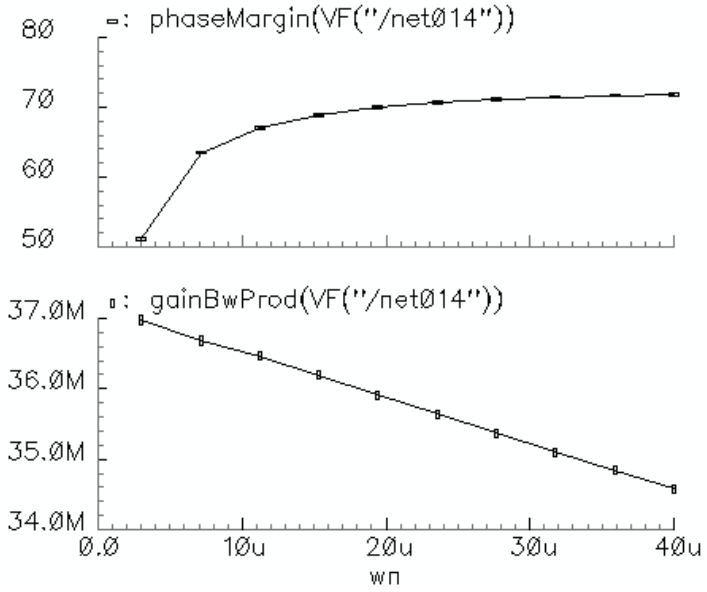

Figure 4: Wn vs GBW-PM for C_c=500fF

If C_c is increased PM increases but GBW decreases and if C_c is decreased, PM decreases but GBW increases. Taking all of these into consideration, choosing Wn=21µm where C_c=500fF is suitable. It gives 70.5º PM. Change of PM and GBW with Wn is given in Figure 4. Vb=1V, Vp=1.8V is chosen.
Aspect ratios of the other transistors are given in Table 1.

Table 1: Device dimensions

Transistor	Dimension (W/L)	Transistor	(W/L)
M5-M7	40µ/0.5µ	M18	12µ/0.5µ
M6-M8	20µ/0.5µ	Mn	21µ/0.5µ
M9-M11	60µ/0.5µ	Mp	73.5µ/0.5µ
M10-M12	30µ/0.5µ		
M13	24.5/0.5µ		
M14	64µ/0.5µ		
M15	32µ/0.5µ		
M16	6µ/0.5µ		
M17	7µ/0.5µ		

4. Simulation Setup and Results

If the designed OPAMP is used in open loop, output of the OPAMP can go to V_{DD} or gnd due to offset voltage at the input. Output node must be biased at the middle point. For this reason, offset voltage must be applied to the input. One of the known methods to obtain the offset voltage is use of the replica of the OPAMP in unity gain feedback. One of the inputs of the OPAMP in test is taken from the OPAMP in unity gain feedback so that OPAMP can operate in open loop. Test setup is shown in Figure 5. VCVS prevents loading effect of the OPAMP1.

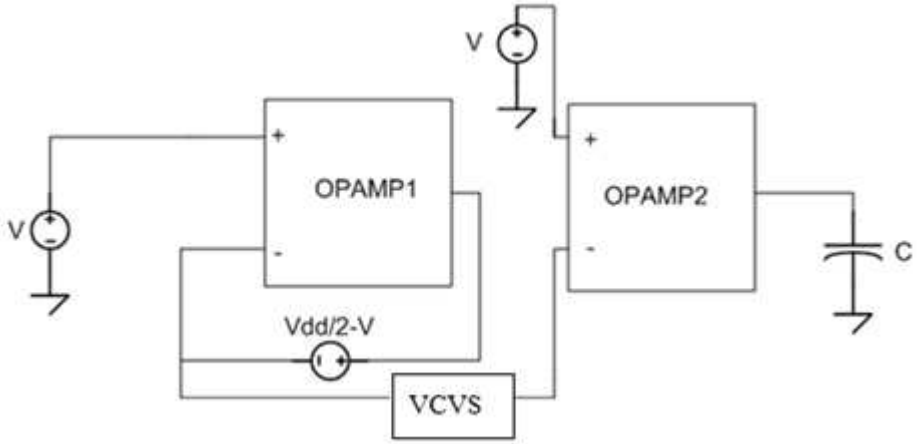

Figure 5: Test setup for open loop OPAMP simulation

Offset voltage is measured between the two inputs of OPAMP2 when the output is at Vdd/2. It is found 60µV.

Change of open loop gain of OPAMP and GBW are shown in Figure 6 and Figure 7. It is seen that open loop gain changes only 1.53dB and GBW changes 2.37MHz for whole input common mode range.

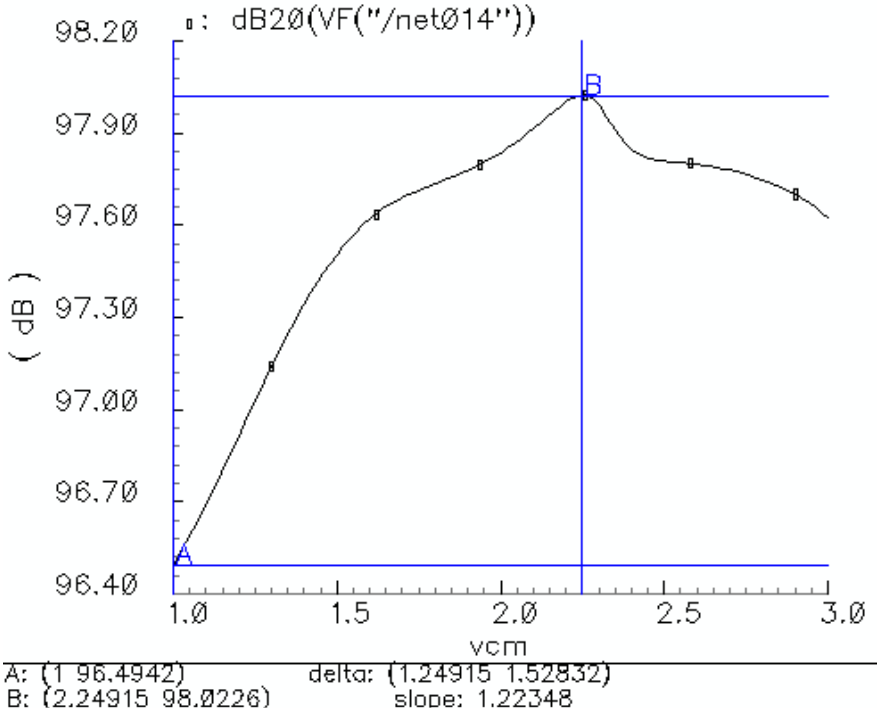

Figure 6: Change of DC open loop gain with common mode input voltage

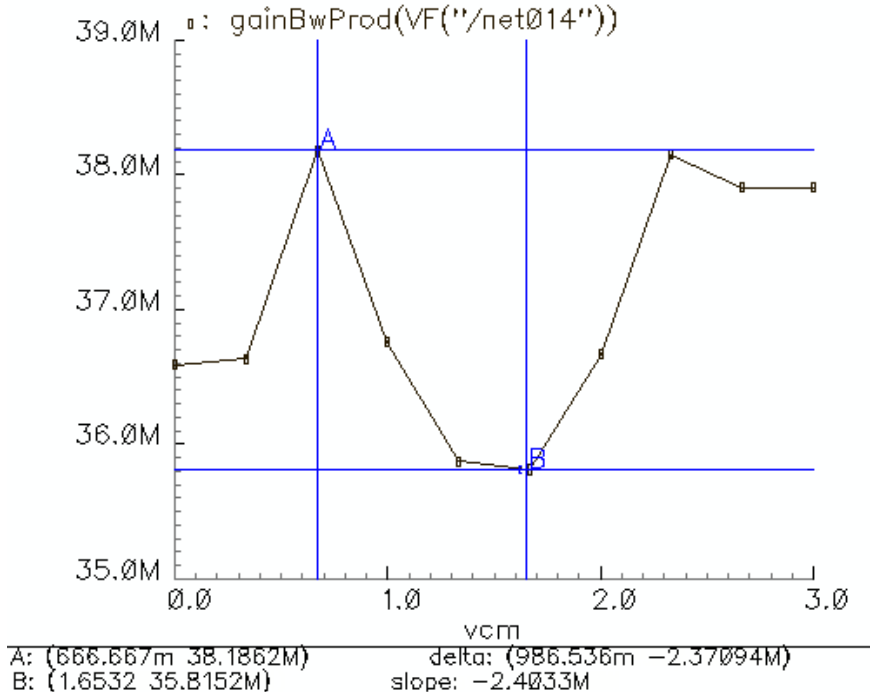

Figure 7: Change of GBW with input common mode voltage

In Figure 8, change of PM with input V_{CM} is shown. It changes from 75.7º to 70.3º. In Figure 8, change of output voltage when a 1kHz sin wave is applied to OPAMP in buffer configuration is given. It is seen that OPAMP operates rail to rail.

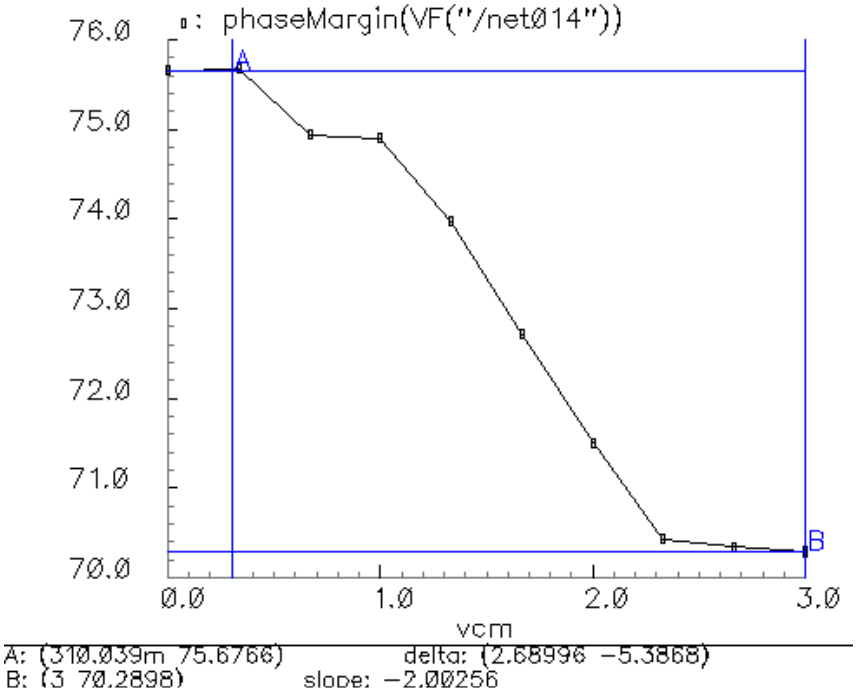

Figure 8: Change of PM with input common mode voltage

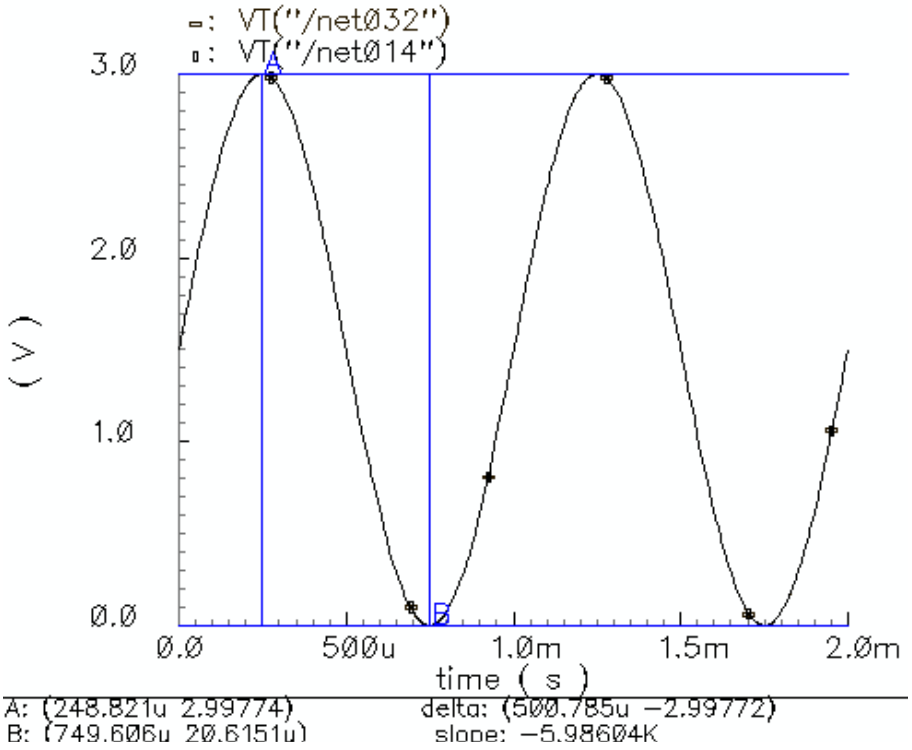

Figure 9: Input and output voltage when a rail to rail sin wave is applied

1MHz square wave with 40ps rise and fall times is applied to OPAMP in buffer configuration. It is seen that OPAMP operates rail to rail and SR is measured. Rising and falling SRs are SR_{rise}=70V/us, SR_{fall}=65V/us. Figure 10 shows change of output voltage for this case.

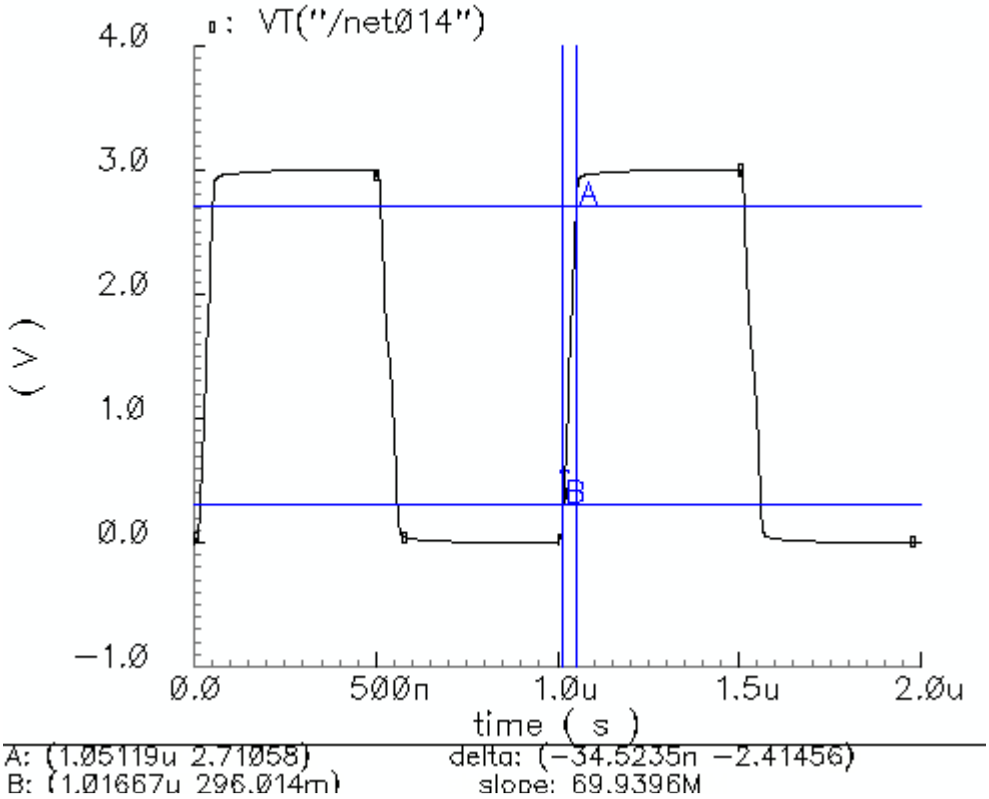

Figure 10: Change of output voltage when 1MHz square wave is applied to buffer

Compensation capacitor creates a right half plane zero, it can be shifted to the left half plane with a series resistance to compensation capacitor. It must be larger than $2/g_{mn,p}$.By using parametric sweep its value can be found. In this circuit R=6kΩ resistance is used. This increases PM of the OPAMP. PM becomes about 100º. Since this value is too high and OPAMP speed is low, it is possible to decrease PM and increase GBW of the OPAMP by decreasing C_c. C_c is decreased to 220fF for which worst case PM becomes 71º which is above the specs.

Change of GBW after RC compensation is shown in Figure 11. It is seen that GBW nearly doubles. Change of PM also for this case is given in Figure 12.

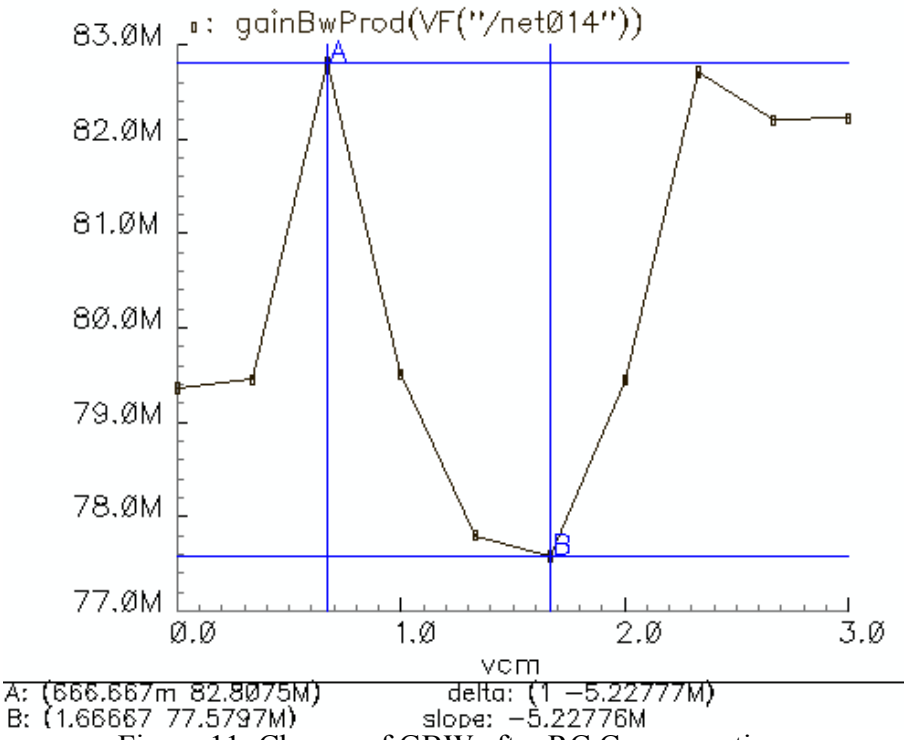

Figure 11: Change of GBW after RC Compensation

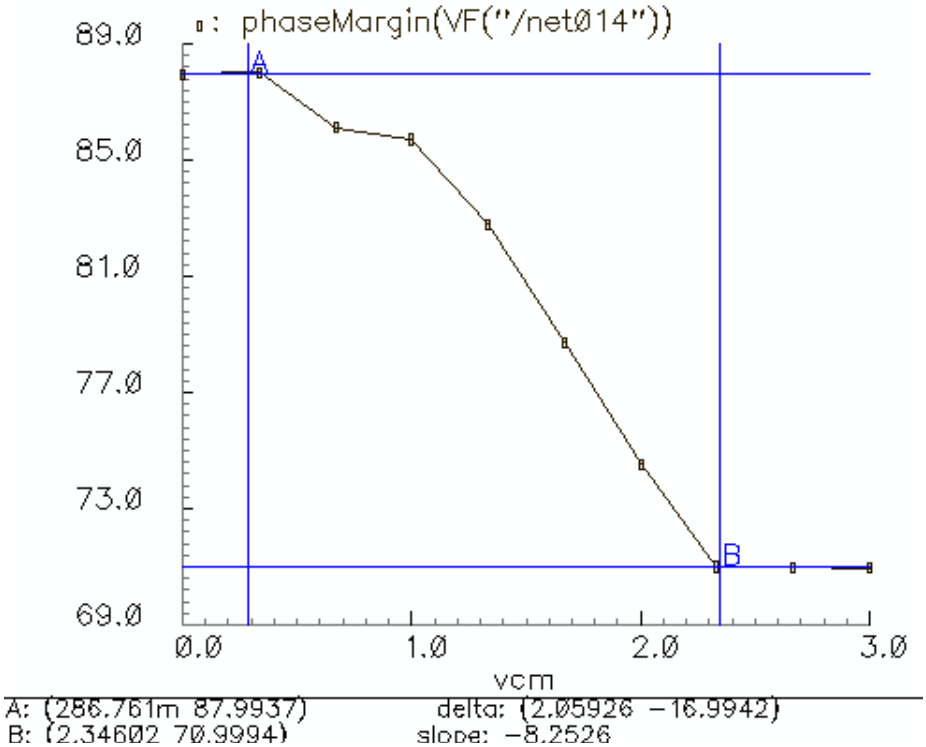

Figure 12: Change of PM after RC Compensation

1MHz square wave is applied again to buffer and change of output voltage after RC compensation is shown in Figure 13. SRs are measured again, they are SR-rise=140µV/s SR-fall=130V/µs. It is seen that they also double.

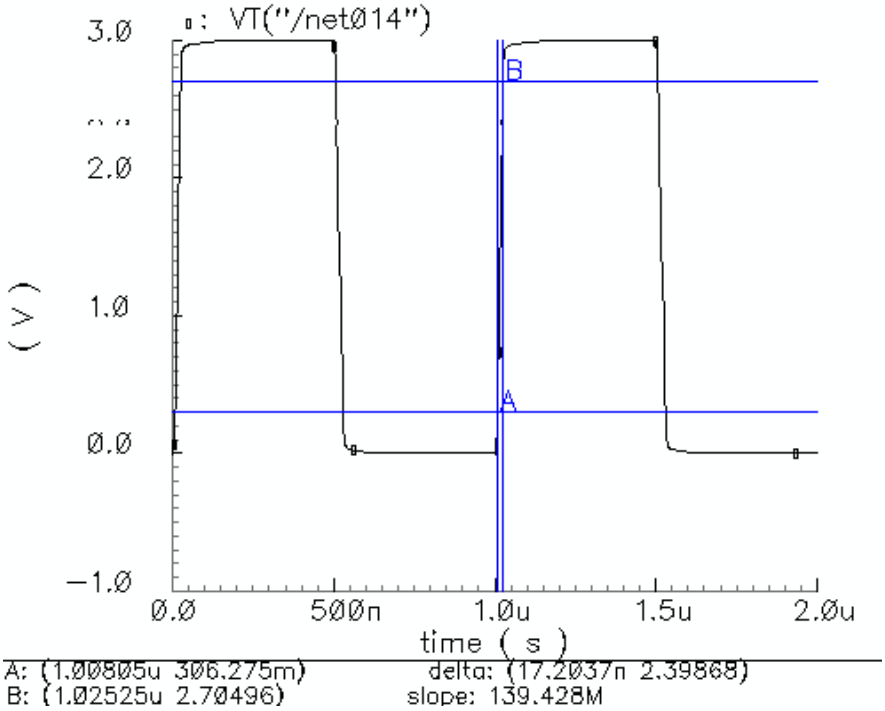

Figure 13: Change of output voltage when a 1MHz square wave is applied to buffer after RC compensation

Minimum power supply can be assumed as 2.5V. For which Gain, PM and GBW change less than 10%. Change of gain, PM and GBW for 2.5V DC supply are shown in Figure 14.

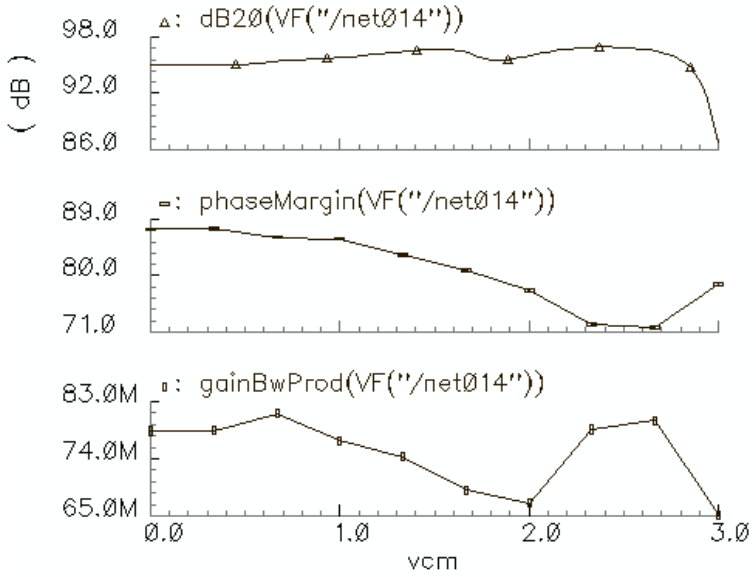

Figure 14: Change of performance parameters for 2.5V DC supply

After connecting resistor to the output of the buffer, sine wave is applied to system. Resistors have different values 1k, 5k, 10k and 15k are connected with parallel to C_L and maximum and minimum output voltages are measured as

For 1K Vmax=2.86V-Vmin=140mV
For 5K Vmax=2.97V-Vmin=30mV
For 10k Vmax=2.985V-Vmin=15mV
For 15k, Vmax=2.99V-Vmin=10mV

For R_L=15k, buffer operates rail to rail. Change of output voltage for this value is shown in Figure 15.

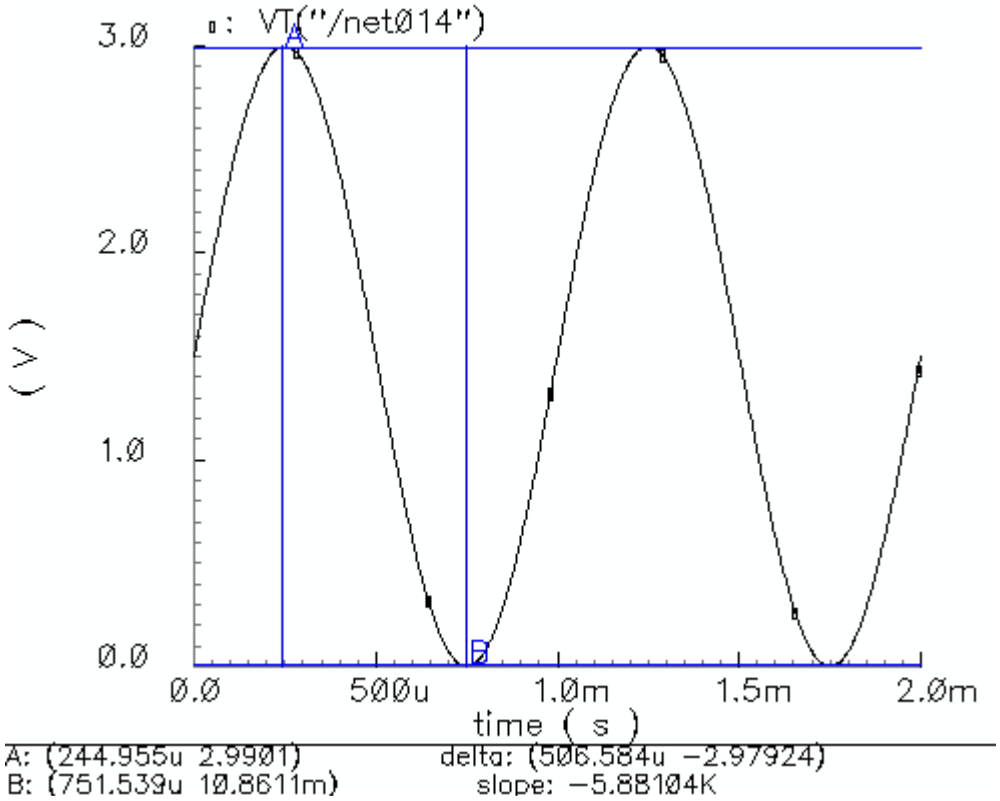

Figure 15: Change of output voltage for 1kHz sine wave after connecting R_L=15k

In Table 2, summary of important performance parameters are given.

Table 2: Summary of important performance parameters

	C compensation	R-C Compensation
DC Power Consumption	2.7mW	2.7mW
Minimum Gain	96.5dB	96.5dB
Worst Case PM	70.3º	71º
Worst Case GBW	35.8MHz	77.6MHz
Slew Rate Rise	70V/µs	140V/µs
Slew Rate Fall	65V/µs	130V/µs
Offset Voltage	60µV	60µV

5. CONCLUSION

In this project, a rail to rail OPAMP is designed. 70dB gain and 70º PM specs are provided. Other performance parameters GBW, power consumption, SR are also taken into account and optimized. Firstly, only C compensation is done and after that series R is added to compensation capacitor so that GBW and SR are doubled. From large signal performance it is seen that OPAMP operates rail to rail. In project 1, it is seen that input stage could operate about 2.5V. From the simulations, it is seen that OPAMP can also operate about 2.5V. If V_{DD} voltage is decreased below 2.5V, OPAMP can operate but important performance parameters Gain, PM, GBW change about 10% from their nominal values due to change in G_{mt} of the input stage.

REFERENCES

[1] Dennis Monticelli, “A quad CMOS single-supply Op Amp with rail-to-rail output swing,” IEEE J. Solid-State Circuits, vol. 21, no. 6, pp. 1026‑1034, Dec. 1986.

[2] Edgar Sanchez-Sinencio & Andreas G. Andreou (Editors), "Low-voltage/low-power integrated circuits and systems: low-voltage mixed-signal circuits", IEEE Press, New York, 1999.

[3] S. Yan and E. Sanchez-Sinencio, “Low Voltage Analog Circuit Design Techniques: A Tutorial,” *Institute of Electronics,Information and Communication Engineers Transaction on Analog Integrated Circuits and Systems*, Vol. E00-A, pp. 1-17, February 2000.