LOW VOLTAGE ANALOG IC DESIGN

PROJECT 1

CONSTANT Gm RAIL TO RAIL INPUT STAGE DESIGN

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1. Introduction

In this project, two constant Gm input stages are designed. First circuit tries to keep sum of the square roots of the tail currents constant. Second circuit shifts the DC voltage between two input pairs. Design steps and simulation results are given in this work. Simulations are done in Cadence Environment and circuits are designed using UMC018 process technology with 3V.

2. Constant Gm Input Stage Using Square Root Circuit

First circuit is given below in Figure 1.

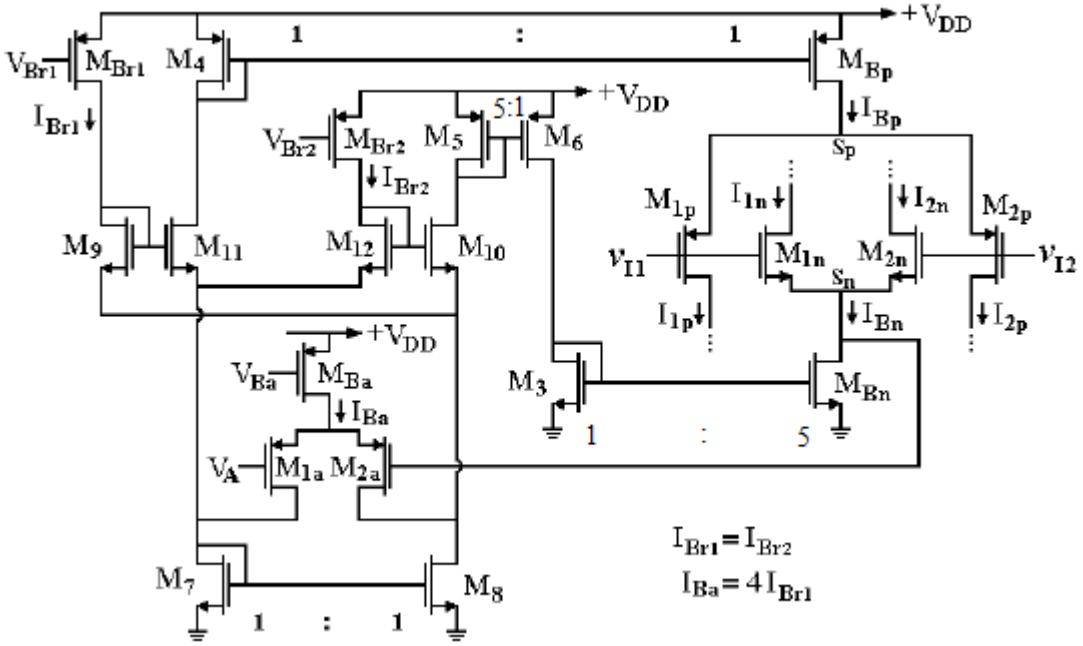

Figure 1: Constant G_m circuit using square root current based method

If common mode input voltage decreases drain voltage of M_{Bn} transistor also decreases and finally it goes into triode region. After that, I_{B10} current which is equal to I_{Bn} decreases. As the drain voltage of M_{Bn} decreases, gate voltage of M_{2a} decreases. V_A voltage is compared to this voltage. If the gate voltage of M_{2a} is lower than V_A, I_{2a} current becomes higher than I_{1a} and I_{11} current increases. For this reason, I_{Bp} current also increases. This is a feedback mechanism and by the help of translinear loop between M9-M12 transistors helps obtaining the equation, $\sqrt{I_{Bn}} + \sqrt{I_{Bp}} = 2I_{Br1}$.

Transistors M_{Br1}, M_{Br2}, M_{Ba} are current sources. V_{Br1}, V_{Br2}, V_{Ba} voltages are chosen equal and their aspect ratios are chosen as $M_{Ba}=4M_{Br1}=4M_{Br2}$ so that $I_{Ba}=4I_{Br1}=4I_{Br2}$ is obtained. Maximum current difference between I_{Bn} and I_{Bp} is limited to $4I_{Br1}$. Aspect ratios of the current mirror transistors are chosen such that $V_{DS,SAT}$ voltage is 100mV.

Input pair transistor dimensions are chosen to keep them in strong inversion. When one input pair is off, dimensions are chosen such that gm of other pair is 250uA/V. Since

maximum current equals to $4I_{Br1}$, dimensions of these transistors can be calculated using $gm = \frac{2I}{V_{gs} - V_t}$ and $gm = \sqrt{2u_{n,p}C_{ox}\frac{W}{L}I}$.

V_{Br1}-V_{Br2}-V_{Ba} voltages are obtained using a diode connected transistor. These voltages are chosen equal to 2.1V. Firstly, I_{Br1} current was chosen 10µA, 15µA. It was seen that there is a large ripple in Gm curve. After that it is seen that for 20µA current, low ripple is obtained. Although it increases power consumption, flatter behavior is obtained. In order to keep power consumption low, aspect ratios of M3-M_{Bn} is chosen 1:5 and M5-M6 5:1. Equations do not change because current of M5-M10 is same with respect to 1:1 ratios. When N-input stage is off, total current is a little more than 14Ibr. This is because although M_{Bn} goes into cutoff region, M3-M6-M5 transistors consume little power. In other case, total current is 15.6Ibr. Thus, worst case current is expected to be 312µA when N-pair is on and P-pair is off.

Choosing V_A voltage is important, because it determines the value of input common mode voltage for which I_{2a} and I_{1a} changes. For a very low V_A voltage, I_{2a} never becomes equal to I_{Ba}. For a large V_A, I_{1a} never becomes equal to I_{Ba}. Dimensions of M_{1a} and M_{2a} are also important. Although their aspect ratios are equal, their current ratios will change if we change aspect ratios of them at the same time. This is valid if gate voltages of these transistors are not equal. Therefore, current of M11-M10 changes and this affects Gm curve. Taking ripple in G_{mt} into account, V_A voltage is chosen 550mV.

Dimensions of the transistors M9-M12 are chosen equal due to the translinear loop. Aspect ratios of these devices also have effect on G_{mt} curve. They change drain voltage of M_{1a} and M_{2a} and this affects current sharing ratio of these transistors. Hence, G_{mt} slightly changes. This is a secondary effect, but must be taken into account. From simulations it is understood that choosing M9-M12 as 5µ/0.5µ and M_{1a}-M_{2a} 6µ/0.5µ provides flatter G_{mt} curve.

Input transistors must be biased in strong inversion because transistors in weak inversion have smaller transconductance and their cutoff frequency is lower [1]. Choosing I_{br} 20µA, tail current becomes 80µA when one input stage is off. The practical values $\mu_n C_{ox}$=118uA/V^2 and $\mu_p C_{ox}$=28uA/V^2 are found using simulator. Lengths of these devices are not chosen minimum due to channel length modulation effect. Using $g_m = \sqrt{2\mu Cox\left(\frac{W}{L}\right)I}$ and simulator $(W/L)_n$=6µ/1µ and $(W/L)_p$=27µ/1µ gives 250µS transconductance when one of the stages is off.

Schematic of the designed circuit is given in Figure 2. Common mode voltage is swept from ground to V_{DD} and AC signal is applied which has 1V differential AC magnitude. Common mode signal is swept by 20mV steps and G_{mt} curve is plotted using G_{mt}=[(I_{1n}-I_{2n})+(|I_{1p}|-|I_{2p}|)]/1V equation. Change of G_{mt} is given in Figure 3.

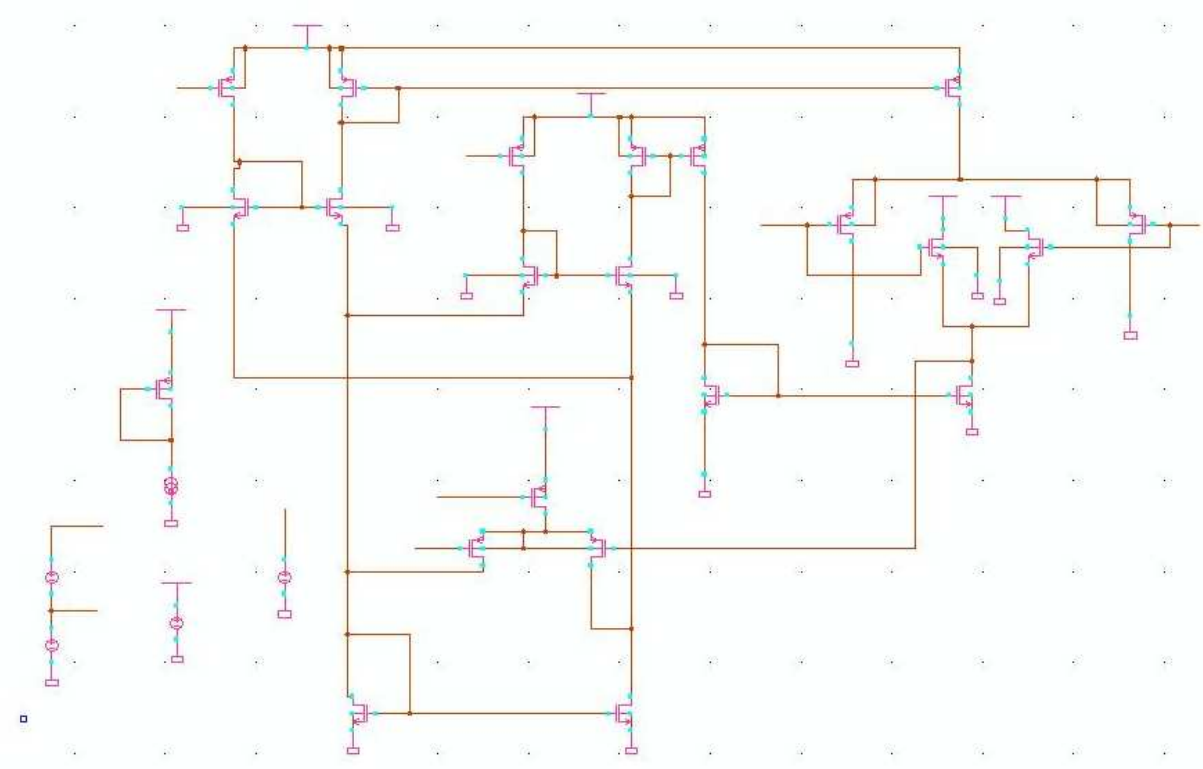

Figure 2: Schematic of square root constant G_m circuit

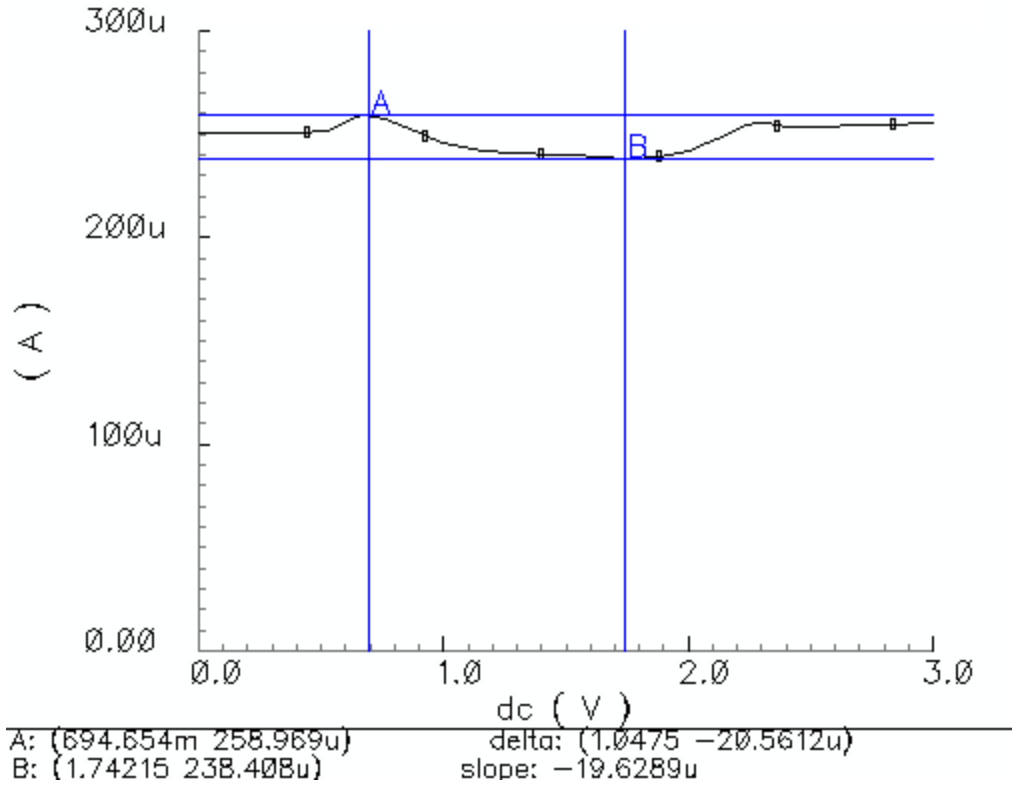

Figure 3: G_{mt}-V_{CM} curve of the circuit in Figure 2

Average value of the G_{mt} in Figure 3 is 248.8µA/V and its ripple equals to ripple1=($G_{mt,Max}$-$G_{mt,Min}$)/G_{mtAv}=20.5µ/248.5µ=8.25%.

In Figure 4, change of total current sunk from DC supply is shown. Since on-off conditions of the circuit are not symmetric curve is not symmetric. Worst case current is 308µA. It is calculated as 312µA. Channel length modulation effect causes this situation.

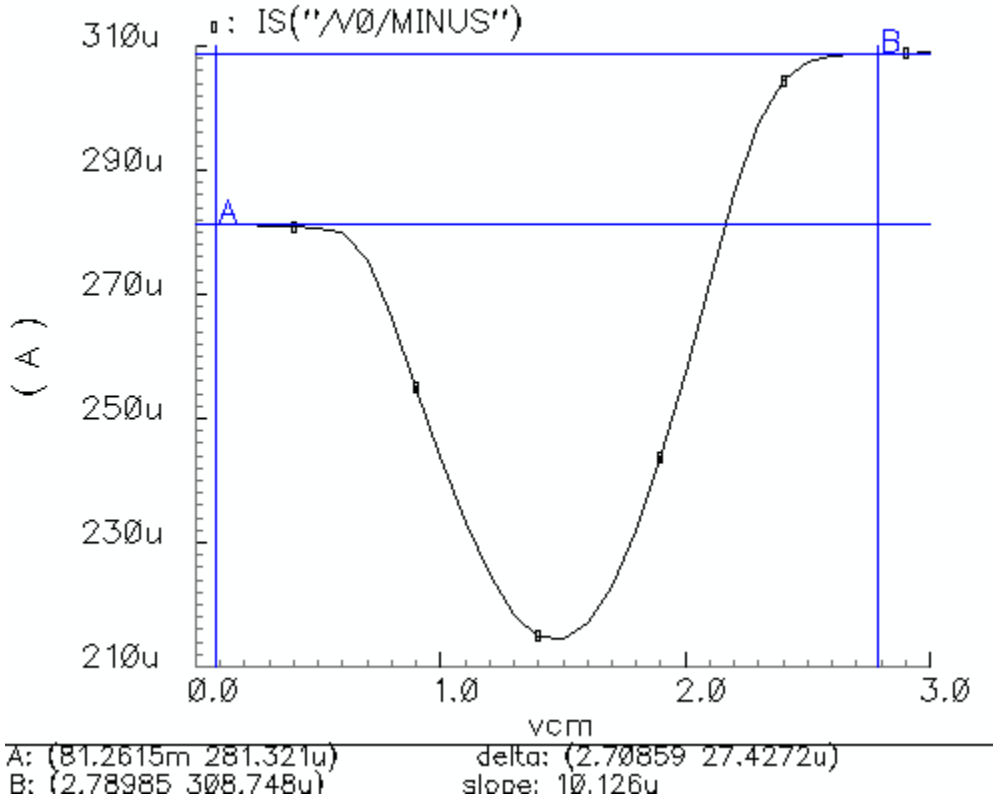

Figure 4: Total current sunk from DC supply vs CM voltage

Dimensions of the transistors are given in Table 1.

Table 1: Transistor Dimensions

Transistors	Dimension, W/L	Transistors	Dimension, W/L
M_{1n}-M_{2n}	6µ/1µ	M_{Bp}	80µ/1µ
M_{1p}-M_{2p}	27µ/1µ	M_4	80µ/1µ
M_{Bn}	50µ/1 µ	M_{Br1}-M_{Br2}	60µ/1µ
M_3	10µ/1µ	M_{Ba}	240µ/1µ
M_6	20µ/1µ	M_{1a}-M_{2a}	6µ/0.5µ
M_5	100µ/1µ	M_9-M_{12}	5µ/0.5µ
M_7-M_8	50µ/1µ		

In Figure 5, G_{mt} curves for different power supply voltages changing from 2.5V-3V are given. It is seen that when one pair is off, change of power supply does not have much effect since the transistors are in saturation. However, it shows its effect when both transistors are on. Lowering supply voltage is a problem especially for PMOS transistors because first they change their operating region. Circuit still operates at 2.5V.

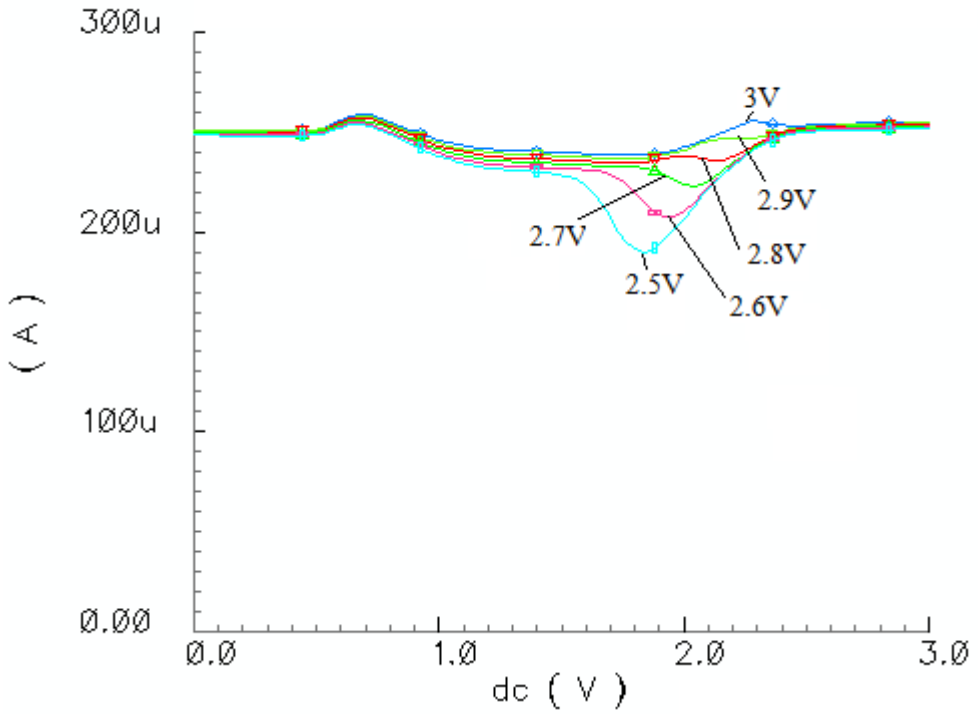

Figure 5: G_{mt} curve for different power supply voltages

3. Constant Gm Input Stage Using DC Level Shift Method

Second input stage is given in Figure 6 which is proposed in [2].

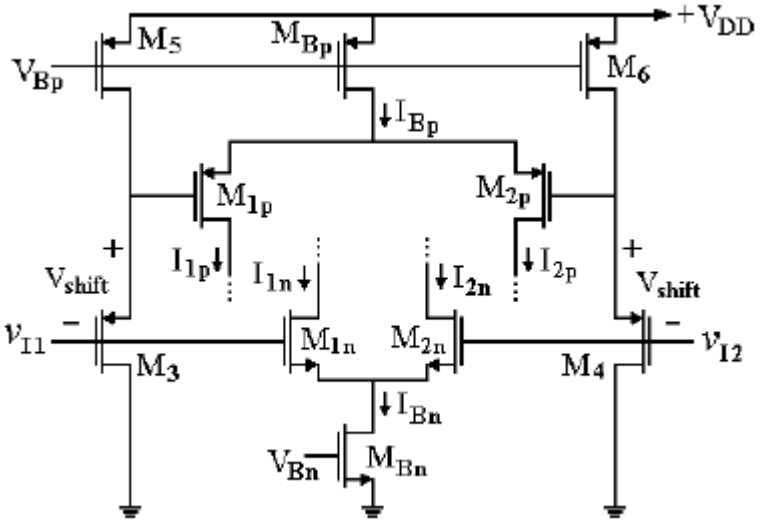

Figure 6: Input Stage using DC level shift

M_3-M_4 transistors together with their bias current sources, M_5-M_6, shift the input DC voltage. Thus, increment in G_{mt} curve due to both on regions of input pairs is avoided. Thus, flatter G_{mt} curve is obtained. This method again relies on B_n=B_p matching.

The transistors M_5-M_6-M_{Bp} and M_{Bn} are biased by two diode connected transistors as shown in Figure 7. Overdrive voltages of these transistors are chosen 100mV in order to keep voltage headroom low.

Tail currents are chosen 40µA for strong inversion. Dimensions of the input transistors are chosen such that when one input stage is off, G_{mt} becomes 250µA/V. Minimum channel length is chosen 1µm due to channel length modulation problems and corresponding widths are found using g_m formula. Then, these values are adjusted using simulator.

Aspect ratios of M_{bn3}:M_3:M_{bn} are chosen 1:1:8 in order to keep power consumption low. I_{br} current is chosen 5µA. When only PMOS stage is on, M_{bp3}-M_5-M_6-M_{bn3} transistors consume $4I_{br}$ and M_{bp} consumed $8I_{br}$. Therefore, total current becomes $12I_{br}$. It is 60µA for 5µA I_{br}. For high values of V_{CM}, N-input stage is on, P stage is off and M_5-M_6 transistors are driven into triode region. M_{bn3}-M_{bp3} transistors consume $2I_{br}$ current and M_{bn} consumes $8I_{br}$. Total current becomes $10I_{br}$ which is equal to 50µA.

From simulations it is seen that G_{mt} curve is too much sensitive to M_3-M_4 transistors and also to change in power supply voltage. Overlapping region of g_{mn} and g_{mp} can easily change and this results in positive or negative peaks in G_{mt}.

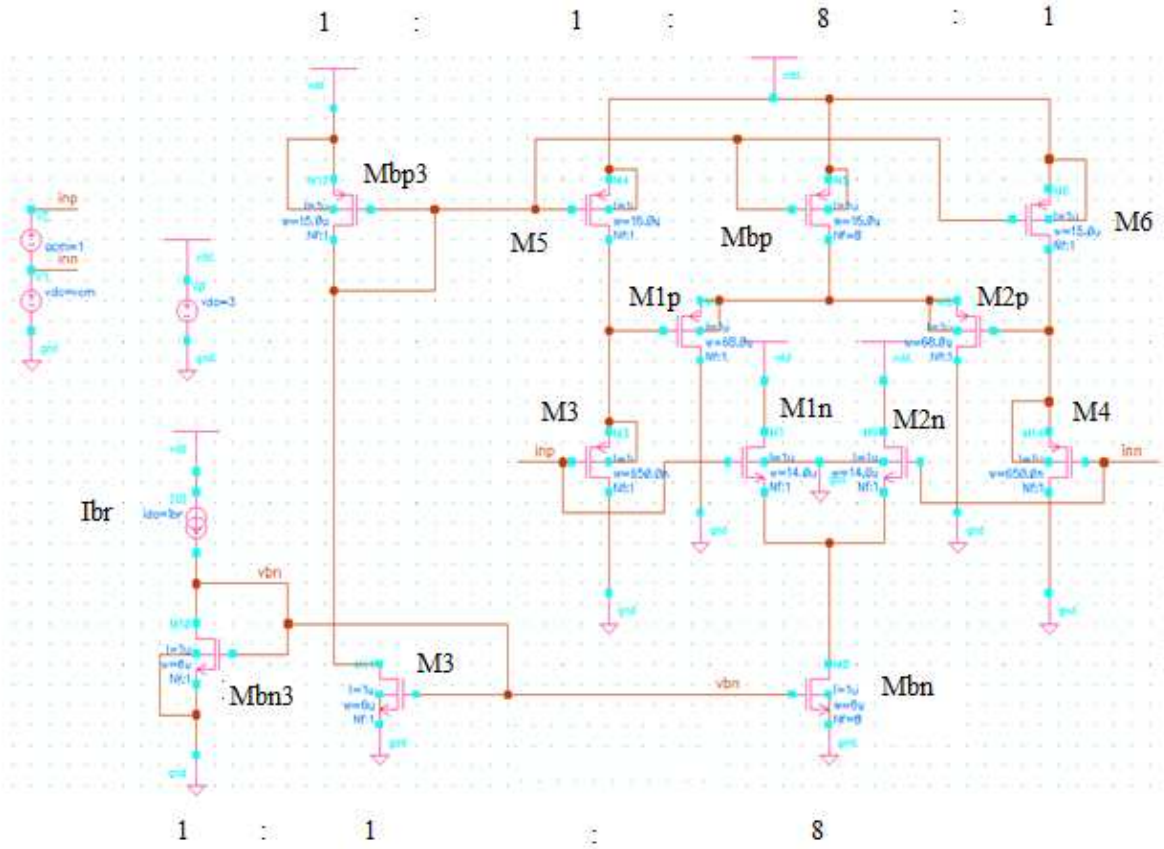

Figure 7: Schematic of the 2nd circuit

Change of G_{mt} curve with V_{CM} is given in Figure 8. Average value of G_{mt} is 248.2µA/V and its ripple equals to $(G_{mt,Max}-G_{mt,Min})/G_{mt,Av}$=17.1/248.2=6.9%.

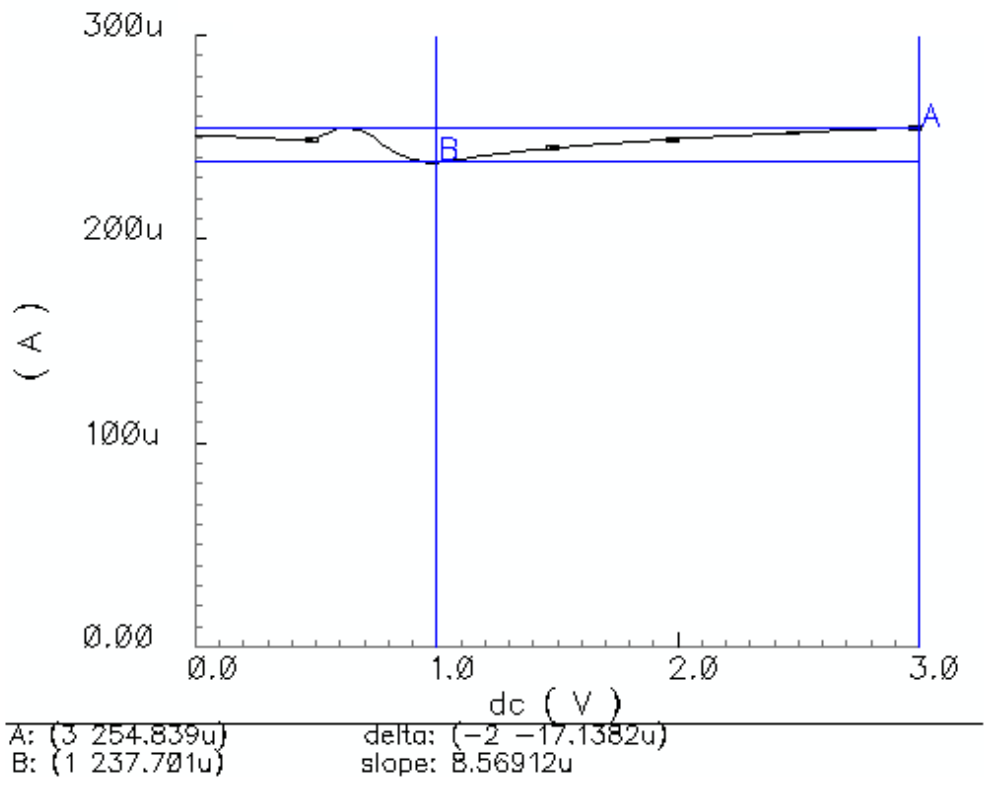

Figure 8: G_{mt}-V_{CM} curve for DC level shift input stage

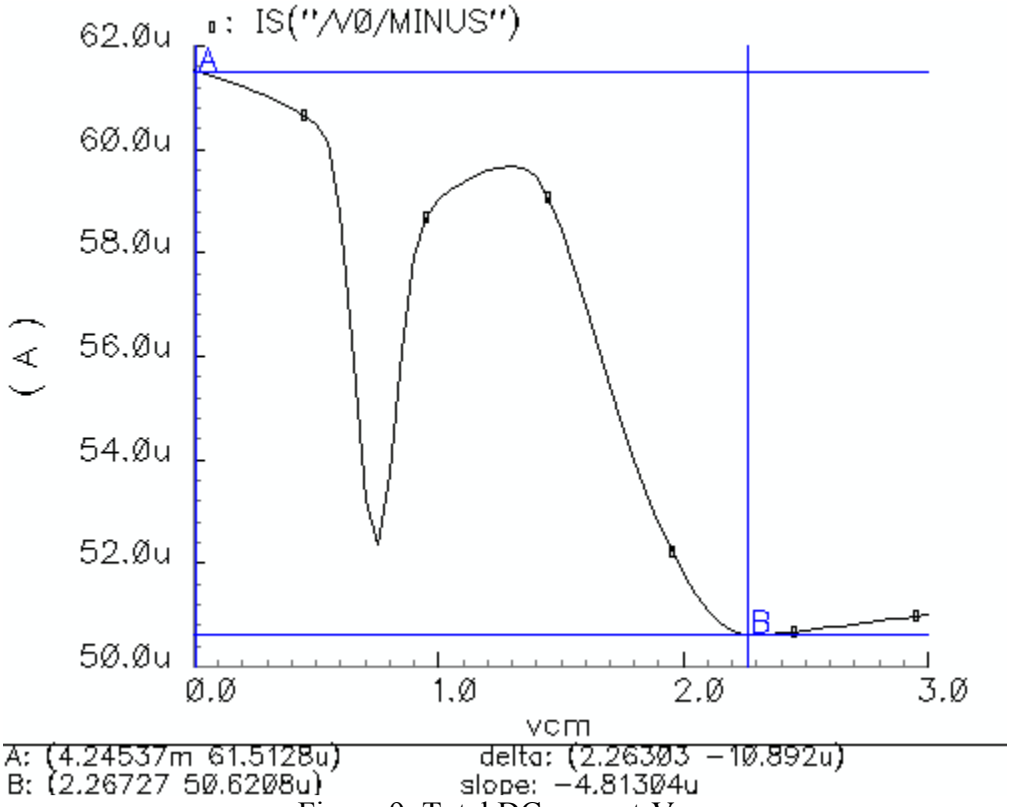

Figure 9: Total DC current-V_{CM}

In Figure 9, change of total current sunk from DC supply is given. Minimum and maximum currents are calculated before as 50µA and 60µA. Simulation results are as expected. Channel length modulation effect causes some error. I_{bp}-I_{bn} currents intersect around 0.8V and sum of them decreases. This situation can easily be seen from Figure 10. After 0.8V, I_{bn} current increases and total current consumption increases. After 1.5V, current of M_3 starts to decrease. Thus, total current decreases.

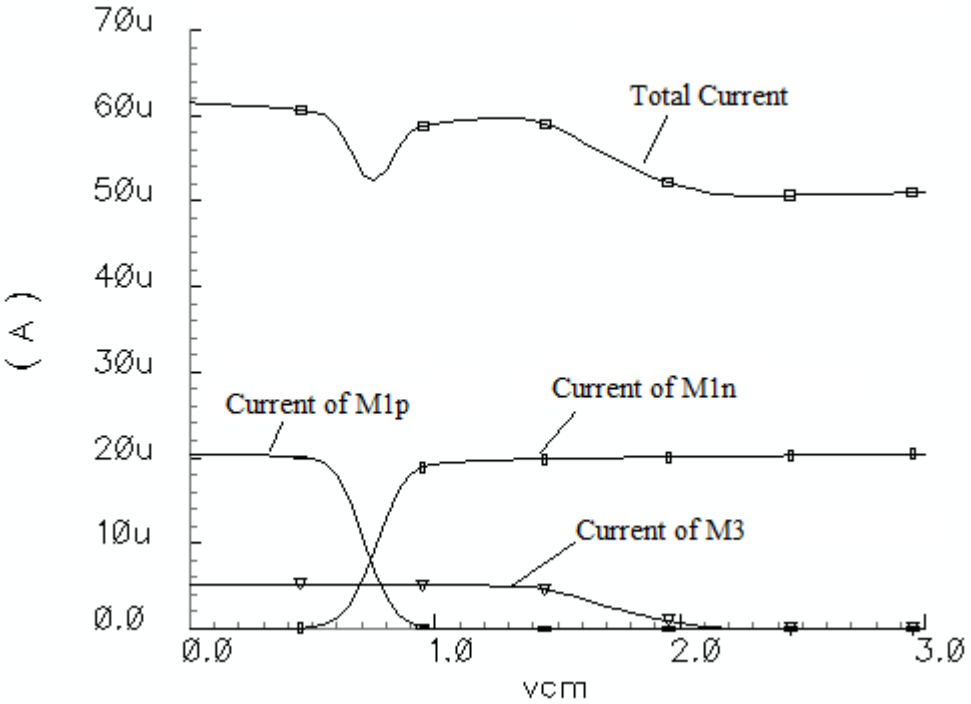

Figure 10: Change of M_{1n}-M_{1p}-M_3 currents

Device dimensions are given in Table 2.

Table 2: Device dimensions

Transistor	Dimension (W/L)	Transistor	Dimension (W/L)
M_{1n}-M_{2n}	14µ/1µ	M_{1p}-M_{2p}	68µ/1µ
M_{Bn}	48µ/1µ	M_{bp3}-M_5-M_6	15µ/1µ
M_3-M_{bn3}	6µ/1µ	M_3-M_4	0.65µ/1µ
		M_{Bp}	120µ/1µ

4. Conclusion

In this project, two constant G_m input stages have been designed with UMC018 process and simulated with BSIM3v3 parameters and their simulation results are given.

First circuit is a square root circuit which uses current base method to obtain constain G_m. Its ripple is 8.25% and its maximum DC power consumption is 927μW. Power consumption of this circuit can be decreased using less tail current. However, it is seen from the simulations that ripple increases. Disadvantage of this circuit is that it relies on quadratic equation of MOSFET which is not exact in all cases and it is more complex than the second circuit. It still operates at 2.5V.

Second circuit uses DC level shift method. Its ripple is lower than the first one. It is 6.9%. DC power consumption is also lower than the first one. Its maximum value is 183μW. Second circuit is simpler than the first one. However, simulations show that it is sensitive to M_3-M_4 transistors and power supply change too much. At 2.9V, its G_m at transition region decreases down to 200μS which cannot be neglected. It can also be added that layout of first circuit occupies larger area.

REFERENCES

[1] J. H. Botma, R. F. Wassenaar, and R. J. Wiegerink, “A low voltage CMOS op amp with a rail-to-rail constant-gm input stage and a class AB rail-to-rail output stage,” EEE Proc. ISCAS 1993, vol. 2, pp. 1314-1317, May 1993.

[2] Wang, M., Mayhugh,Jr., T.L., Embabi, S.H.K. and Sanchez-Sinencio, E., “*Constant-gm rail-to-rail CMOS op-amp input stage with overlapped transition region,*” IEEE J.Solid-State Circuits, vol.34, no.2, pp.148–156, 1999.