SYNOPSYS®
Predictable Success

Platform Architect

SoC Architecture Performance Analysis and Optimization

Overview

Synopsys Platform Architect is a SystemC TLM standards-based graphical environment for capturing, configuring, simulating, and analyzing the system-level performance of next-generation SoC architectures.

Platform Architect enables system designers to explore and optimize the configuration of the SoC infrastructure, specifically the global interconnect and memory subsystem, to achieve the right system performance and cost.

Its efficient turnaround time, powerful analysis views, and available IP models make Platform Architect the premier choice for system-level performance analysis and optimization of ARM AMBA®-based SoCs.

Platform Architect is a production-proven solution used by leading Systems OEMs and Semiconductor companies worldwide.

SYSTEMC™

Highlights

- SoC Interconnect and Memory Sub-system Performance Optimization
- Efficient Exploration Using Traffic Generation and Cycle-Accurate TLM Interconnect Models
- Powerful Performance Analysis Visualization for Root-Cause and Sensitivity Analysis
- Hardware-Software Validation Using Cycle-Accurate TLM Processor Models
- IEEE 1666 SystemC TLM Standards-based Environment

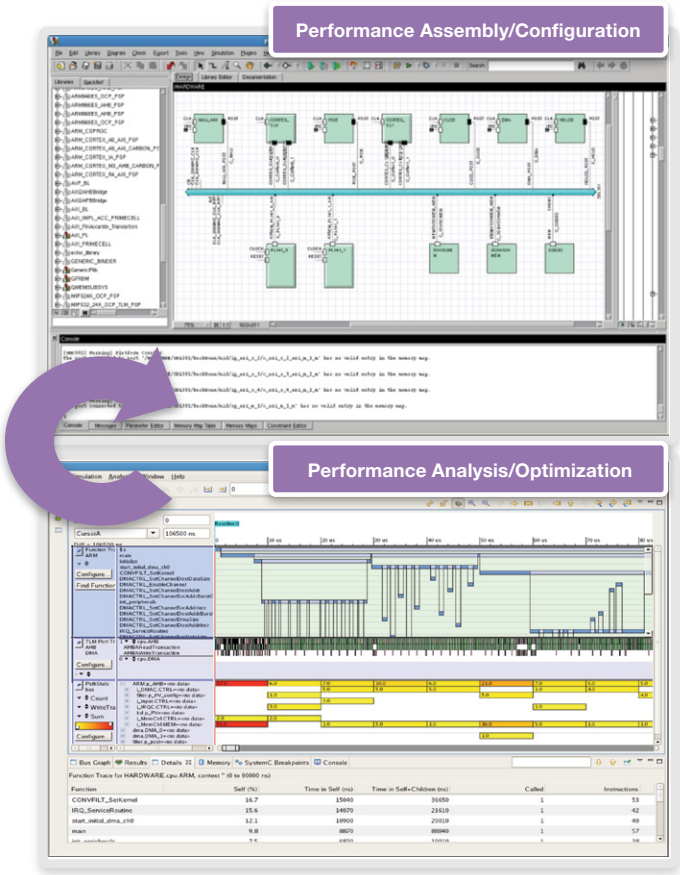

Figure 1: Graphical platform assembly, configuration, performance analysis, and optimization of AMBA-based SoC designs in Synopsys Platform Architect

Problem: Predicting Dynamic System Performance

Predicting the dynamic system performance of today's multi-function, multi-application SoCs requires simulation. This impacts both System OEMs and Semiconductor companies, and creates an opportunity for information sharing and collaboration within the supply chain.

Challenges with Traditional Methods

Discovering system performance problems late in the development cycle can be catastrophic to project schedules and product competitiveness, causing failure in the market. Accurate performance analysis must be done earlier in the design cycle.

- While spreadsheets are good for aggregating data, static spreadsheet calculations are not accurate enough to estimate performance and take design decisions. Simulation is needed
- Traditional RTL simulation is too slow and lacks the configurability and visibility to analyze performance. In addition, the RTL may simply not be available
- Risks including overdesign, underdesign, cost increases, schedule delays, and re-spins

Solution: System-Level Simulation and Performance Analysis

System-level performance analysis in Synopsys Platform Architect provides system designers with the transaction-level simulation, rapid turnaround time, and powerful system-level visibility they need to greatly improve the analysis and decision making process.

Interconnect and Memory Subsystem Performance Optimization Using Trace-Driven Traffic Generation

Platform Architect focuses on the architecture design challenges associated with the optimization and performance validation of the backbone SoC interconnect and global memory subsystem.

- Dynamic application workloads are modeled using traffic generation, enabling early measurement of system performance before software is available
- Simulation sweeping enables performance data to be collected parametrically, exploring all traffic scenarios against the complete of range architecture configurations.
- Powerful tools for analysis visualization provide graphical transaction tracing and statistical analysis views that enable you to identify performance bottlenecks, determine their root-cause, and examine the sensitivity that system performance may have to individual or combined parameter settings
- The result is an executable specification used to carefully dimension the SoC interconnect and memory subsystem to support the latency and bandwidth requirements of all SoC components, under all operating conditions

Product trends requiring analysis	Results with Platform Architect
• Multiple initiators and software stacks • Dynamic workloads • Complex arbitration • Advanced QoS capabilities	• Measurable improvement in product performance • Reduce schedule risk by 50% vs. traditional methods

Figure 2: SoC performance analysis challenges and the benefits of using system-level methods for performance analysis in Synopsys Platform Architect

Hardware/Software Partitioning and Performance Optimization of Using Task Mapping

Application Task Mapping, or ATM, enables architects to create task-driven workload models of their end-product application.

- Generic task models are easily configured to create a SystemC performance model of the application, called a task-graph
- Using the task-graph, the performance workload of parallel application tasks are mapped onto Virtual Processing Unit (VPU) task-driven traffic generators
- Simulation and task analysis enables hardware/software partitioning to be optimized for best system performance well before the application software is available
- Task graphs are fully reusable as task-driven traffic generators for Interconnect and Memory Subsystem Performance Optimization in combination with trace-driven traffic generation

Hardware/Software Performance Validation Using Processors Models and Critical Software

After exploration the performance model of the candidate architecture can be refined to replace the trace-driven and task-driven traffic generators with cycle-accurate processor models.

- This enables architects to validate the candidate architecture using the available performance critical software
- Software and hardware analysis views can be visualized together to provide unique system-level visibility to measure performance and confirm goals are met

Model debugging using TLM port transaction tracing and analysis

Sensitivity analysis using pivot charts to aggregate and explore results

Root cause analysis using bus path and resource utilization statistics

Combining hardware and software analysis for performance validation

Figure 3: Powerful performance analysis visualization for root-cause and Sensitivity Analysis in Platform Architect

Complete IEEE 1666 SystemC TLM Standards-based Environment

Platform Architect is a native SystemC environment fully compatible with the IEEE 1666 SystemC Language Reference Manual (LRM). It supports the assembly, simulation, and analysis of models containing mixed levels of abstraction including:

- Standards-based SystemC transaction-level models using Open SystemC Initiative (OSCI) TLM-2.0 and Open Core Protocol International Partnership (OCP-IP) TLM industry standards, and the open Synopsys SystemC Modeling Library (SCML) API library for highly reusable TLM-2.0 based peripheral modeling
- Mixed SystemC/HDL co-simulation with Synopsys VCS and other third party HDL simulation environments enabling reuse of RTL memory controllers and other IP components
- Plus, models used in Platform Architect for performance analysis can be reused to accelerate the creation of Synopsys Virtual Prototypes for software development and software-driven verification

Getting Started with Available Architecture IP Models

Platform Architect supports the broadest commercially available portfolio of pre-instrumented SystemC TLM IP models for architecture exploration and validation.

Traffic Generators

- Generic File Reader Bus Master (GFRBM) for trace-driven traffic generation
- Generic Virtual Processing Unit (VPU) for application task-mapping and task-driven traffic generation

Interconnect Models

- Cycle-accurate SystemC TLM bus libraries for ARM AMBA 2 AHB™/ APB™, AMBA 3 AXI™ (PL300), and CoreLink™ Network Interconnect (NIC-301)
- Generic approximately-timed SystemC TLM bus libraries for industry-standard OCP-IP and OSCI TLM-2.0

Memory Controller Models

- Generic approximately-timed SystemC TLM memory subsystem models for ARM AXI, OCP-IP, and OSCI TLM-2.0 interfaces
- Cycle-accurate SystemC TLM memory subsystem models for ARM PL172 (AHB), PL320 (AXI), PL340 (AXI), and PL341 (AXI) Primecells

Processor Models

- Cycle-accurate SystemC TLM processor support packages (PSPs) for ARM, MIPS, and Tensilica processor families
- Plus custom processor PSPs generated by Synopsys Processor Designer

CoStart Methodology Guidelines and Examples

More than tool-clicks, Synopsys CoStart methodology guidelines and examples for Platform Architect help educate users on Synopsys' state-of-the-art architecture design flow.

- Deployed exclusively through Synopsys CoStart Enablement Services
- Ensures end-user value at each step, accelerating results
- Minimizes modeling effort to get started and achieve initial value
- Maximizes ROI through exploration (not just checking)

CoStart Enablement Services

Synopsys CoStart is a packaged service that shortens the ramp-up cycle for architecture design methodologies so that users become productive in the shortest time.

The Synopsys CoStart program contains an intense knowledge transfer, while assisting in architecture study project planning, use case traffic capture, performance model creation, simulation, and analysis of results.

- Tool, IP model, and methodology training
- Exclusive access to CoStart Methodology Guidelines and Examples
- Modeling services for the development and integration of custom interconnect and memory subsystem models
- Expert consulting and support

About Synopsys System-Level Solutions

Platform Architect is part of a comprehensive system-level offering from Synopsys. Synopsys' System-Level Solutions:

- Provide the broadest portfolio of systems-level IP models from a single supplier
- Accelerate the creation and optimization of common SoC blocks
- Facilitate SoC architecture exploration and optimization
- Provide the most complete prototyping solutions to accelerate embedded software development and system validation
- And enable value throughout the semiconductor supply chain

For more information on System-Level Solutions, visit: http://www.synopsys.com/sld.

For more information on Platform Architect visit: http://www.synopsys.com/platformarchitect.

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