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LETTER

Seventh-order elliptic video filter with 0.1 dB pass band ripple employing CMOS CDTAs

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Abstract

In this paper, a CMOS realization of the current differencing transconductance amplifier (CDTA) is given, which is a newly reported active building block for current-mode signal processing. Current differencing stage of the CDTA element is realized using a differential current-controlled current source and in the output stage, floating current sources are used to convert intermediate voltage of z terminal to output currents. Due to the compactness of the circuit, it is capable of high-frequency operation and suitable for video signal-processing applications. The CDTA element is used in a current-mode anti-aliasing video filter, which is designed using operational simulation of a seventh-order passive elliptic filter, so the resulting active filter has the low sensitivity feature of its passive counterpart. The filter has 0.1 dB maximum pass band ripple as imposed by ITU video anti-aliasing filter standard. SPICE-simulation results of both the CDTA element and the seventh-order elliptic filter are given. Simulation results are found in close agreement with theoretical results.

Keywords: Current-mode circuits; CDTA; Video filter

1. Introduction

In many signal-processing applications, current-mode circuits have become very good alternatives to voltage mode counterparts due to their relative large bandwidths. In current-mode circuits, current source-driven low impedance nodes carry current signals. That leads to higher-frequency poles and results in high-frequency operation. Moreover, since voltages are not essentially involved in signal processing, it is possible to design circuits at low-supply voltages that are capable of high-frequency operation [1]. Because of those features, the interest towards current-mode signal processing has steadily increased among many researchers and numerous current-mode circuit structures are proposed [2–6].

Current differencing transconductance amplifier (CDTA) is a recently reported current-mode active building block [7]. It leads to very compact circuit structures. Especially, when more than two output terminals are used, it is possible to obtain very compact circuit topologies requiring less passive elements. It is shown recently that using only three multi-output CDTA and three all grounded passive elements, five mostly used filter transfer functions are generated simultaneously with theoretical minimum passive element sensitivities [8].

2. CDTA

CDTA is a five terminal current-mode active building block. It can be also seen as a current operational amplifier if the intermediate z terminal is not taken outside. Its symbol

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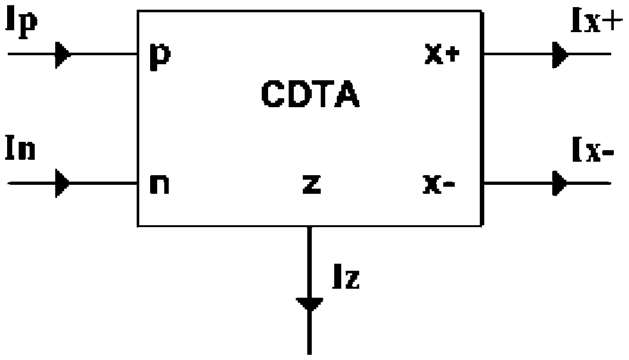

Fig. 1. Symbol of the CDTA element.

is in Fig. 1 and defining equations are given in (1).

$$V_p = V_n = 0, \quad I_z = I_p - I_n,$$
$$I_{x+} = gV_z, \quad I_{x-} = -gV_z. \tag{1}$$

Differential input current flows over the z terminal. Usually, an external impedance is connected to this node and the voltage over this impedance is converted to the output currents by the output transconductors with transconductance g for the positive output and $-g$ for the negative output.

Intermediate z terminal of the CDTA can be very handy if a circuit is to be designed with all grounded passive elements which is good in view of process-dependent realization issues. Since input differential current flows over that z terminal it is possible to use one or more than one grounded passive elements to convert this differential current to voltage which seems a very promising method to obtain compact designs.

3. CMOS realization of CDTA and simulation results

Since difference of the input current signals, similar to current differencing-buffered amplifier (CDBA) [9], flows over CDTA, it is meaningful to choose such a stage used for CDBA input stage [8]. The difference of the CDTA is that it has an output transconductor with dual outputs whereas CDBA uses a current buffer as an output stage. Floating current sources are used as output transconductors of the CDTA because of their high-current-tracking accuracy and compactness [10]. One drawback of this structure is the inability to tune the transconductance of the element without changing the bias currents. If it is needed to tune the g parameter independently, tunable transconductance stages must be used as output transconductors.

A CMOS realization of the CDTA element is shown in Fig. 2. The transistors $M1$ to $M16$ form the input differential current-controlled current source (DCCCS) stage which is used for transforming the differential input current to the intermediate voltage which is the voltage at the z terminal. $M17$ to $M22$ form the dual-output transconductor stage [8]. A compensation capacitor of 1 pF is used to guarantee the stable closed-loop operation with sufficient phase margin. Aspects of the transistors in Fig. 2 are given in Table 1. To note that aspects of the $M8$ and $M9$ should be chosen two times of the $M3$, $M4$ and $M12$, $M13$ transistors in order to operate the input stage correctly.

Table 1. Aspect ratios of the transistors

$M1 = 8\,\mu m/1\,\mu m$	$M12 = 20\,\mu m/1\,\mu m$
$M2 = 8\,\mu m/1\,\mu m$	$M13 = 20\,\mu m/1\,\mu m$
$M3 = 20\,\mu m/1\,\mu m$	$M14 = 30\,\mu m/1\,\mu m$
$M4 = 20\,\mu m/1\,\mu m$	$M15 = 30\,\mu m/1\,\mu m$
$M5 = 8\,\mu m/1\,\mu m$	$M16 = 30\,\mu m/1\,\mu m$
$M6 = 8\,\mu m/1\,\mu m$	$M17 = 50\,\mu m/1\,\mu m$
$M7 = 30\,\mu m/1\,\mu m$	$M18 = 45\,\mu m/1\,\mu m$
$M8 = 40\,\mu m/1\,\mu m$	$M19 = 45\,\mu m/1\,\mu m$
$M9 = 40\,\mu m/1\,\mu m$	$M20 = 10\,\mu m/1\,\mu m$
$M10 = 30\,\mu m/1\,\mu m$	$M21 = 10\,\mu m/1\,\mu m$
$M11 = 30\,\mu m/1\,\mu m$	$M22 = 50\,\mu m/1\,\mu m$

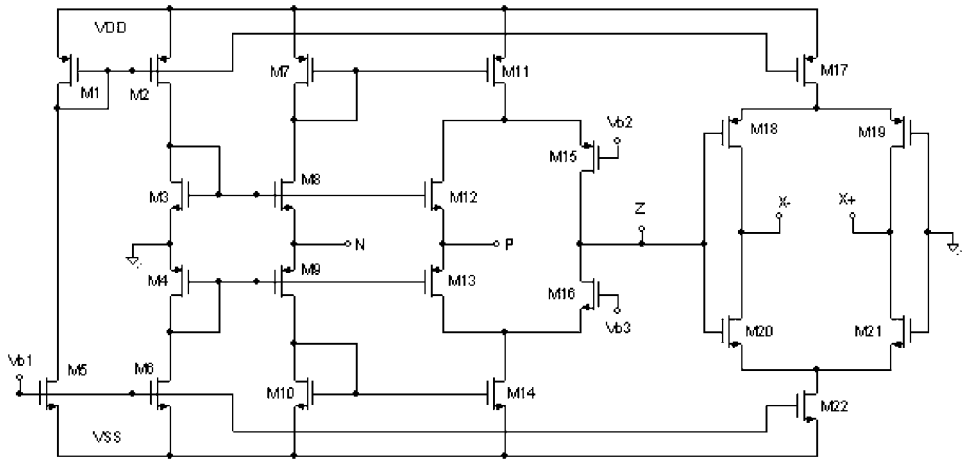

Fig. 2. CMOS realization of CDTA.

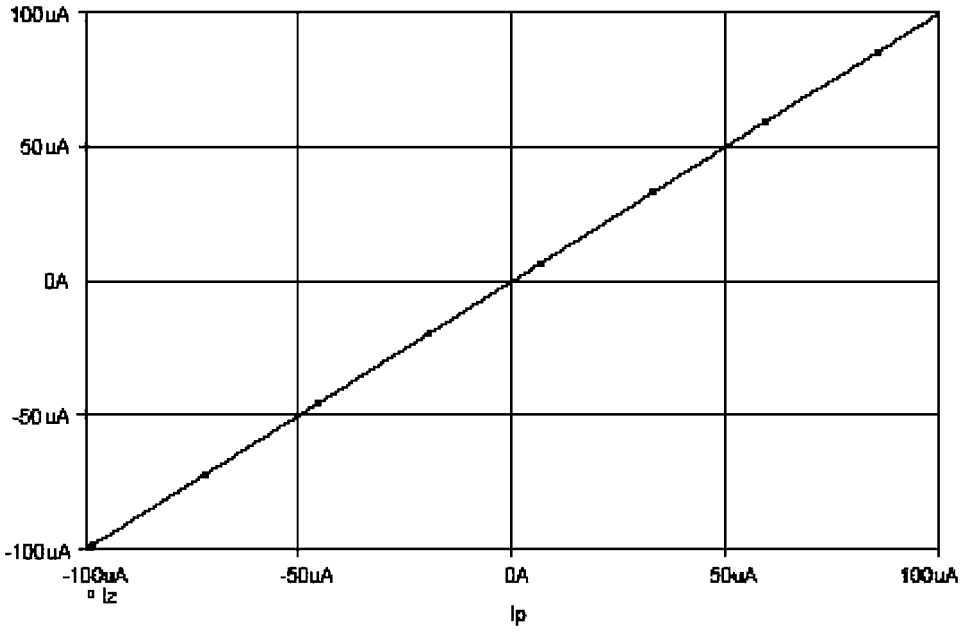

Fig. 3. Current transfer from p to z.

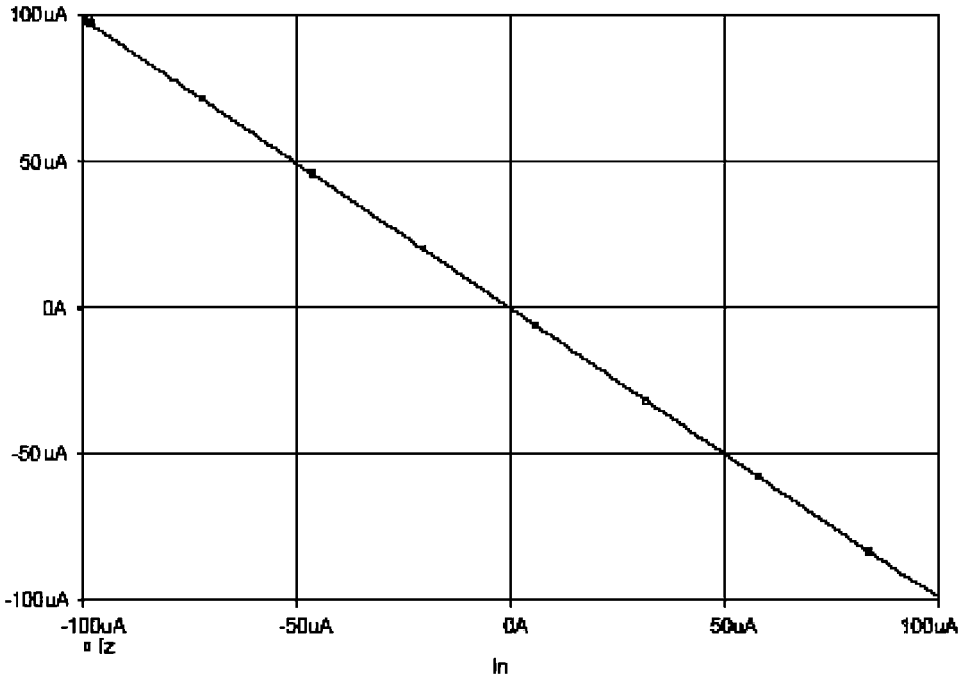

Fig. 4. Current transfer from n to z.

SPICE simulations are conducted using process parameters of 0.5 μm MIETEC technology. Supply voltages are chosen as ±2.5 V. Input terminals' current transfer characteristics are given in Figs. 3 and 4, respectively. Figures are obtained when one input is open circuited. Input stage transfers the difference of the input currents to the z terminal with good accuracy as demonstrated by the figures.

Since few internal nodes exist over the signal path from input to the z terminal of the input stage, high-frequency operation is satisfied exploiting the high-frequency capability

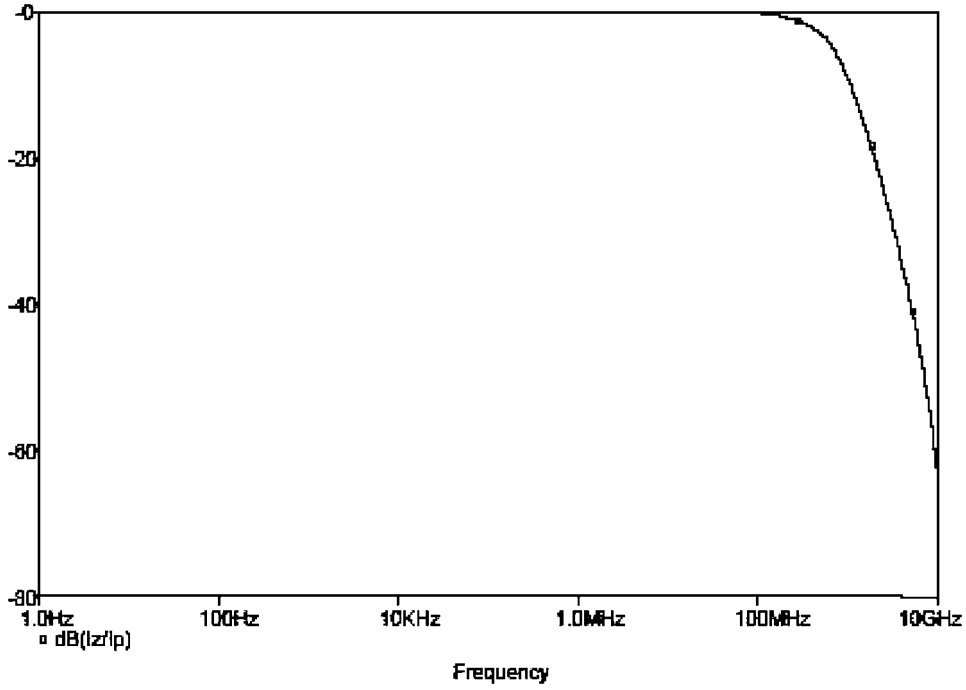

Fig. 5. Variation of I_z/I_p.

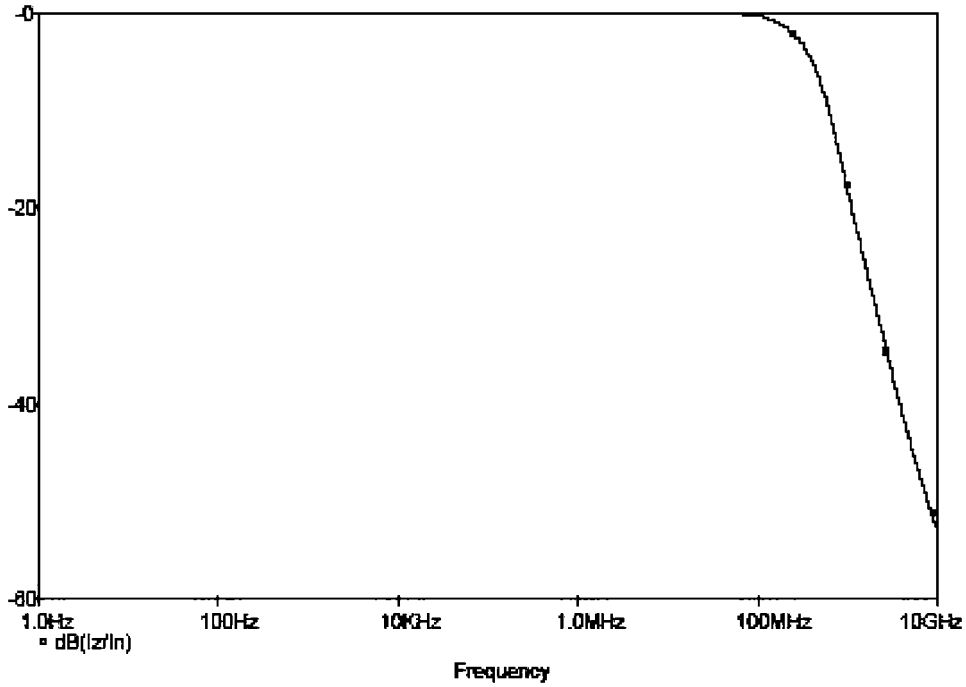

Fig. 6. Variation of I_z/I_n.

of current mode signal processing. Figs. 5 and 6 show AC responses of the variation of the current at the z terminal with respect to input currents.

Variation of dual output transconductance stage's output currents with respect to the input current is given in Fig. 7. According to the direction of the output currents it is possible to obtain different CDTA elements so we can also have CDTA $++$ where both output currents flow outside of the element or CDTA $--$ where both output currents flow inside of the element [7]. These CDTA elements can

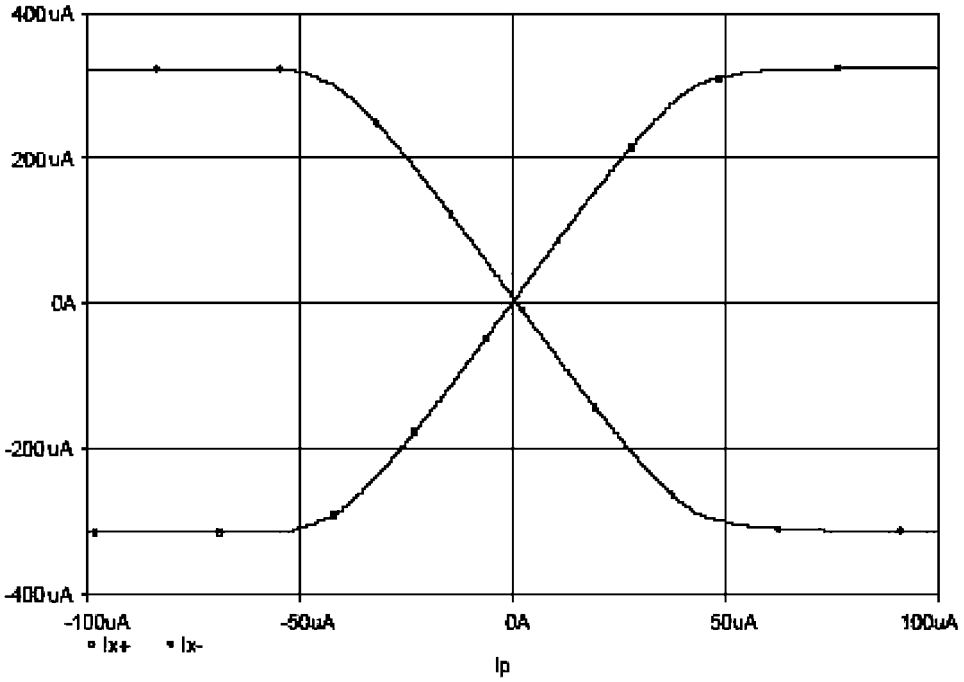

Fig. 7. Variation of the current of x− and x+ terminals with respect to I_p input current (z terminal is loaded with a 20 kΩ impedance).

Table 2. Simulation results

I_z/I_p (−3 dB) bandwidth (MHz)	497
I_z/I_n (−3 dB) bandwidth (MHz)	301
P input resistance	1.24 kΩ at 100 MHz
N input resistance	834 Ω at 100 MHz
Power consumption (mW)	4
Transconductance (g) (μA/V)	400

be used for different applications and can be very handy in some circuits where the others are clumsy.

Transconductance parameter of the CDTA element in the circuit is determined by the transconductance of output transistors. It can be approximated as

$$g = \frac{g_{m18} + g_{m20}}{2}. \quad (2)$$

Summary of the simulation results of the CDTA element is given in Table 2. As seen from Table 2, current transfer from p and n terminals to the z node is achieved over a very large bandwidth. Output transconductor stage is build by floating current sources which is also reported for high-frequency operation [10]. Input resistances of the p and n terminals are moderately low at 100 MHz. Power consumption of the circuit is 4 mW when the transconductance is set to 400 μA/V by adjusting the biasing current of the circuit. If transconductance of the circuit is to be tuned without changing the bias current of the output transconductors, tunable transconductance stages can be used at the output trading off the circuit simplicity.

4. Seventh-order video anti-aliasing filter employing CDTAs

Efficient anti-aliasing is one of the main requirements in today's video processing circuits. Anti-aliasing filters are used before on ADC to attenuate signals above Nyquist frequency which characteristics are strictly determined by ITU BT 601 standard. These characteristics are chosen very tight to establish smooth picture quality. However, to satisfy these specifications of anti-aliasing filter is difficult for many analog filters. Therefore, design of analog anti-aliasing filter structures is an important and challenging application area for filter designers.

ITU BT 601 standard recommends a low-pass filter which has a bandwidth of 5.75 MHz with maximum 0.1 dB passband ripple and attenuation greater than 45 dB at 8 MHz. Group delay is also another important specification of video filters and it is recommended by ITU for anti-aliasing filter as less than 5 ns over the whole pass band.

With computer aid, it can be shown that a seventh-order elliptic filter will be sufficient to meet the specified requirements. It is also sensible to choose a passive filter first, and then make it active using active blocks, because of the passive filter low sensitivity feature. Operational simulation is a well known and effective method to simulate passive filters

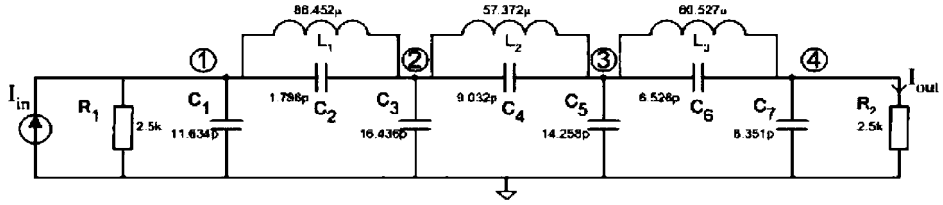

Fig. 8. Seventh-order passive elliptic low-pass filter.

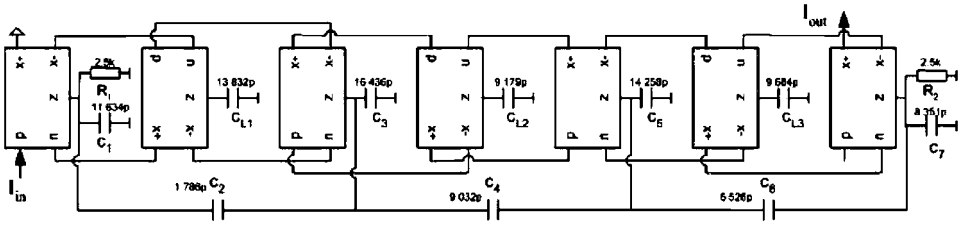

Fig. 9. Seventh-order passive elliptic low-pass filter employing CDTAs.

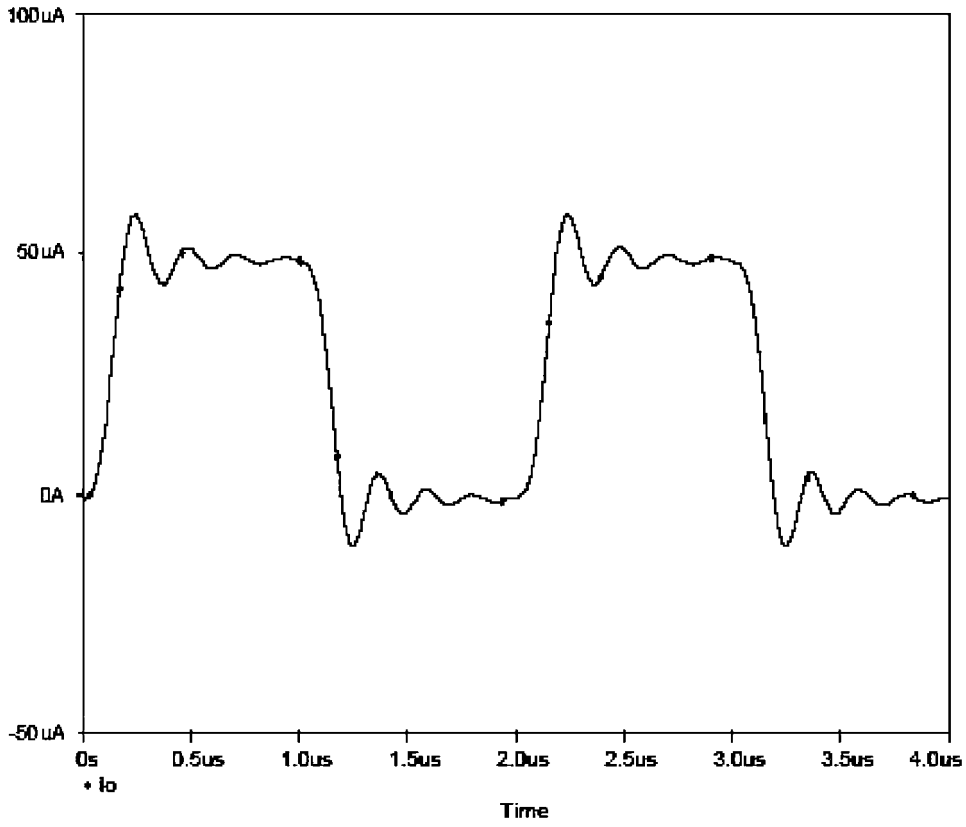

Fig. 10. Step response of the filter.

mimicking the voltages of the every node and currents of every branch in the passive filter. Fig. 8 shows seventh-order passive filter which is used to design the active filter in this paper. An approach, similar to the one in [7], is used to simulate the passive filter whereas here CDTA element with dual output is used in order to investigate the performance of the proposed CMOS circuit. To simulate the passive filter, transconductance of the CDTA element is used to transform

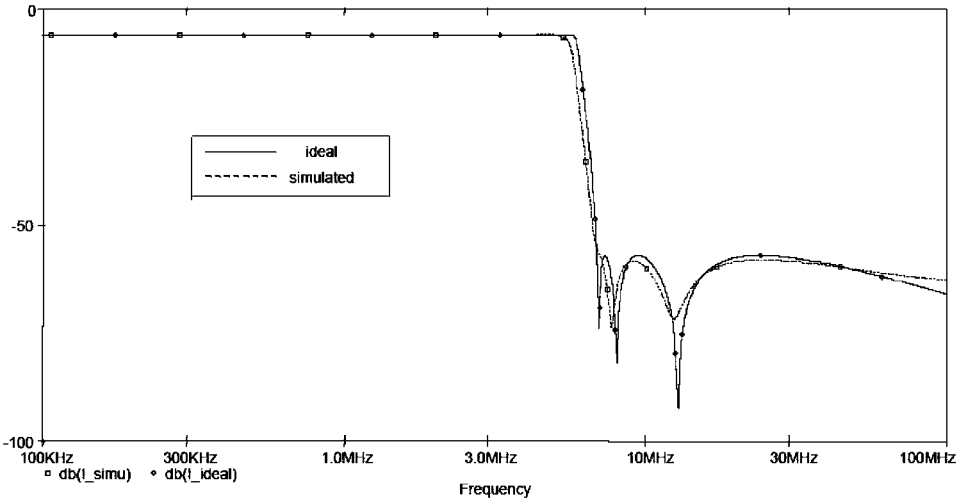

Fig. 11. Ideal and simulated filter responses.

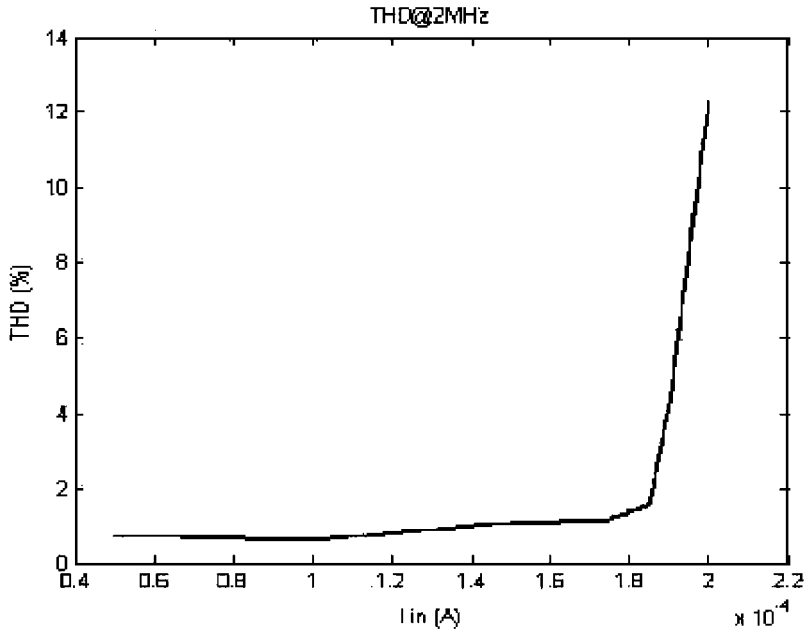

Fig. 12. Total harmonic distortion of the filter.

the voltages of each node to currents. So adding an arbitrary g to the both sides of the current voltage relationship of the passive filter does not effect circuit equations but let us to use CDTA as an active element.

Active filter employing CDTA is given in Fig. 9. CL1, CL2, and CL3 are used to simulate the inductors in the passive filter with CDTA elements and their values are determined to the following relations (4) which come from circuit equations (3). In obtaining circuit equations $C2$, $C4$ and $C6$ are not considered in the first step. Further information can be found in [7].

$$I_{l_i} = \frac{gV_i - gV_{i+1}}{gsL_i}, \quad i = 1, \ldots, 3,$$

$$gV_1 = g(I_{\text{in}} - I_{L_1})\frac{1}{sC_1 + G_1},$$

$$gV_{i+1} = g(I_{L_i} - I_{L_{i+1}})\frac{1}{sC_{2i+1}}, \quad i = 1, 2,$$

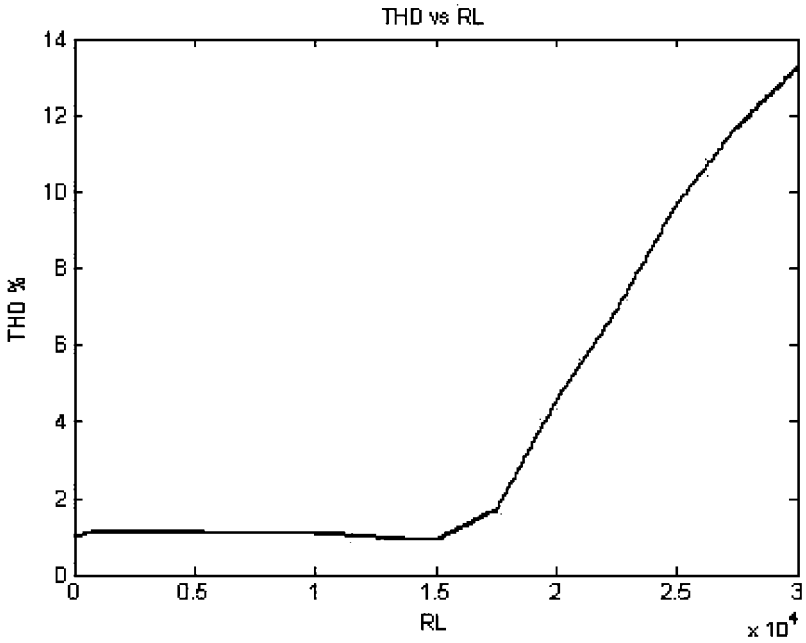

Fig. 13. Total harmonic distortion versus load resistance.

$$gV_4 = g(I_{L_3})\frac{1}{sC_7 + G_2}, \tag{3}$$

$$C_{L_i} = L_i g^2, \quad i = 1, \ldots, 3. \tag{4}$$

Group delay is also an important parameter for video filters. It must be a few nanoseconds for an anti-aliasing filter for properly working video applications. ITU BT 601 recommends it as 5 ns which cannot be achieved by anti-aliasing filters without using additional delay equalizers. Delay equalizers are implemented by all pass networks and five order all pass network will be sufficient for the video filter in this topology to meet the requirements recommended by ITU.

Seventh-order elliptic low-pass filter using CDTA as the active element is given in Fig. 9. Arbitrary g parameter in circuit equations (3), here, is used for the transconductance parameter of the CDTA elements. Passive filter element values are taken from a elliptic filter table [11]. Frequency is renormalized by the cut-off frequency of 5.75 MHz of the anti-aliasing filter and impedance renormalized.

SPICE simulations are carried out and resulting figure of the filter and ideal responses are given in the Fig. 11. As seen from the figure, simulated and ideal responses agree well. Small deviation from the ideal is caused by the parasitics of the CDTA element. Maximum ripple in the passband is found as 0.1 dB.

Filter step response is shown in Fig. 10. Ringing in the filter should be compensated if the filter is to be used for video applications since such a ringing is not tolerable for acceptable video quality. The reason of this ringing is the nonlinear phase response the filter. The solution is, as mentioned before, the usage of delay equalizers. Also, an additional gain stage should be used to get 0 dB gain for the anti-aliasing filter (Fig. 11).

Filter distortion is also investigated using SPICE program. It is found in Fig. 12 that for an input current signal less than 200 μA amplitude, filter THD value is no more than 2% at 2 MHz. Also in Fig. 13, for an input signal of 100 μA amplitude at 2 MHz, variation of the THD value versus output load resistance is shown. For a load resistance lower than 15 kΩ?, THD is low, less than 2%.

5. Conclusion

Compact, capable of high-frequency operation, CMOS CDTA structure is given and related simulation results are obtained. Seventh-order elliptic video anti-aliasing filter is designed using operational simulation of a passive filter and it is found that the theoretical and simulated responses agree well.

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