A new high speed and low power four-quadrant CMOS analog multiplier in current mode

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Current Mode Analog Circuit Design
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ABSTRACT

In [1], a new CMOS current-mode four-quadrant analog multiplier and divider circuit based on squarer circuit is proposed. The dual translinear loop is used as the basic building block. The major advantages of this multiplier are high speed, low power, high linearity and less dc offset error.
ABSTRACT

The simulation results of analog multiplier demonstrate a linearity error of 1.1%, a THD of 0.97% in 1MHz, a –3dB bandwidth of 41.8MHz and a maximum power consumption of 0.34mW.
INTRODUCTION

The four-quadrant multiplier has many applications in automatic gain controlling, phase locked loop, modulation, detection, frequency translation, square rooting of signals, neural networks, fuzzy integrated systems.
INTRODUCTION

Power consumption, linearity and the accuracy parameters are the key parameters in the design of high-performance mixed-signal integrated circuit.

Linearity, speed, supply voltage and power dissipation are the main goals of the design.
INTRODUCTION

Several techniques for reducing power consumption in CMOS analog multiplier circuits have recently been proposed[1]. They use floating gate MOS [2–4], bulk-driven MOS [5], subthreshold mode [6,7] or class-AB mode [8,9]. They suffer for not being highly precise and not having low power and high speed.
INTRODUCTION

In [1], a low-power, high-speed four-quadrant current mode analog multiplier circuit uses “dual translinear loops” is proposed. The circuit is based on the square-law characteristics of an MOS transistor operated in the saturation region. In addition, the dual translinear loops allow the design of the analog multiplier circuit, which exhibits wide bandwidth, high dynamic range and high speed[10,11].
CURRENT-MODE SQUARER CIRCUIT

The current mode squarer circuit is based on the dual translinear loop. This circuit is used to realize the multiplier circuit. The drain-to-source current ($I_{DS}$) of an MOS transistor operated in the saturation region is given by:

\[
I_{DS} = K(V_{GS} - V_t)^2
\]

\[
K = 0.5\mu_0C_{OX}(W/L)
\]

\[
v_{GS} = V_t + \sqrt{\frac{I_{DS}}{K}}
\]
\[ V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \]

\[ \sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \]

\[ 2\sqrt{I_B} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \]

\[ I_{DS3} = I_{out} + I_{in} \]

\[ I_{DS4} = I_{out} - I_{in} \]

\[ 4I_B = I_{in} + I_{out} + I_{out} - I_{in} + 2\sqrt{I_{out}^2 - I_{in}^2} \]

\[ 16I_B^2 - 16I_BI_{out} + 4I_{out}^2 = 4I_{out}^2 - 4I_{in}^2 \]

\[ I_{out} = \frac{I_{in}^2}{4I_B} + I_B \]
The principle of operation of the proposed multiplier is based on the square-difference identity:

\[ \lambda \times y = \tau(\lambda - y) - \tau(\lambda + y) \]
MULTIPLIER CIRCUIT

The multiplier is based on the squaring circuit which has two dual translinear loops. The first loop \((M_1-M_4)\) provides a \((X+Y)\) input to the squarer function, \((X+Y)^2\) and the second loop \((M_5-M_8)\) provides a \((X-Y)\) input to the squarer function, \((X-Y)^2\).
The analog multiplier circuit is simulated using HSPICE with level 49 model (BSIM3v3) of 0.35 µm CMOS technology, and the supply voltage is 3.3V.
SIMULATION RESULTS

![Graph showing simulation results with current axes and values]
SIMULATION RESULTS
THD

- 100 kHz @ Iy=10μA dc
- 1 MHz @ Iy=10μA dc
DIVIDER CIRCUIT

\[ I_{out} = \frac{I_X I_Y}{I_B} \]

By keeping the current \( I_X \) (or \( I_Y \)) constant, the output current of the multiplier circuit will be proportional to \( I_Y/I_B \) (or \( I_X/I_B \)) and the divider circuit can be obtained. However, care must be taken as \( I_B \) cannot be reduced below a minimum value in order to guarantee the proper biasing of the transistors.
DIVIDER CIRCUIT
ERROR DUE TO BODY EFFECT

In an MOS transistor, as the source-to-substrate voltage $V_{SB}$ increases, the threshold voltage $V_T$ will also increase. This is the "body effect", and can be characterized by:

$$V_t = V_{t0} + \gamma \left[ \sqrt{2\phi_b + |V_{SB}|} - \sqrt{2\phi_b} \right]$$

where $V_{t0}$ is the zero-bias threshold voltage, $\delta$ is the body effect coefficient and $\Phi_b$ is the bulk potential.
To avoid body effect, the cascaded MOS transistors are placed in separated wells, and $V_{SB}$ will be zero. Thus, these transistors will have zero-bias threshold voltage. In $M_2$ and $M_4$ transistors bulk is connected to the source, hence $V_{SB}=0$ and $V_t=V_{t0}$. 
ERROR DUE TO BODY EFFECT

But for $M_1$ and $M_3$, $V_{SB} \neq 0$. Considering this mismatch between $M_1$ and $M_3$ transistors we can write

$$V_{GS1} = V_{t1} + \Delta V_1$$

$$V_{t1} = V_t + \delta, \ V_{t3} = V_t - \delta,$$

$$V_{GS3} = V_{t3} + \Delta V_3$$

$$V_{t1} + \Delta V_1 + V_{GS2} = V_{t3} + \Delta V_3 + V_{GS4}$$

Where $\delta$ is the mismatch term between $V_{t1}$, $V_{t3}$. 

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ERROR DUE TO BODY EFFECT

\[ I_{DS1} = I_{DS2} = I_B, \quad I_{DS3} = I'_\text{out} + I_{\text{in}}. \]

\[ I_{DS4} = I'_\text{out} - I_{\text{in}} \]

\[ V_{t2} = V_{t4} (|V_{SB}| = 0) \]

\[ \delta + 2 \sqrt{\frac{I_B}{K}} = -\delta + \sqrt{\frac{I'_\text{out} + I_{\text{in}}}{K}} + \sqrt{\frac{I'_\text{out} - I_{\text{in}}}{K}} \]

\[ I'_{\text{out}} = \frac{I_{\text{in}}^2}{4I_B + 8\delta \sqrt{KI_B}} + \frac{I_B + 4\delta \sqrt{KI_B}}{1 + 2\delta \sqrt{K/I_B}} \]

Assuming \( I_B = K \Delta V^2 \)

\[ I'_{\text{out}} = \frac{I_{\text{in}}^2}{4K \Delta V (\Delta V + 2\delta)} + \frac{K \Delta V (\Delta V + 4\delta)}{1 + 2\delta / \Delta V} \]
ERROR DUE TO BODY EFFECT

It can be seen that the mismatch error between threshold voltages is dispensable. Because

\[ \Delta V \gg 4\delta \quad \Delta V \gg 2\delta \quad 1 \gg \frac{2\delta}{\Delta V} \]

\[ |I_{\text{error}}| = I_{\text{out}} - I'_{\text{out}} = \frac{I_{\text{in}}^2}{4K \Delta V^2} + K \Delta V^2 \]

\[ \cdot \left[ \frac{I_{\text{in}}^2}{4K \Delta V(\Delta V + 2\delta)} + \frac{K \Delta V(\Delta V + 4\delta)}{1 + 2\delta/\Delta V} \right] \]
ERROR DUE TO BODY EFFECT

\[ |I_{\text{error}}| = |I_{\text{out}} - I'_{\text{out}}| = \frac{I_{\text{in}}^2}{4K \Delta V^2} + K \Delta V^2 \]

\[ = \left[ \frac{I_{\text{in}}^2}{4K \Delta V(\Delta V + 2\delta)} + \frac{K \Delta V(\Delta V + 4\delta)}{1 + 2\delta/\Delta V} \right] \]

Ignoring terms containing \( \Delta V^n (n = 3, 4, 5), \delta^2 \)

\[ |I_{\text{error}}| = \frac{\delta}{2K \Delta V^2} I_{\text{in}}^2 + 4K \delta \Delta V^2 \]
ERROR DUE TO BODY EFFECT

The term $\Delta V^2$ shows very small error. The advantage of using the function $(X+Y)^2-(X-Y)^2$ in the multiplier circuit is to cancel the offset and body effect errors by eliminating the second term in $I'_{\text{OUT}}$.

\[
I'_{\text{out}} = \frac{I_{\text{in}}^2}{4I_B + 8\delta\sqrt{KI_B}} + \frac{I_B + 4\delta\sqrt{KI_B}}{1 + 2\delta\sqrt{K/I_B}}
\]

\[
I_{\text{out}} = \frac{I_X I_Y}{I_B + 2\delta K\Delta V}
\]
INPUT RANGE AND I/O RESISTANCE

The input current range of the multiplier is restricted by dual translinear loop, M₁-M₄ and M₅-M₈, operating in saturation region. If we assume that the MOS transistors M₁-M₄ operate in saturation region:

\[ \sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \]

\[ 2\sqrt{I_B} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \]

\[ 2\sqrt{I_B} \geq \sqrt{I_{out}} + I_{in} + \sqrt{I_{out} - I_{in}} \]
INPUT RANGE AND I/O RESISTANCE

Assuming $I_{in} = XI_B$ we obtain $X$ or namely maximum current value with which the multiplier circuit can work correctly.

\[ 2\sqrt{I_B} \geq \sqrt{I_{out} + I_{in}} + \sqrt{I_{out} - I_{in}} \]

\[ 2\sqrt{I_B} \geq \sqrt{\frac{X^2I_B^2}{4I_B}} + I_B + XI_B + \sqrt{\frac{X^2I_B^2}{4I_B}} + I_B - XI_B \]
INPUT RANGE AND I/O RESISTANCE

Squaring both sides and eliminating $I_B$ we obtain $X=0$, $X=\pm 2$, where $X=+2$ is acceptable: $I_{in}\leq 2I_B$.

In the multiplier circuit, maximum input current is: $I_{in_{\text{max}}} = I_X + I_Y$. Therefore $I_{in}$ will be maximum if

$$|I_X| = |I_Y| \leq |I_B|$$
INPUT RANGE AND I/O RESISTANCE

Assuming input ports are SUM and SUB, the input and output impedances are:

\[ R_{in\text{SUM}} = r_{ds7}(1 + g_{m7} \cdot r_{ds8}) || r_{ds10}(1 + g_{m10} \cdot r_{ds12}) \]

\[ R_{in\text{SUB}} = r_{ds1}(1 + g_{m1} \cdot r_{ds2}) || r_{ds9}(1 + g_{m9} \cdot r_{ds11}) \]

\[ R_{out} = r_{ds7}(1 + g_{m7} \cdot r_{ds8}) || r_{ds10}(1 + g_{m10} \cdot r_{ds12}) \]
A four-quadrant CMOS multiplier based on a new squaring circuit was proposed. The performance of the multiplier was simulated using HSPICE software. The advantages of the proposed analog multiplier circuit over previous circuits are given as high speed, high bandwidth and low-power consumption[1].
CONCLUSION

The multiplier can be used in analog VLSI circuit for low-power and high-speed applications such as IF variable gain amplifiers, adaptive filters, phase locked loops, neural networks and integrated fuzzy systems.
## CONCLUSION

<table>
<thead>
<tr>
<th></th>
<th>[2]</th>
<th>[4]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption (mW)</td>
<td>0.46</td>
<td>0.055</td>
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<td>Bias current (µA)</td>
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<td>THD (%) (1 MHz, 20 µA)</td>
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<td>1 (1KHz)</td>
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<td>Nonlinearity (%)</td>
<td>1.20</td>
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<td>−3dB bandwidth (MHz)</td>
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<td>Technology (µm)</td>
<td>0.5</td>
<td>0.35</td>
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References:


References:


Thanks...