ELE509E
Current-Mode Analog Circuit Design
Homework 4 (17.12.2004)

Design a CMOS CDBA (Current Differencing Buffered Amplifier) employing CCIIs. The DOCCII structure designed in a previous Homework can be used for realization. Try to simplify your CMOS structure by removing some unused terminals if possible.
Circuit symbol and equivalent circuit of the CDBA are shown in Figure 1. Definition equations of CDBA are given in Eq. 1. CCII-based realization of CDBA is illustrated in Figure 2.

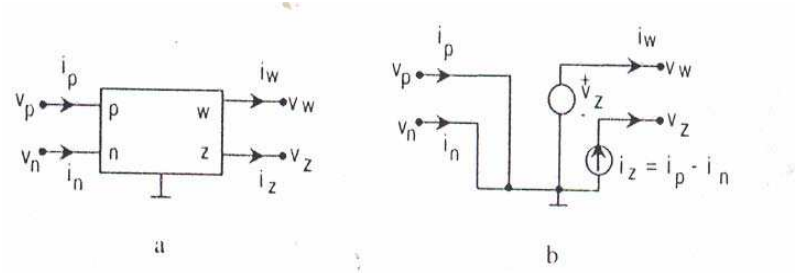

Figure 1. Circuit symbol of CDBA and equivalent circuit

$$\begin{bmatrix} i_z \\ v_w \\ v_p \\ v_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_z \\ i_w \\ i_p \\ i_n \end{bmatrix} \tag{1}$$

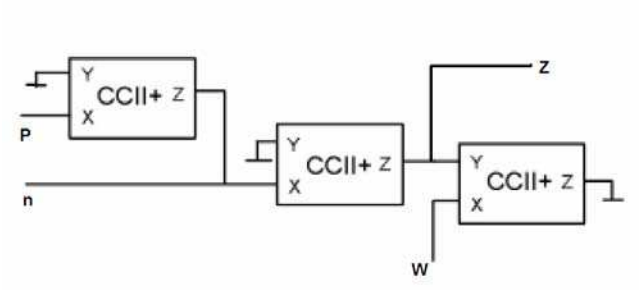

Figure 2. CCII based realization of CDBA

Using SPICE simulation program:

a- draw the the plot of I_Z against $\left(I_P - I_N\right)$. For this plot set one of the input currents equal to zero, than vary the other input current in operating range of your amplifier.

b- specify the limits of the operation region, the limits of the output currents.

c- Repeat (a) and (b) by applying input current to the other input terminal and setting the input current of the former active input equal to zero.
d- Plot the frequency response of the current gains and determine the bandwidth.
e- Plot the frequency response of terminal impedances.

Using the CMOS structure designed realize the filter topology shown in Figure 3.

f- Realize the filter circuit illustrated in Figure 3 employing the CMOS CDBA designed.
g- Choose passive element values to obtain a pole frequeny of 150 kHz.

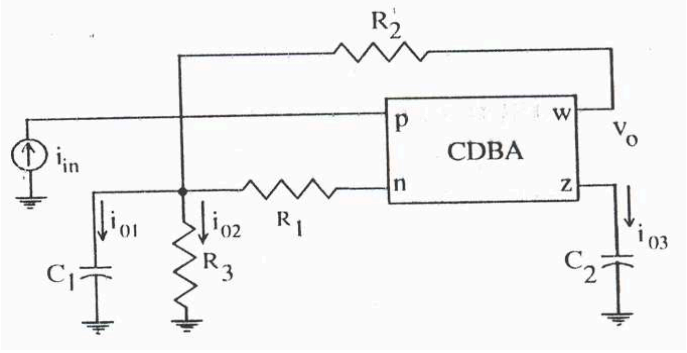

Figure 3

Using SPICE simulation program

h- Draw the plots of i_{o1}/i_{in}, i_{o2}/i_{in}, i_{o3}/i_{in} against frequency (ideal and actual responses together).

Investigate the large signal response of the filter (BP output).

i- Apply a sinusoidal input current in the passband to the input and observe the total harmonic distortion THD at the output for different input levels; draw the plot of THD against i_{out}. (Connect an adequate load resistance to the output terminal).
j- investigate the dependence of the output voltage upon the load resistance R_L keeping the input level constant at a low distortion level determined in f, observe the harmonic distortion THD at the output for each load resistance value; draw the plot of V_O against R_L.
k- Give a detailed evaluation of your results.

References

1) Özcan S., Kuntman H., Çiçekoğlu O., "Cascadable Current Mode Multipurpose Filters Employing CDBA". Int. J. Electron. Commun. (AEÜ) 56 (2002) No: 2 67-72
2) Acar C., Özoğuz S., "A new versatile building block: current differencing amplifier suitable for analog signal-processing filters". Microelectronics Journal 30 (1999) 157-160
3) I. Myderrizi, Cascadable Current Mode Multipurpose Filters Employing Current Differencing Amplifier (CDBA), Seminar Notes for ELE509E: Current-Mode Analog Circuit Design, Istanbul Technical University, 17. 12.2004.

Table 1. Transistor parameters of 0.5µm CMOS process

.MODEL NT NMOS LEVEL=3

+UO=460.5 TOX=1.0E-8 TPG=1 VTO=.62 JS=1.8E-6 XJ=.15E-6 RS=417 RSH=2.73

LD=0.04E-6 ETA=0 +VMAX=130E3 NSUB=1.71E17 PB=.761 PHI=0.905

THETA=0.129 GAMMA=0.69 KAPPA=0.1 AF=1 +WD=.11E-6 CJ=76.4E-5 MJ=0.357

CJSW=5.68E-10 MJSW=.302 CGSO=1.38E-10 CGDO=1.38E-10 +CGBO=3.45E-10

KF=3.07E-28 DELTA=0.42 NFS=1.2E11

.MODEL PT PMOS LEVEL=3

+UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6 XJ=0.1E-6 RS=886 RSH=1.81
LD=0.03E-6 ETA=0 +VMAX=113E3 NSUB=2.08E17 PB=.911 PHI=0.905
THETA=0.120 GAMMA=0.76 KAPPA=2 AF=1 +WD=.14E-6 CJ=85E-5 MJ=0.429
CJSW=4.67E-10 MJSW=.631 CGSO=1.38E-10 CGDO=1.38E-10 +CGBO=3.45E-10
KF=1.08E-29 DELTA=0.81 NFS=0.52E11