

# ELE509E

## Current-Mode Analog Circuit Design

### Homework 3 (21.11.2003)

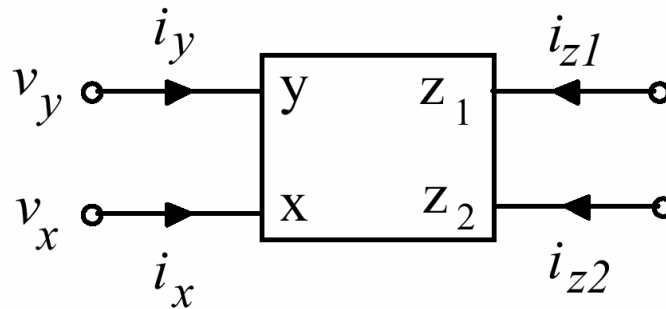


Figure 1. Circuit symbol of DOCCII.

A dual output current conveyor (DOCCII) is described by

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ k & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z1} \\ V_{Z2} \end{bmatrix}$$

$k = \pm 1$ . For  $k = 1$  a DOCCII with two noninverting Z outputs is obtained. For  $k = -1$  the  $Z_2$  terminal yields an inverted output signal.

Design a CMOS dual output current conveyor with inverting and noninverting outputs..

1. Terminal output resistances  $R_{Z1}, R_{Z2}, R_Y > 25 \text{ M}\Omega$ ,  $R_X < 10 \Omega$ .
2. Voltage tracking error  $\epsilon_V < 0.1\%$ , current tracking error  $\epsilon_I < 0.1\%$ ,
3. BW of the voltage gain ( $A_V = v_x/v_y$ )  $f_{V3db} > 10 \text{ MHz}$ ,
4. BW of the current gain ( $A_{I1} = i_{z1}/i_x$ ,  $A_{I2} = i_{z2}/i_x$ )  $f_{I3db} > 50 \text{ MHz}$ ,

The supply voltages are given as  $V_{DD} = 2.5\text{V}$ ,  $-V_{SS} = -2.5\text{V}$ . The model parameters of the MOS transistors are given in Table 1.

a - Specify the CMOS DOCCII structure, determine transistor dimensions.

Using SPICE simulation results

- a) draw the the plots of  $V_X$  against  $V_Y$ ,  $I_{Z1}$  and  $I_{Z2}$  against  $I_X$ ,
- b) specify the limits of the operation region,

- c) draw the frequency response of the voltage gain and determine the bandwidth,
- d) draw the frequency response of the current gain and determine the bandwidth,
- e) draw the plot of the terminal impedances against the frequency,
- f) investigate the large signal behaviour of the DOCCII by applying to Y terminal a sinusoidal input voltage in the passband and observing the total harmonic distortion THD at the X, Z1 and Z2 terminals for different input levels; draw the plot of THD against  $i_{in}$  for each terminal. (Connect adequate load resistances to the X, Z1 and Z2 terminals.
- g) Give a detailed evaluation of your results.

**Table 1. Transistor parameters of 0.5 $\mu$ m CMOS process**

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.MODEL NT NMOS LEVEL=3
+UO=460.5 TOX=1.0E-8 TPG=1 VTO=.62 JS=1.8E-6 XJ=.15E-6 RS=417 RSH=2.73
LD=0.04E-6 ETA=0 +VMAX=130E3 NSUB=1.71E17 PB=.761 PHI=0.905
THETA=0.129 GAMMA=0.69 KAPPA=0.1 AF=1 +WD=.11E-6 CJ=76.4E-5 MJ=0.357
CJSW=5.68E-10 MJSW=.302 CGSO=1.38E-10 CGDO=1.38E-10 +CGBO=3.45E-10
KF=3.07E-28 DELTA=0.42 NFS=1.2E11

.MODEL PT PMOS LEVEL=3
+UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6 XJ=0.1E-6 RS=886 RSH=1.81
LD=0.03E-6 ETA=0 +VMAX=113E3 NSUB=2.08E17 PB=.911 PHI=0.905
THETA=0.120 GAMMA=0.76 KAPPA=2 AF=1 +WD=.14E-6 CJ=85E-5 MJ=0.429
CJSW=4.67E-10 MJSW=.631 CGSO=1.38E-10 CGDO=1.38E-10 +CGBO=3.45E-10
KF=1.08E-29 DELTA=0.81 NFS=0.52E11
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