3.1 Distance Cell (DCELL)

As mentioned earlier, a Vector Quantizer (VQ) system chooses the closest template-vector to the input vector within the previously determined set of template-vectors. To determine the closest one, we must measure the distances between template and input vectors. Total distance between two vectors can be calculated as a sum of the distances between their vector elements. Thus first, I will measure the distance between the vector elements and then I will add them all. I name the block that measures the distance between the vector elements "Distance Cell" (DCELL). The function realized by DCELL must satisfy the following properties:

1. DCELL must produce the same output for input vector elements that are equidistant to the template-vector element. Thus, the function must be even symmetric.

$$f_{dcell}(x) = f_{dcell}(-x) \qquad 3.1$$

2. Output must be a monotonously increasing function of the distance between input and template-vector elements. Thus, the derivative of the function can change its sign only one single time at the symmetry point **T**.

$$\operatorname{sgn}\left[\left.\frac{df_{dcell}(x_1 - T)}{dx_1}\right|_{x_1<T}\right]\operatorname{sgn}\left[\left.\frac{df_{dcell}(x_2 - T)}{dx_2}\right|_{X_2<T}\right] = 1$$

$$\operatorname{sgn}\left[\left.\frac{df_{dcell}(x_3 - T)}{dx_3}\right|_{x_3>T}\right]\operatorname{sgn}\left[\left.\frac{df_{dcell}(x_4 - T)}{dx_4}\right|_{x_4>T}\right] = 1 \qquad 3.2$$

$$\operatorname{sgn}\left[\left.\frac{df_{dcell}(x - T)}{dx}\right|_{x\le T^-}\right]\operatorname{sgn}\left[\left.\frac{df_{dcell}(x - T)}{dx}\right|_{x\ge T^+}\right] = -1$$

In (3.2) and (3.1), **x** represents an input vector element. **T** represents a template-vector element. Finally, $\mathbf{f_{dcell}}$ represents the function realized by DCELL. Many different functions satisfy the above-mentioned conditions. Each of them defines

different distance metric. For example, the Euclidean distance between two one-dimensional vectors is

$$f_{dcell}(x,T) = \sqrt{(x-T)^2} = |x-T| = abs(x-T) \qquad 3.3$$

In Figure 3.1, we see the plot of (3.3) with three different template (**T**) values. (3.3) satisfies all of the conditions in (3.1) and (3.2). Another distance function can be

$$f_{dcell}(x,T) = (x-T)^2 \qquad 3.4$$

In Figure 3.2, we see the plot of (3.4) with three different template (**T**) values. (3.4) satisfies all of the conditions in (3.1) and (3.2) .

For different realization of the DCELL, please refer to the following references in the literature. [8-18]

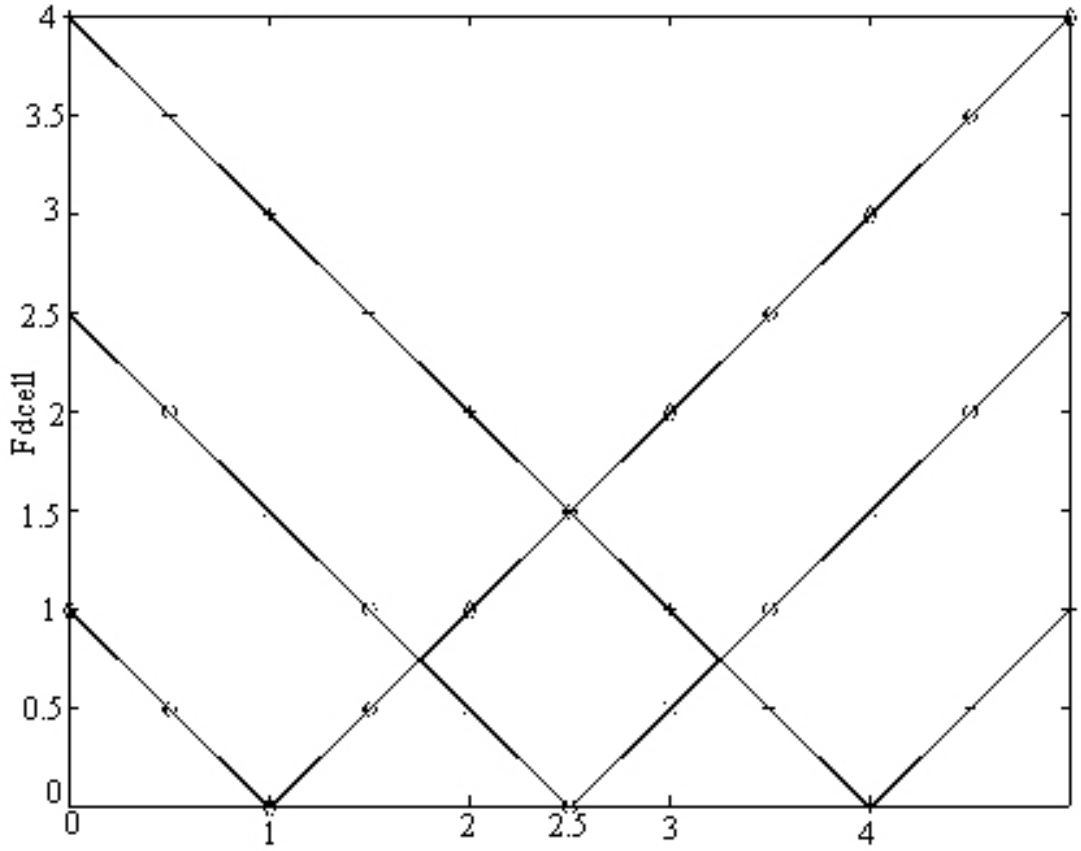

Figure 3.1 : Plot of (3.3) with T = 1(diamond), 2.5(circle), 4(plus)

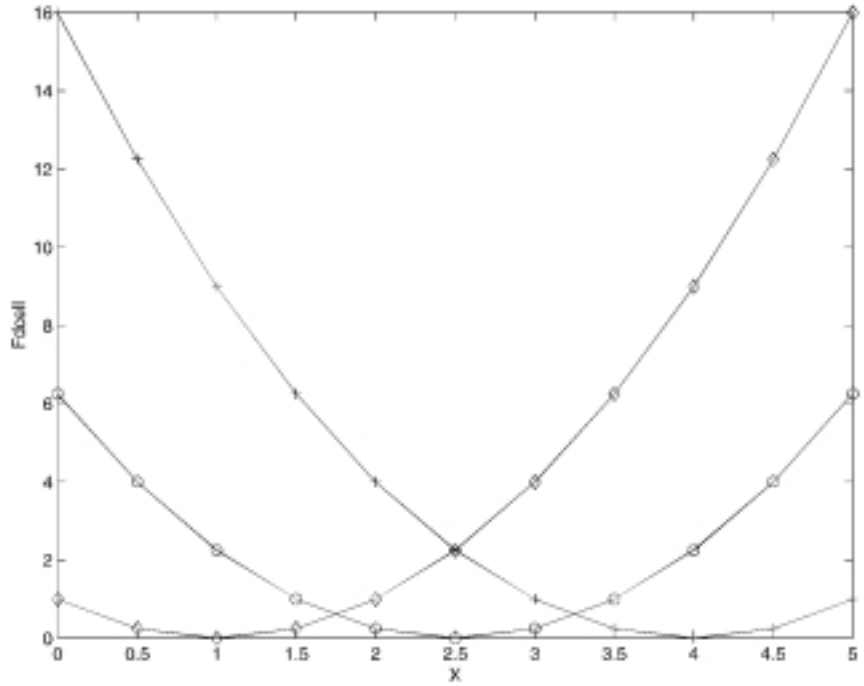

Figure 3.2 : Plot of (3.4) with T = 1(diamond), 2.5(circle), 4(plus)

In this work, we will examine in detail the DCELL proposed by ÇİLİNGİROĞLU and AKSIN in [18]. With its features high speed, small area, high modularity, simplicity, suitability to Low-Power Low-Voltage (LP-LV) applications, this DCELL is a very attractive one. This is a generic cell, it can be utilized in every analog block where we need to measure a distance.

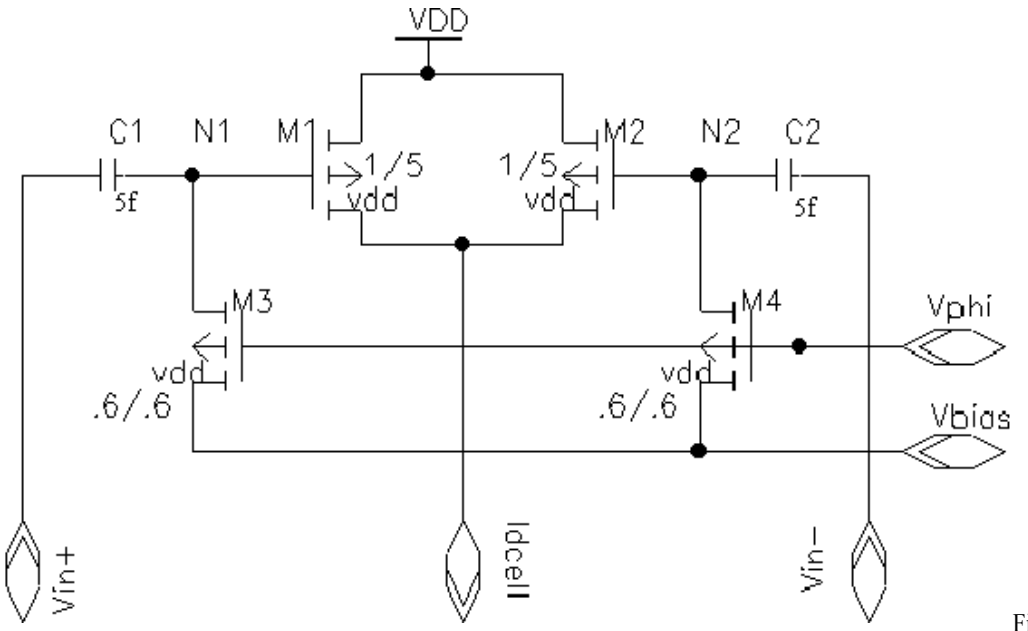

Figure 3.3 : CMOS schematic of DCELL

In Figure 3.3, we see the schematic view of the DCELL. Current-voltage transfer function of two PMOS transistors (M1, M2) biased into saturation region is utilized to realize the $\mathbf{f_{dcell}}$ function. Conditions for biasing M1 and M2 into saturation region are:

$$V_{DS(1,2)} < V_{GS(1,2)} - V_{TP} \qquad V_{TP} < 0$$

$$\begin{aligned} V_{DS(1,2)} &= V_O - V_{DD} \\ V_{GS(1,2)} &= V_{N(1,2)} - V_{DD} \\ V_O - V_{DD} &< V_{N(1,2)} - V_{DD} - V_{TP} \end{aligned} \qquad 3.5$$

$$V_O < V_{N(1,2)} - V_{TP}$$

V_{TP} represents the threshold voltage of PMOS transistors. $V_{N(1,2)}$ represents the voltage on node N1 or N2. Under the conditions given in (3.5), output voltage of the DCELL is set to a constant value below the minimum voltage that difference between $V_{N(1,2)}$ and V_{TP} can reach. Drain and source voltages of transistors M1 and M2 are constant. Thus, drain and source parasitic junction capacitances will not charge or discharge. This is the reason why the DCELL is suitable for high-speed applications. Another advantage of this structure is that as the drain voltage is constant, there is no channel length modulation. Under the conditions (3.5), the current-voltage transfer function of transistors M1 and M2 is:

$$V_{TP} < 0$$

$$I_{D(1,2)} = \begin{cases} 0 & V_{GS(1,2)} > V_{TP} \\ \frac{\beta}{2}\left(V_{GS(1,2)} - V_{TP}\right)^2 & V_{GS(1,2)} < V_{TP} \end{cases} \qquad 3.6$$

The current-voltage transfer function of a transistor biased in saturation region can be seen in Figure 3.4. Power consumption of the DCELL is highly influenced by aspect ratios (β) of transistors M1 and M2. We can summarize the operation principle of the DCELL as follows:

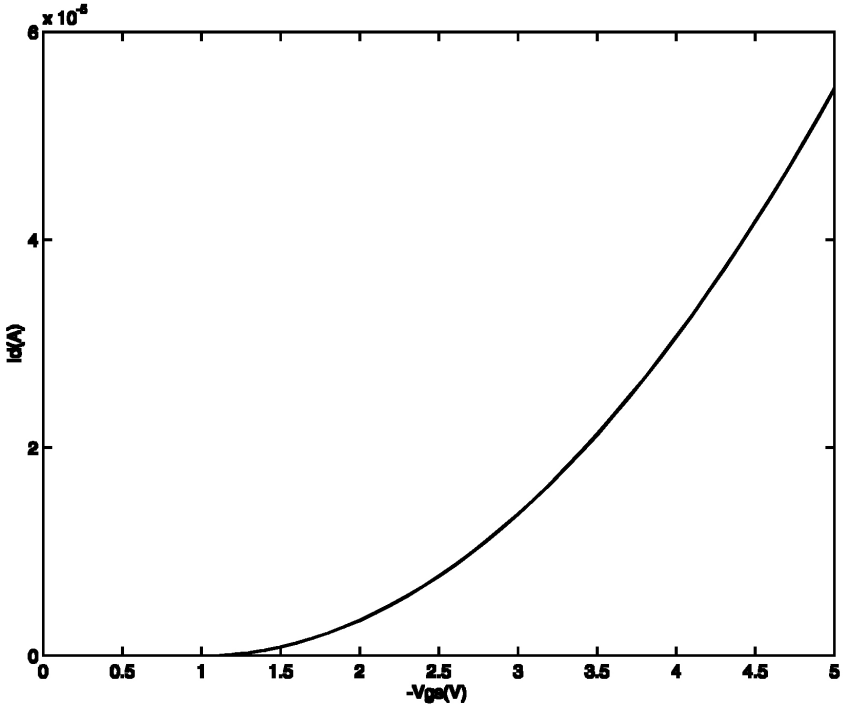

Figure 3.4 : Plot of (3.6) with V_{TP}= -1 V (W/L) = 1/5, KP = 34.12e-6 A/V^2

During the first phase (template writing phase), control voltage, V_Φ, is set to 0 V. Switch transistors M3 and M4 are conducting (on). Thus, voltages on nodes N1 and N2 are equal to V_{bias}. The bias voltage V_{bias} determines the minimum output current of the DCELL, which occurs when the input vector element is equal to template-vector element. During the same time interval, we apply voltage **T** (template) and (V_{DD}-**T**) on terminals V_{in+} and V_{in-} respectively. I will show later that the value of V_{DD} has no impact on the operation. During the second phase (operation phase), V_Φ is set to 5V; thus M3 and M4 switch transistors are in cut-off region. Nodes N1 and N2 are isolated and we conserve an amount of charge proportional to **T** and (V_{DD}-**T**) on these nodes. Then, when we apply input **x** on terminal V_{in+} and V_{DD}-**x** on terminal V_{in-}, the DCELL output current varies with respect to (3.7).

$$I_O = K(x - T)^2 \qquad 3.7$$

In (3.7), K represents a constant determined by the circuit, **x** represents the input voltage and **T** represents the template voltage. Template voltage T is stored dynamically on nodes N1 and N2. This creates two constraints for system level design. First one is the refresh requirement due to the leakage currents. Second one is

that in order conserve the stored charge during the operation, the pn junction between the bulk and the source of transistors M3 and M4 (junctions on node N1 and N2) must never be forward biased. Let me now prove the validity of (3.7) analytically. In Figure 3.5, we see the schematic view of the circuit IN_AMP that produces the signals V_{in+} and V_{in-}.

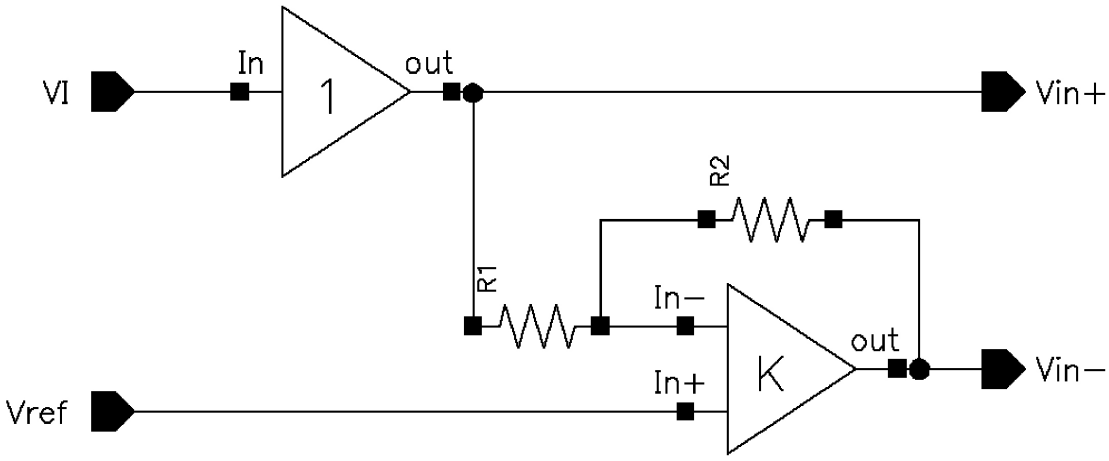

Figure 3.5 : Circuit schematic of IN_AMP

Under the conditions

K>>1, $R_1=R_2$ and $V_{REF}=\frac{V_{DD}}{2}$

We can model V_{in+} and V_{in-} signals as follows

$$\begin{aligned} V_{in+} &= V_I + \Delta V_{B1} \\ V_{in-} &= V_{DD} - V_I - \underbrace{\Delta V_{B1} + \Delta V_{b2}}_{\Delta V_{B2}} \\ &= V_{DD} + \Delta V_{B2} - V_I \end{aligned} \qquad 3.8$$

In (3.8), ΔV_{B1} and ΔV_{b2} are the offset errors of amplifiers.

First Phase (template writing phase):

V_ϕ=0 V (M_3 and M_4 are conducting)

$$
\begin{aligned}
V_1 &= T_{ij} \quad (\text{template voltage}) \\
V_{in+} &= T_{ij} + \Delta V_{B1} \\
V_{in-} &= V_{DD} + \Delta V_{B2} - T_{ij} \\
V_{N1} &= V_{N2} = V_{bias}
\end{aligned}
\qquad 3.9
$$

Charge stored on node N1 is

$$C_1\left(V_{bias} - T_{ij} - \Delta V_{B1}\right) + C_{T1}V_{bias} + \Delta Q_3 = Q_{N1} \qquad 3.10$$

In (3.10), C_{T1} represents all capacitances on node N1 with the exception of C_1; ΔQ_3 represents the channel charge of transistor M3, which is injected to node N1 at the moment transistor turn off. As M3 is a PMOS transistor, ΔQ_3 must have a positive sign. Similar equation for node N2

$$C_2\left(V_{bias} + T_{ij} - V_{DD} - \Delta V_{B2}\right) + C_{T2}V_{bias} + \Delta Q_4 = Q_{N2} \qquad 3.11$$

Second phase (operation phase):

V_ϕ=5 V (M_3 and M_4 are in cut-off region)

$$
\begin{aligned}
V_1 &= X_j \,(\text{input voltage}) \\
V_{in+} &= X_j + \Delta V_{B1} \\
V_{in-} &= V_{DD} + \Delta V_{B2} - X_j
\end{aligned}
\qquad 3.12
$$

Since the charge stored on node N1 is conserved, we can write

$$C_1\left(V_{N1} - X_j - \Delta V_{B1}\right) + C_{T1}V_{N1} = C_1\left(V_{bias} - T_{ij} - \Delta V_{B1}\right) + C_{T1}V_{bias} + \Delta Q_3$$

$$C_1\left(X_j + \Delta V_{B1} - T_{ij} - \Delta V_{B1}\right) + \left(C_1 + C_{T1}\right)V_{bias} + \Delta Q_3 = \left(C_1 + C_{T1}\right)V_{N1} \qquad 3.13$$

$$V_{N1} = V_{bias} + \frac{\Delta Q_3}{C_1 + C_{T1}} + \frac{C_1}{C_1 + C_{T1}}\left(X_j - T_{ij}\right)$$

For node N2

$$C_2\left(V_{N2}+X_j-V_{DD}-\Delta V_{B2}\right)+C_{T2}V_{N2}=C_2\left(V_{bias}+T_{ij}-V_{DD}-\Delta V_{B2}\right)+C_{T2}V_{bias}+\Delta Q_4$$

$$C_2\left(T_{ij}-V_{DD}-\Delta V_{B2}-X_j+V_{DD}+\Delta V_{B2}\right)+\left(C_2+C_{T2}\right)V_{bias}+\Delta Q_4=\left(C_2+C_{T2}\right)V_{N2}$$

$$V_{N2}=V_{bias}+\frac{\Delta Q_4}{C_2+C_{T2}}+\frac{C_2}{C_2+C_{T2}}\left(T_{ij}-X_j\right) \qquad 3.14$$

When we examine (3.13) and (3.14), we can note that

a) Node voltages V_{N1} and V_{N2} are independent of IN_AMP offset error.

b) With respect to the rule mentioned in (a), the value of V_{DD} has no influence on V_{N2}.

c) Charge injection creates an extra term that is added to others. Under the condition $\Delta Q_3=\Delta Q_4$, its influence can be cancelled by simply changing the bias voltage V_{bias}. Alternatively, it can be minimized by increasing total capacitance on these nodes. However, this will cause more silicon consumption.

Now we can draw some conclusions for the design of the transistors M3 and M4. To minimize charge injection effect, channel area of these transistors must be minimal. Moreover, to minimize leakage current, source diffusion area of M3 and M4 must be minimal too. Let us now calculate the DCELL's output current during the second phase. Transistors M1 and M2 operate in saturation region. The drain current of transistor M1 can be expressed as follows:

$$V_{N1}-V_{DD}<V_{TP(M1)} \qquad V_{TP(M1)}<0$$

$$I_{D(M1)}=\frac{\beta_1}{2}\left(V_{N1}-V_{DD}-V_{TP(M1)}\right)^2 \qquad 3.15.a$$

$$=\frac{\beta_1}{2}\left[V_{bias}+\frac{\Delta Q_3}{C_1+C_{T1}}+\frac{C_1}{C_1+C_{T1}}\left(X_j-T_{ij}\right)-V_{DD}-V_{TP(M1)}\right]^2$$

and the drain current of the transistor M2 is

$$V_{N2} - V_{DD} < V_{TP(M2)} \quad V_{TP(M2)} < 0$$

$$I_{D(M2)} = \frac{\beta_2}{2}\left(V_{N2} - V_{DD} - V_{TP(M2)}\right)^2 \qquad 3.15.b$$

$$= \frac{\beta_2}{2}\left[V_{bias} + \frac{\Delta Q_4}{C_2 + C_{T2}} + \frac{C_2}{C_2 + C_{T2}}\left(T_{ij} - X_j\right) - V_{DD} - V_{TP(M2)}\right]^2$$

We assume that

$$C_1 = C_2 = C \qquad \Delta Q_3 = \Delta Q_4 = Q \qquad \beta_1 = \beta_2 = \beta \qquad \frac{C}{C + C_T}\left(X_j - T_{ij}\right) = \Delta V$$

$$C_{T1} = C_{T2} = C_T \qquad V_{TP(M1)} = V_{TP(M2)} = V_{TP} \qquad V_{bias} + \frac{Q}{C + C_T} = V_B$$

Under these conditions, (3.15.a) becomes

$$I_{D(M1)} = \begin{cases} \frac{\beta}{2}\left(V_B + \Delta V - V_{DD} - V_{TP}\right)^2 & V_B + \Delta V - V_{DD} < V_{TP} \\ 0 & V_B + \Delta V - V_{DD} > V_{TP} \end{cases} \qquad 3.16.a$$

and (3.15.b) becomes

$$I_{D(M2)} = \begin{cases} \frac{\beta}{2}\left(V_B - \Delta V - V_{DD} - V_{TP}\right)^2 & V_B - \Delta V - V_{DD} < V_{TP} \\ 0 & V_B - \Delta V - V_{DD} > V_{TP} \end{cases} \qquad 3.16.b$$

For Class B operation, V_B is chosen as

$$V_B = V_{DD} + V_{TP} \qquad 3.17$$

We substitute (3.17) in (3.16.a)

$$V_B + \Delta V - V_{DD} < V_{TP} \Rightarrow \Delta V < 0$$

$$I_{D(M1)} = \begin{cases} \frac{\beta}{2}\left(\Delta V\right)^2 & \Delta V < 0 \\ 0 & \Delta V > 0 \end{cases}$$

Respectively (3.17) in (3.16.b)

$$V_B - \Delta V - V_{DD} < V_{TP} \Rightarrow \Delta V > 0$$

$$I_{D(M2)} = \begin{cases} \frac{\beta}{2}(-\Delta V)^2 & \Delta V > 0 \\ 0 & \Delta V < 0 \end{cases}$$

Thus, the DCELL's output current can be expressed as

$$\begin{aligned} I_{DCELL} &= I_{D(M1)} + I_{D(M2)} \\ &= \frac{\beta}{2}(\Delta V)^2 + 0 && \Delta V < 0 \\ &= 0 + \frac{\beta}{2}(-\Delta V)^2 && \Delta V > 0 \end{aligned}$$

$$I_{DCELL} = \frac{\beta}{2}(\Delta V)^2 = \frac{\beta}{2}\left(\frac{C}{C + C_T}\right)^2 (X_j - T_{ij})^2 \qquad \forall \Delta V \qquad 3.18$$

Same calculation for Class A operation

$$V_{bias} < V_{DD} + V_{TP} - \frac{C}{C + C_T}\left|X_j - T_{ij}\right|_{max} + \frac{Q}{C + C_T} \qquad 3.19$$

We substitute (3.19) in (3.16a) and (3.16.b). Then we add them to calculate output current.

$$\begin{aligned} I_{DCELL} = \frac{\beta}{2}\Bigg[& \left(V_{bias} + \frac{Q}{C + C_T} + \frac{C}{C + C_T}(X_j - T_{ij}) - V_{DD} - V_{TP} \right)^2 \\ & + \left(V_{bias} + \frac{Q}{C + C_T} + \frac{C}{C + C_T}(T_{ij} - X_j) - V_{DD} - V_{TP} \right)^2 \Bigg] \end{aligned}$$

Previous equation can be arranged as follows:

$$I_{DCELL} = \frac{\beta}{2}\left(V_{bias} + \frac{Q}{C + C_T} - V_{DD} - V_{TP} \right)^2 + \frac{\beta}{2}\left(\frac{C}{C + C_T}\right)^2 (X_j - T_{ij})^2 \qquad 3.20$$

If we compare (3.20) with (3.18), we can note that in case of Class A operation, we simply add a DC current term to (3.18). For classifier networks like vector quantizer,

this kind of DC current has no influence on classification process if it has the same value for each distance cell. However, DC current in (3.20) can differ for each DCELL due to the fabrication process noise. Another undesirable effect of the DC current is the increase of power consumption.

Due to process noise, threshold voltages of transistors M1 and M2 will differ from their mean value V_{TP}. For that reason, transistor M1 or M2 may enter cut-off region before input voltage and template voltages are equal. This situation creates a dead zone. To prevent the dead zone caused by process noise in Class B operation, it is more suitable to use DCELL in Class AB operation. For class B and AB operation, when difference between input and template voltage (X - T) goes to zero, M1 and M2 transistors start to operate in weak-inversion region. In this case, we can express the cell's output current as follows [19-23]

Input voltage goes to template voltage level, $X_j \rightarrow T_{ij}$ and $V_{bias} = V_{DD} + V_{TP}$, Thus, gate-source voltage $V_{GS(1,2)}$ of transistors M1 and M2 are

$$V_{GS(1,2)} = V_{bias} \mp \frac{C}{C + C_T}\left(X_j - T_{ij}\right) - V_{DD} \rightarrow V_{bias} - V_{DD} = \Delta V$$

$$\Delta V \rightarrow V_{TP}$$

Transistors M1 and M2 operate in weak-inversion region. Drain current of a transistor biased in weak-inversion can be expressed as follows:

$$I_{D(M1)} = I_{D(M2)} = \left(\frac{w}{l}\right)_{M1} I_{D0}\, e^{-V_{BS}\left[\left(\frac{1}{nV_T}\right)-\left(\frac{1}{V_T}\right)\right]}\left(1 - e^{-V_{DS}/V_T}\right) e^{\frac{V_{GS}-V_{TP}}{nV_T}}$$

$V_{BS} = 0$ V, $V_T = 25$ mV at room temperature, $V_T << V_{DS}$ and $1<n<2$. Thus

$$I_{D(M1)} = I_{D(M2)} = \left(\frac{w}{l}\right) I_{D0}\, e^{\frac{V_{GS}-V_{TP}}{nV_T}}$$

$$I_{D0} = \frac{2\mu Cox\left(nV_T^2\right)}{e^2}$$

$$I_{DCELL} = \frac{4w}{l}\frac{\mu Cox\left(nV_T^2\right)}{e^2}\exp((\Delta V - V_{TP})/nV_T) \qquad 3.21$$

Simulation schematic of DCELL can be seen in Figure 3.6.

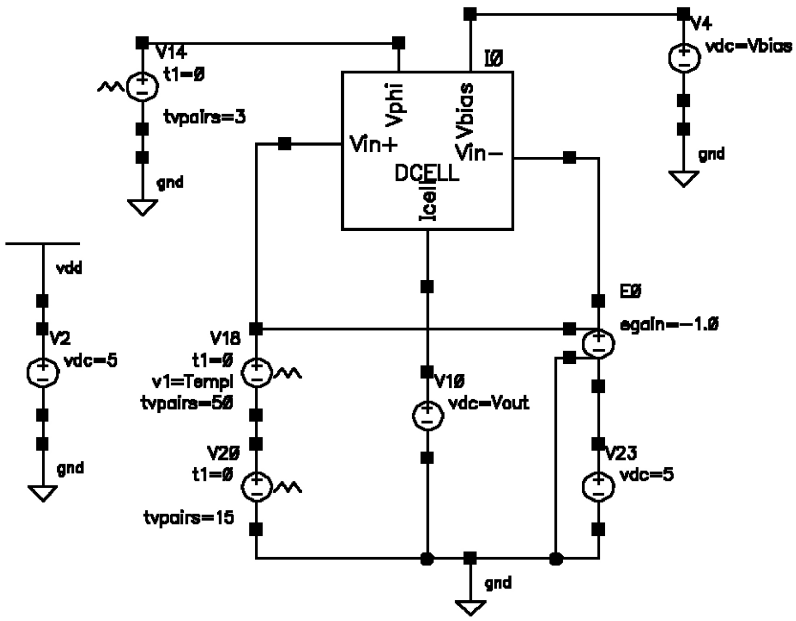

Figure 3.6 : Simulation Schematic of DCELL

Variation of DCELL output current for 4 different V_{bias} voltage can be seen in Figure 3.7. Dead zone is created for the bias voltage level V_{bias} = 4.1 V. Variation of DCELL output current for 3 different template voltage can be seen in Figure 3.8.

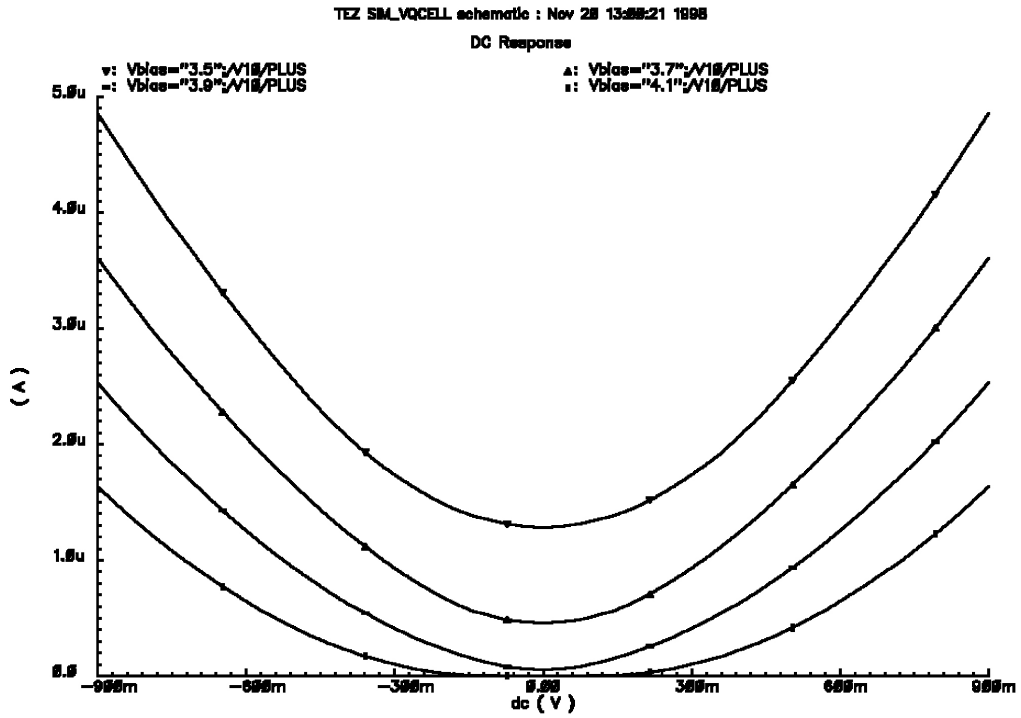

Figure 3.7 : Variation of DCELL output current for Vbias= 3.5V, 3.7V, 3.9V, 4.1V

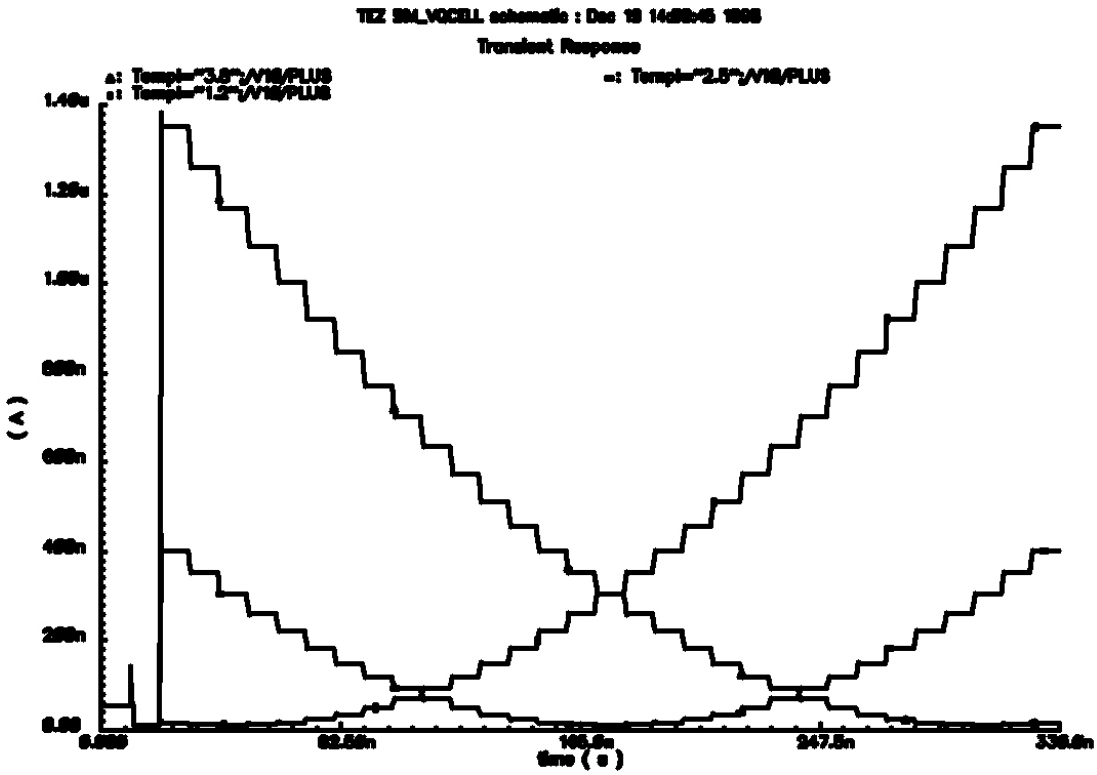

Figure 3.8 : Variation of DCELL output current for template voltage T=1.2V, 2.5V, 3.8V

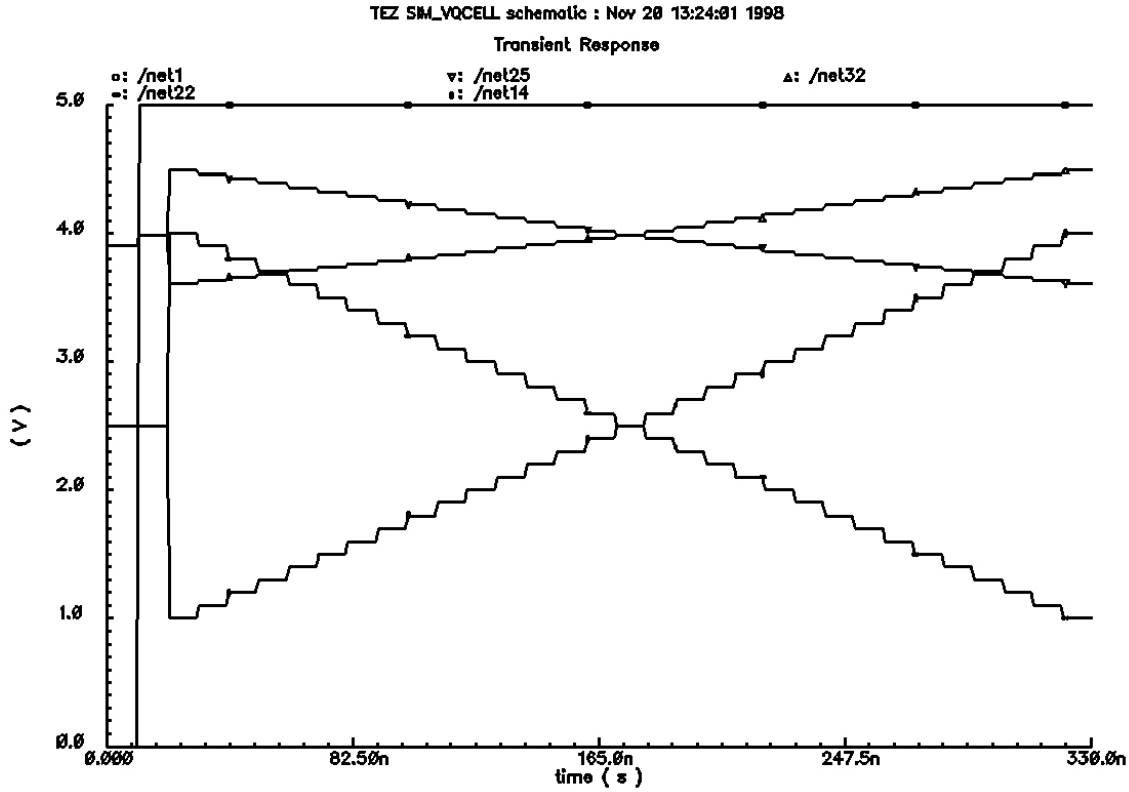

Figure 3.9 : Variation of input signals for Template Voltage T equal to 2.5V

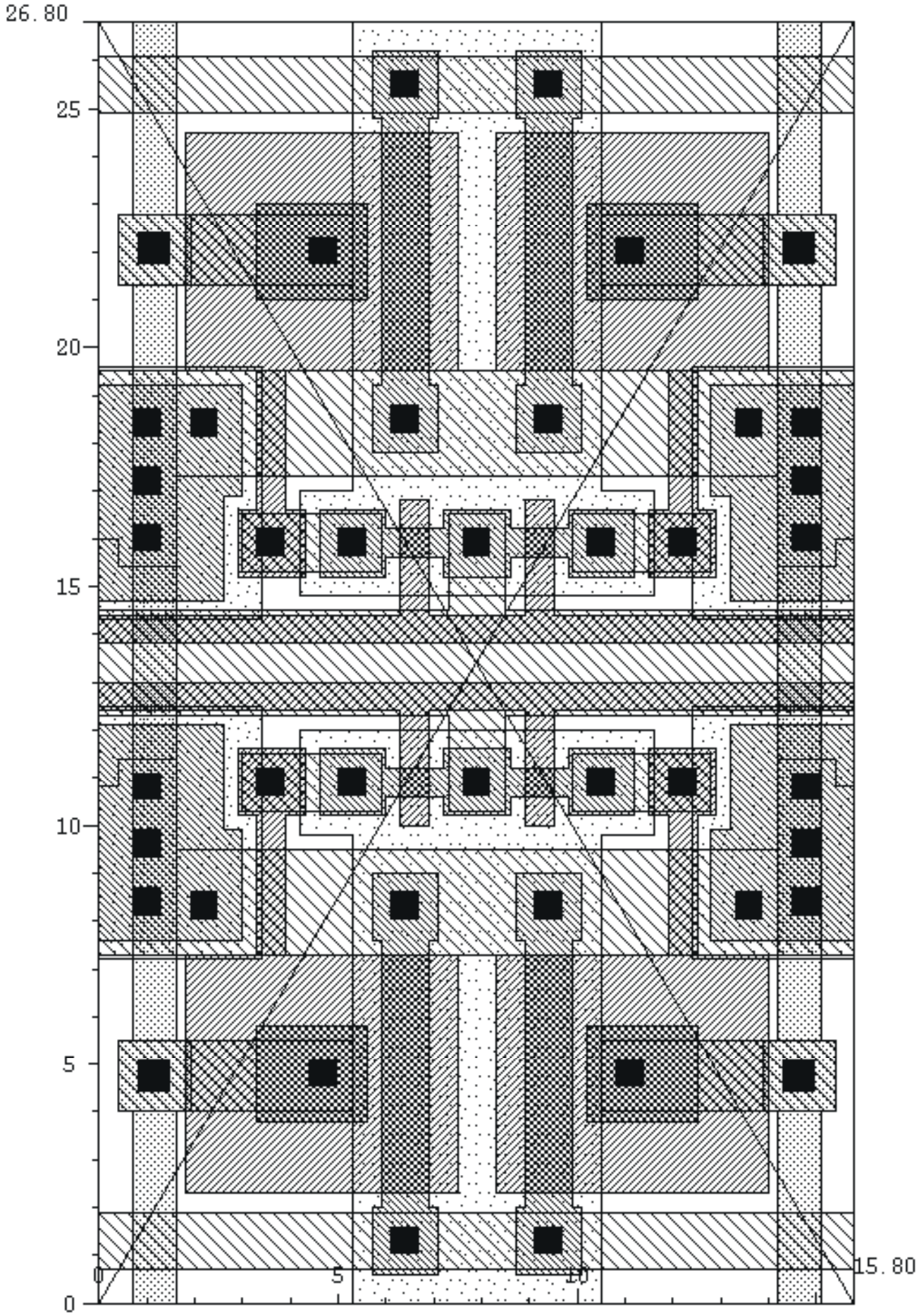

Figure 3.10 : Layout of DCELL

Variation of input signals during the transient simulation in Figure 3.8 can be seen in Figure 3.9. Template voltage is set to 2.5V. /net14 represents signal V_{IN+}, /net22 represents signal V_{IN-}, /net32 represents signal on node N1 and /net25 represents signal on node N2. As we can see in Figure 3.9, control signal V_Φ (/net1) is 0V during first 10ns. Thus, transistors M3 and M4 conduct (First phase). At t=10ns, V_Φ is 5V (second phase). We can easily remark the effect of charge injection at t=10ns in Figure 3.8. The output current reaches its maximum value when the difference $|x - T|$ is maximal. Obviously, the power consumption of the block is a function of the template voltage written on. The output current, the power consumption, is minimal when the template voltage is equal to the middle of the input signal range. The variation of the voltages on node N1 and N2 is within the range [4.868V, 3.299V].

Layout of DCELL for AMS 0.6µm double-poly, double-metal CUQ process can be seen in Figure 3.10. The extracted view of this layout was used for all simulations of DCELL. Modularity and small area are primary design considerations. Poly1-Poly2 capacitance is used as input capacitor. M3 and M4 transistor's gate voltages are driven by poly wire path. I will simulate later the effect of poly layer's serial resistance on switching characteristics. There are 2 DCELLs in Figure 3.10. The width of layout is 15.8µm and the height of layout is 26.8µm. The total silicon area consumption of 1 DCELL block is 2.1172e-4mm^2. Thus in 1mm^2, we can place 4723 DCELL block. The list of sizes of the transistors and the input capacitors of the block can be seen in Table 3.1.

Table 3.1 : The List of the transistors and capacitors sizes of the block DCELL

Transistor Name	w (µm)	l (µm)	Capacitor Name	Value (fF)
M1, M2	1	5	C1, C2	5
M3, M4	0.6	0.6		

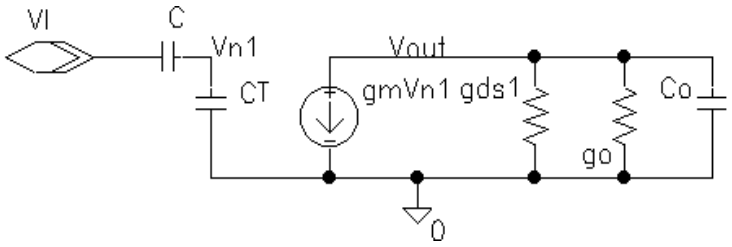

Figure 3.11 : Small Signal equivalent circuit of DCELL

Small signal equivalent circuit of the DCELL can be seen in Figure 3.11. A DC voltage source is connected to output node of the DCELL. In Figure 3.11, gm represents transconductance and gds represents output conductance of the transistor M1. C_O and g_O represent load capacitance and load conductance respectively. Chosen small signal equivalent circuit for MOS transistor can be seen in Figure 3.12. Parasitic C_{GD} capacitance is sufficiently small with respect to the others capacitance and it is neglected.

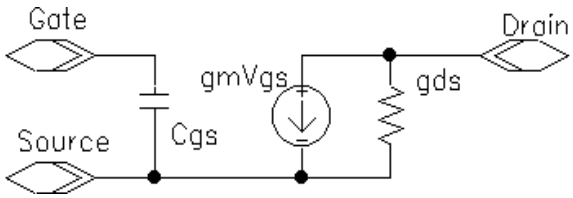

Figure 3.12 : Chosen Small Signal equivalent circuit of MOS transistor

Thus, small signal transfer function can be derived as follows:

$$V_{N1} = \frac{C}{C + C_T} V_I$$

$$I_O = (g_O + sC_O)V_O = -gmV_{N1} - gdsV_O$$

$$V_O = -\frac{1}{gds}(I_O + gmV_{N1})$$

The transfer function is

$$\frac{I_O}{V_I} = -\frac{C}{C + C_T}\frac{gm(sC_O + g_O)}{sC_O + g_O + gds} \qquad 3.22$$

Small signal simulation result of DCELL for C_O=50fF, g_O=50Ω, X=1.5V and T=2.5V can be seen in Figure 3.13. Cut-off frequency of the circuit is 1.164GHz.

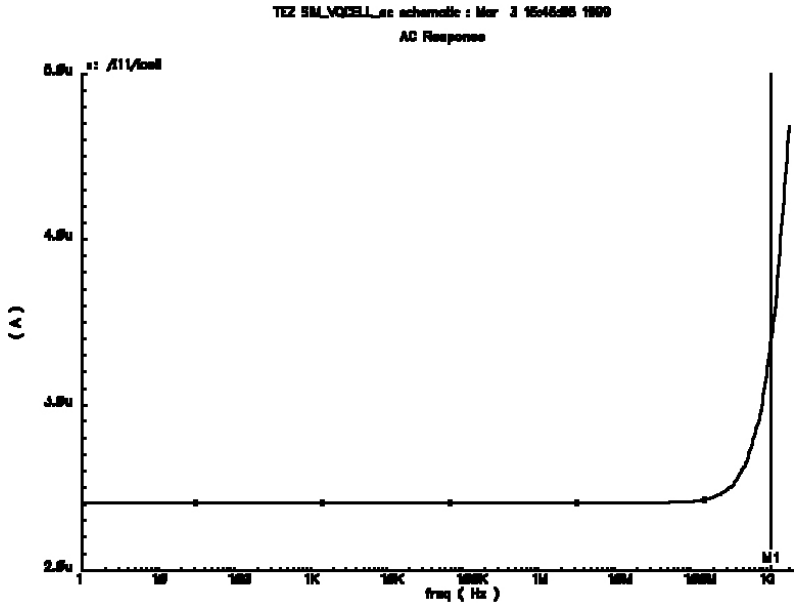

Figure 3.13 : Small Signal Simulation of DCELL

To measure the distance between input and template-vectors that have m vector elements, we must simply connect m DCELLs' output nodes to add the output currents of each cell. This structure constitutes a row whole output current can be expressed as

$$I_{ROW} = \sum_{i=1}^{m} I_{DCELL(iROW)} = \sum_{i=1}^{m} (X_i - T_{iROW})^2 \qquad 3.23$$

Vector Quantizer system tries to select the closest template-vector to the input vector. During the selection process, the system uses DCELL row's output current as a measure of distance. As mentioned previously, integrated circuit fabrication process is a sum of different random process. For that reason, all of device parameters vary around a mean value with a standard deviation determined by the process. Thus, we have to express row current error caused by the process noise. I^{th} row current can be expressed as

$$I_i = \sum_{j=1}^{m} I_{ij} \qquad 3.24$$

In (3.24), I_i represents i^{th} row current, I_{ij} represents output current of the DCELL placed on i^{th} row and j^{th} column. Let me now show relative error of DCELL row current.

$$I_{ij} = \frac{\beta}{2}\left[V_{bias} - \frac{C}{C_T}\left|X_j - T_{ij}\right| - V_{DD} - V_{TP}\right]^2 \quad 3.25$$

In (3.25), β, V_{TP}, C and C_T are random variables. Let me define ΔV and V as follows:

$$\Delta V = \frac{C}{C_T}\left|X_j - T_{ij}\right| \quad 3.26$$

$$V = V_{DD} + V_{TP} - V_{bias} \quad 3.27$$

The standard deviation of the output current of one DCELL block can be expressed as:

$$\sigma^2[I_{ij}] = (V + \Delta V)^2\left\{\frac{\sigma^2[\beta](V + \Delta V)^2}{4} + \beta^2\left[\sigma^2[V_{TP}] + 2\left(\frac{C}{C_T}(X_j - T_{ij})\right)^2\frac{\sigma^2[C]}{C^2}\right]\right\} \quad 3.28$$

Let us assume that all DCELLs have the same template and input voltages. Thus, row current can be expressed as

$$I_i = mI_{ij} = \frac{m\beta}{2}\left(V_{DD} + V_{TP} - V_{bias} + \frac{C}{C_T}\left|X_j - T_{ij}\right|\right)^2 = \frac{m\beta}{2}(V + \Delta V)^2 \quad 3.29$$

$$\sigma^2[I_i] = m\sigma^2[I_{ij}] \quad 3.30$$

Thus relative error of the row output current is

$$\frac{\sigma^2[I_i]}{{I_i}^2} = \frac{1}{m}\left\{\frac{\sigma^2[\beta]}{\beta^2} + \left[\frac{2V_{TP}}{V_{DD} + V_{TP} - V_{bias} + \frac{C}{C_T}\left|X_j - T_{ij}\right|}\frac{\sigma[V_{TP}]}{V_{TP}}\right]^2 + 2\left[2\frac{\frac{C}{C_T}\left|X_j - T_{ij}\right|}{V_{DD} + V_{TP} - V_{bias} + \frac{C}{C_T}\left|X_j - T_{ij}\right|}\frac{\sigma[C]}{C}\right]^2\right\} \quad 3.31$$

For detailed analysis of (3.31) please refer to Appendix B. If we reexamine (3.31), we can state the followings

a) Error is inversely proportional to the template-vector size m.

b) Second term goes to infinity when $V_{bias} \rightarrow V_{DD}+V_{TP}$ and $X_j \rightarrow T_{ij}$. It is normal. For small gate-source voltage, the error caused by the threshold voltage becomes dominant.

c) Third term goes to $\frac{8\sigma^2[C]}{C^2}$ when $V_{bias} \rightarrow V_{DD}+V_{TP}$

d) Third term goes to zero when $X_j \rightarrow T_{ij}$ and $V_{bias} \neq V_{DD} + V_{TP}$

Statistical equations used in this analysis are given in Appendix A.

Error plot for $m = 16$, $\frac{\sigma[\beta]}{\beta} = \frac{\sigma[V_{TP}]}{V_{TP}} = \%1$ and $\frac{\sigma[C]}{C} = \%2$ with respect to V_{bias} and ΔV can be seen in Figure 3.14.

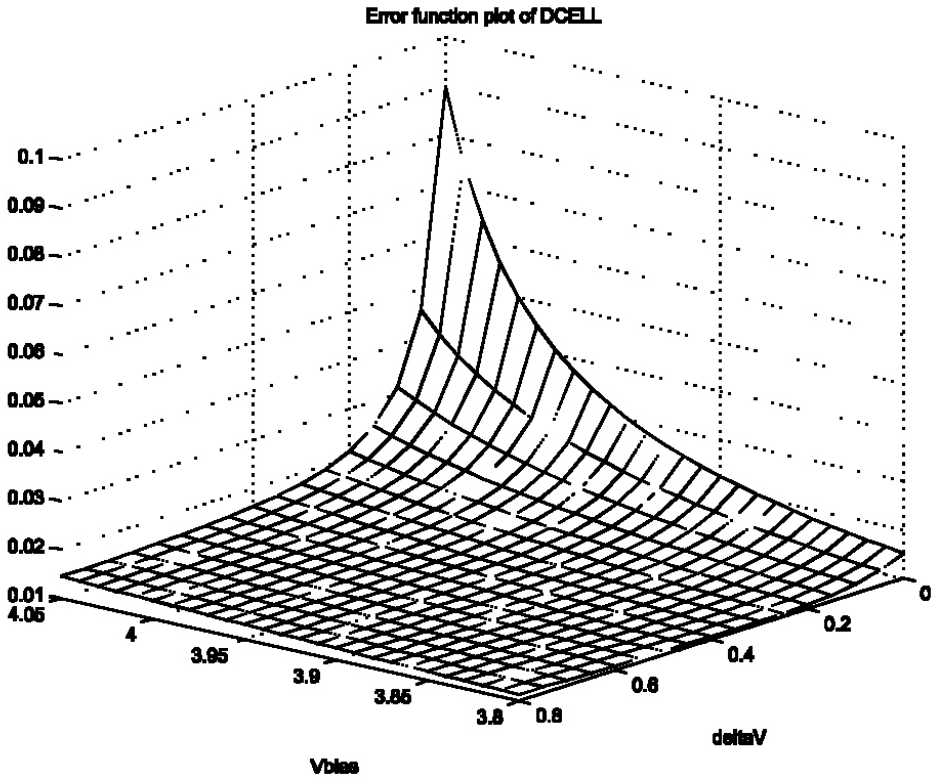

Figure 3.14 : Error Plot of DCELL

Monte Carlo simulation results for different V_{bias} and ΔV can be seen in Figures 3.15, 3.16 and 3.17.

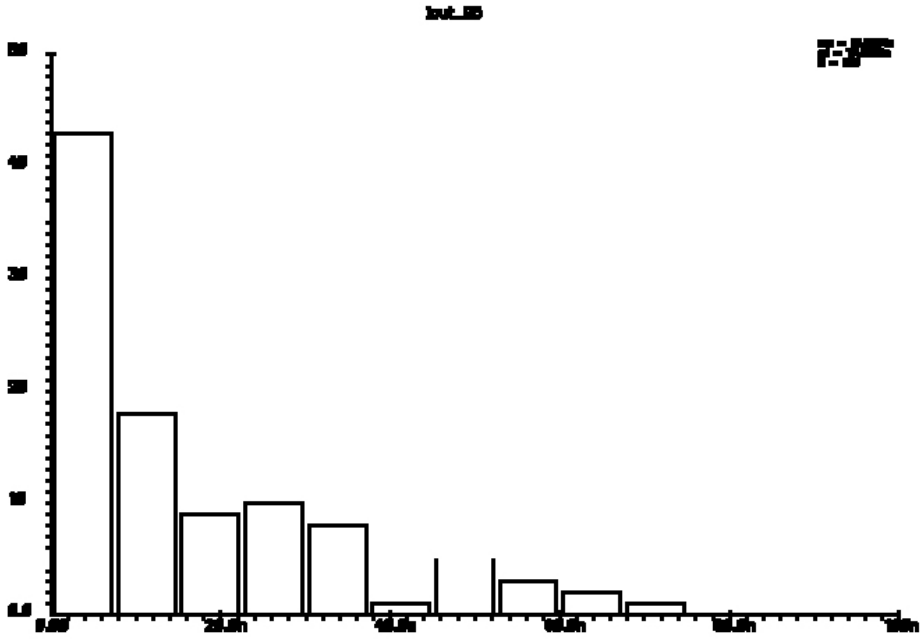

Figure 3.15 : Monte Carlo Simulation result of DCELL for V_{bias}=3.9V ΔV=0V

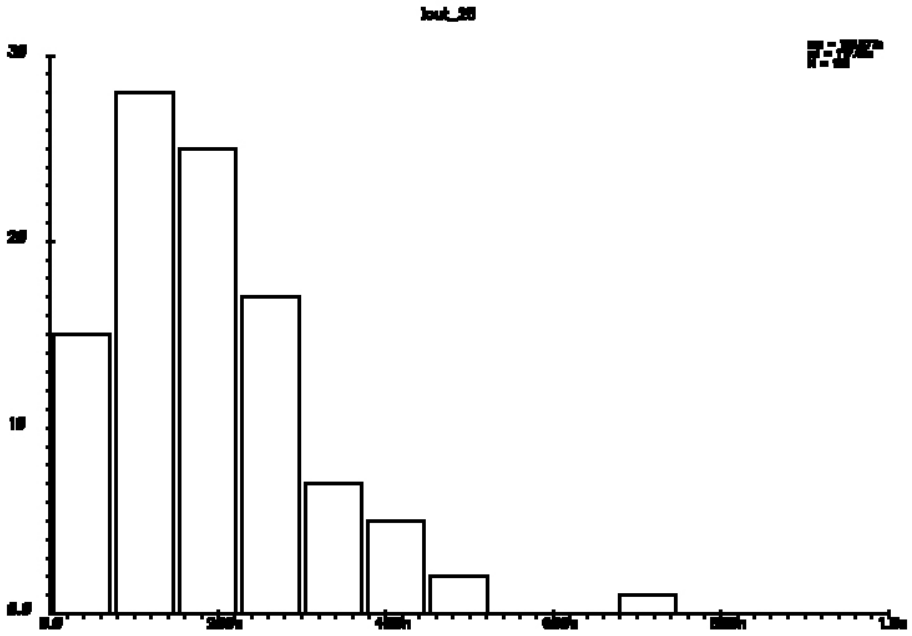

Figure 3.16 : Monte Carlo Simulation result of DCELL for V_{bias}=3.9V ΔV=1V

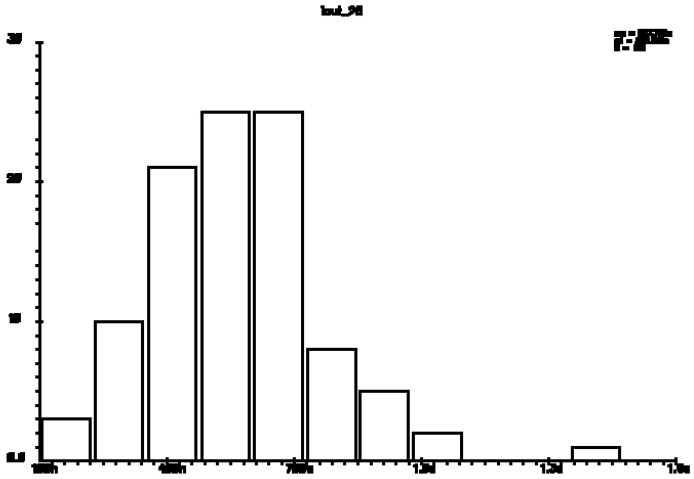

Figure 3.17 : Monte Carlo Simulation result of DCELL for V_{bias}=3.7V ΔV=1V

Monte Carlo simulation is performed on a single DCELL circuit. For a DCELL row containing m DCELLs, simulation result 'sd' must be divided by m. As I have expressed analytically, Monte Carlo simulation results show that relative current error decrease with increase of ΔV and (or) decrease of V_{bias}. To design a DCELL with greater resolution, we must improve matching properties of devices, thus we have to increase gate and capacitors areas. Detailed information on precise prediction of $\frac{\sigma[\beta]}{\beta}, \frac{\sigma[V_{TP}]}{V_{TP}}$ and $\frac{\sigma[C]}{C}$ can be found in [24-30] [21].

Beside process noise, there are two other error sources. First one is the change of the charge quantity stored on nodes N1 and N2 due to leakage currents. We can model it as a variation of the bias voltage V_{bias} during the time. Second one is the gain error of IN_AMP (Figure 3.5) due to finite value of amplifier gain (K) and resistors (R1 and R2) mismatch. Error caused by these sources must be smaller than ½LSB of DCELL row resolution. DCELL row current can be expressed as follows

$$I_i = \sum_{j=1}^{m} I_{ij}$$

$$I_{ij} = \frac{\beta}{2}\left[V_{DD} + V_{TP} - V_{bias} + \frac{C}{C_T}\left[K\left(X_j - T_{ij}\right)\right]\right]^2 \qquad 3.32$$

In (3.32), K and V_{bias} are random variables. Gain accuracy of unity gain amplifier in the block IN_AMP is not important. We can model its gain error as a coefficient in

front of term $\frac{C}{C+C_T}$ in (3.18). This coefficient is smaller than 1, thus it will not increase voltage range on nodes N1 and N2. Let me now examine relative DCELL row current error with respect to the random variables K and V_{bias}. The standard deviation of the DCELL output current can be expressed as

$$\sigma^2[I_{ij}] = \frac{\beta^2}{4}\left\{V_{DD}+V_{TP}-V_{bias}+\frac{C}{C_T}\left[K\left(X_j-T_{ij}\right)\right]\right\}^2\left\{\sigma^2[V_{bias}]+\left[\frac{C}{C_T}\left(X_j-T_{ij}\right)\right]^2\sigma^2[K]\right\} \quad 3.33$$

Assuming that all DCELLs have the same template and input voltages, we can write followings:

$$I_i = mI_{ij} \quad 3.34$$

$$\sigma^2[I_i] = m\sigma^2[I_{ij}] \quad 3.35$$

Thus relative DCELL output current error is

$$\frac{\sigma^2[I_i]}{I_i^2} = \frac{1}{m}\left\{\left[\frac{V_{DD}+V_{TP}}{\frac{C}{C_T}\left(X_j-T_{ij}\right)}\right]^2\frac{\sigma^2[V_{bias}]}{V_{bias}^2}+\frac{\sigma^2[K]}{K^2}\right\} \quad 3.36$$

Detailed analysis of (3.36) can be found in Appendix C. We replace random variables V_{bias} and K in (3.36) by their mean values. That are

$$V_{bias} = V_{DD}+V_{TP} \qquad \text{and} \qquad K = 1 \quad 3.37$$

We predict that the DCELL has six bits of resolution. Thus,

$$\frac{\sigma[I_i]}{I_i} = \frac{1}{2^6} \quad 3.38$$

Finally, error caused by (3.36) must not exceed ½ of (3.38).

$$\left[\frac{V_{DD}+V_{TP}}{\frac{C}{C_T}\left(X_j - T_{ij}\right)}\right]^2 \frac{\sigma^2[V_{bias}]}{{V_{bias}}^2} + \frac{\sigma^2[K]}{K^2} < m\frac{\sigma^2[I_i]}{{I_i}^2} = m\frac{1}{2^{14}} \qquad 3.39$$

(3.39) will draw our limits about refresh time, matching properties between R1 and R2, and minimum open loop gain K of the amplifier in the block IN_AMP at operating frequency .

For m=16, $X_j - T_{ij} = 100\,mV$ $\frac{C}{C_T} = 0.269$ and $V_{DD} + V_{TP} = 4.1\,V$, we can write (3.39) as follows

$$\left[\frac{4{,}1}{0{,}269.100\,m}\right]^2 \frac{\sigma^2[V_{bias}]}{{V_{bias}}^2} + \frac{\sigma^2[K]}{K^2} < \frac{1}{2^{10}} \qquad 3.40$$

At this point, we must share error among the variables K and V_{bias}. We assume that $\frac{1}{10}$ of error is gain error. Thus,

$$\frac{\sigma[K]}{K} < \%1 \quad \text{and} \quad \frac{\sigma[V_{bias}]}{V_{bias}} < \%0{,}019 \qquad 3.41$$

Under the condition (3.41), we must calculate refresh time.

We need to refresh periodically template voltage stored on node N1 (or N2) because of the leakage currents. Node N1 can be seen detailed in Figure 3.18. Discharge of the capacitance on N1 can be expressed as:

$$\begin{aligned} I_{N1} &= C_{N1}\frac{dV_{N1}}{dt} \\ dt &= \frac{C_{N1}dV_{N1}}{I_{N1}} \end{aligned} \qquad 3.42$$

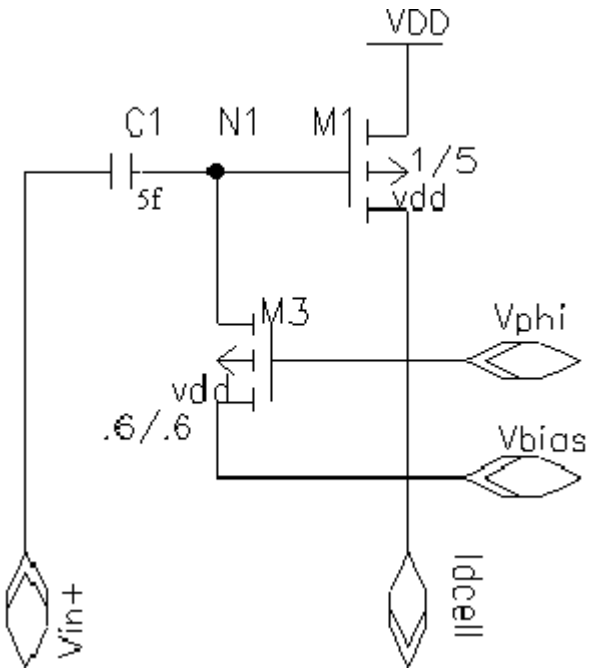

Figure 3.18 : Schematic view of Node N1 (or N2)

To calculate refresh time (dt), we have to find leakage current I_{N1} and total node capacitance C_{N1}.

$$I_{N1} = I_{C1} + I_{G(M1)} + I_{M3} \qquad 3.43$$

Practically input capacitor and M1 transistor's gate current are zero. Current of transistor M3 can be expressed as follows:

$$I_{M3} = I_{leakage(M3)} + I_{sub\_treshold(M3)} \qquad 3.44$$

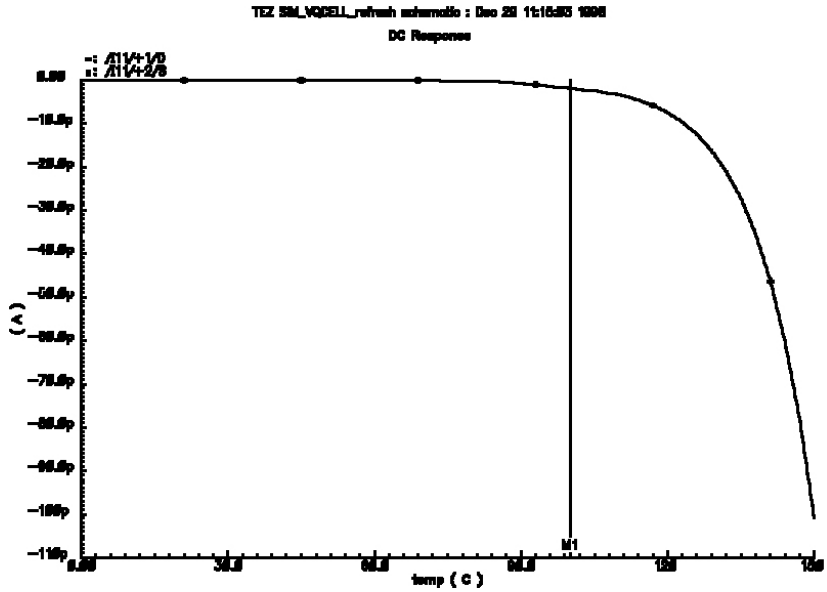

Figure 3.19 : Variation of leakage current with temperature

In (3.44), first term represents leakage current due to reverse biased bulk-source pn junction; second term represents sub-threshold current of transistor M3. The leakage current is the dominant current in I_{M3}. I_{N1} varies exponentially with temperature. Variation of I_{N1} with temperature can be seen in Figure 3.19. In our calculation, we will suppose that ambient temperature is 100°C. Detailed analysis on leakage and sub-threshold currents can be found at references [19, 20, 22, 23].

$I_{N1} = 1.85\text{pA}$ at 100°C.

Total capacitance on node N1 can be divided into two different terms.

$$C_{N1} = C_{const} + C(V_{N1}) \approx C_{const} \qquad 3.45$$

First term is voltage independent (poly capacitance, parasitic wire capacitances, etc…) and second term is voltage dependent (junction capacitances).

$$C_{const} = C_{gate} + C_{poly1-poly2} + C_{poly1-bulk} + C_{metal1-bulk} + C_{poly1-metal1} \approx 20\,\text{fF} \qquad 3.46$$

Voltage independent capacitances can be modeled as

$$C_{ij} = A_{ij}C_{ua\_ij} + P_{ij}C_{up\_ij} \qquad 3.47$$

In (3.47), C_{ij} represents the total capacitance between layers i and j, A_{ij} represents the area of capacitor, C_{ua_ij} represents the unit area capacitance, P_{ij} represents the perimeter of capacitor, C_{up_ij} represent the unit perimeter capacitance.
Junction capacitance can be modeled as follow

$$\begin{aligned} C(V_{N1}) &= AS.C_{bottom} + PS.C_{sidewall} \\ &= AS.\frac{C_{j0}}{\sqrt{1+\frac{V_{N1}}{\phi_0}}} + \frac{PS.x_j C_{j0sw}}{\sqrt{1+\frac{V_{N1}}{\phi_0}}} \end{aligned} \qquad 3.48$$

In (3.48), AS represents source diffusion area and PS represents source diffusion perimeter, and V_{N1} represents the voltage of node N1. Other parameters are process parameters. The size of the constant capacitance is sufficiently large that we can neglect junction capacitances.

With respect to (3.41), dV_{N1} in (3.42) can be 0.19 mV maximum. Thus, refresh time can be calculated as

$$dt \le \frac{C_{N1}}{I_{N1}} dV_{N1} \approx 2\,\text{ms} \qquad 3.49$$

Obviously, to increase refresh time, we have to increase total capacitance on nodes N1 and N2.

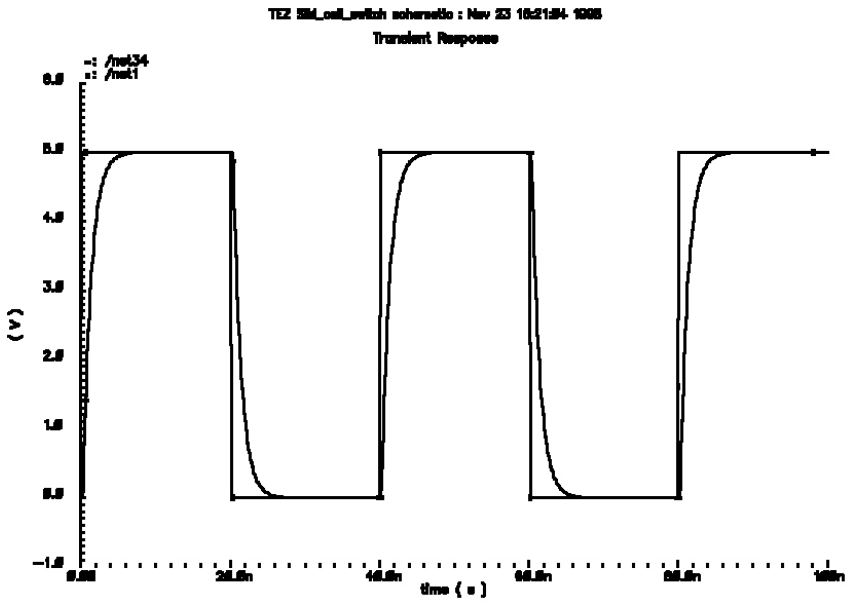

Figure 3.20: Delay of last M3's gate voltage in a row containing 16 DCELL

As mentioned previously, we drive gates of the transistors M3 and M4 with poly wire. Layer resistance will affect turn on (or off) time. Delay of gate voltage of transistor M3 (or M4) which is on the last cell in a DCELL row containing 16 cells can be seen in Figure 3.20. In worst case, the delay between the first and last cell of a row containing 16 DCELL does not exceed 6ns. For a normal operation, input signals that are template voltages during the refresh period have to be changed after that all of M3 and M4 transistors are in cut-off region.

To decrease simulation time in system level simulation, a primitive behavioral model of the DCELL is developed. Our aim is not to model the DCELL perfectly but to reduce simulation time with the simplicity of the behavioral model that contains all necessary behavior of a DCELL. AHDL code models the transconductance of the output transistors M1 and M2, the threshold voltage of the transistors, power supply voltage, the ratio $C/(C+C_T)$, leakage current, template writing protocol and the parabolic output current behavior. The behavioral AHDL code of the block DCELL can be found in Appendix G.

Simulation result of AHDL model to input stimulus in Figure 3.9 can be seen in Figure 3.21.

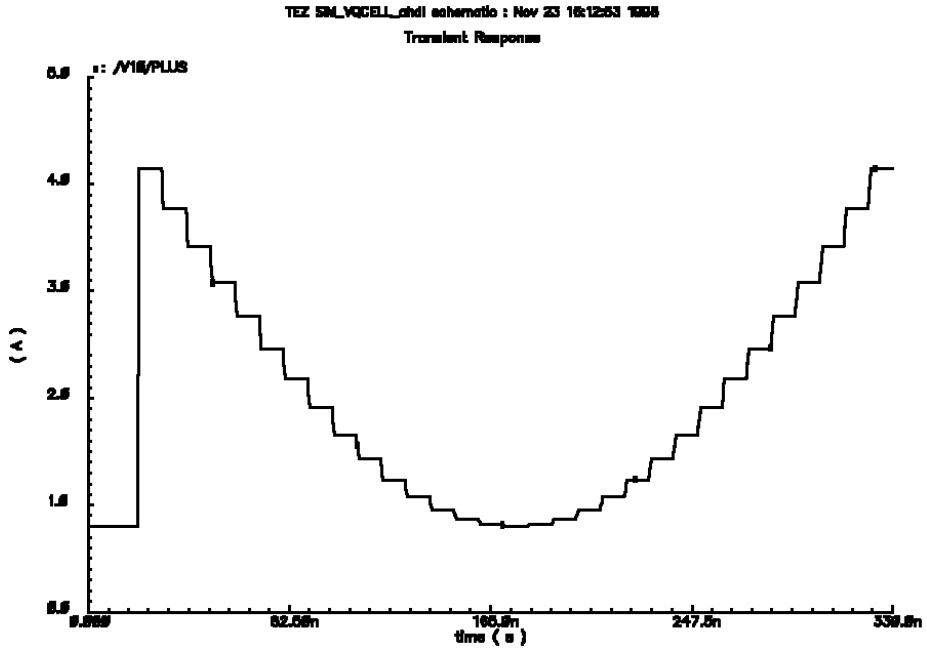

Figure 3.21 : Simulation result of AHDL model

With respect to all above-mentioned knowledge, we can draw following conclusions to design a DCELL block.

a) Criteria for determining of M1 & M2 transistors' β

1) Power dissipation budget for a DCELL

2) Output signal resolution for a given input signal range.

b) Criteria for determining Channel length and input capacitors size

a) Reverse biased source-bulk junction must never be forward biased. This will bound voltage swings on nodes N1 and N2.

b) For a given resolution, the DCELL must satisfy some matching criteria.

3) The DCELL must satisfy given refresh time.

4) Silicon area budget

c) M3 and M4 are chosen with minimum channel area and minimum source diffusion area.