MOSIS SCMOS
Technology Codes and Layer Maps
SCN3ME and SCN3ME_SUBM

Source: http://www.mosis.com/Technical/Layermaps/lm-scmos_scn3me.html

This is the layer map for the technology codes SCN3ME and SCN3ME_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN3ME and SCN3ME_SUBM. For designs that are laid out using other design rules (or technology-codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

SCN3ME: Scalable CMOS N-well, 3 metal, non-silicided, high resistance layer available. Adds a second polysilicon layer (poly2) as the upper electrode of a poly capacitor.

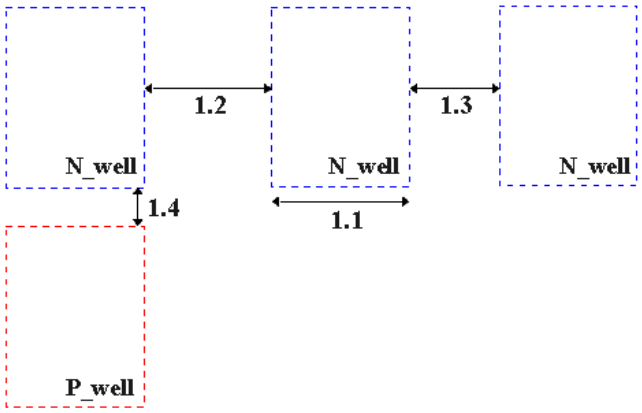
SCN3ME_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Fabricated on AMI 0.50 micron process runs.

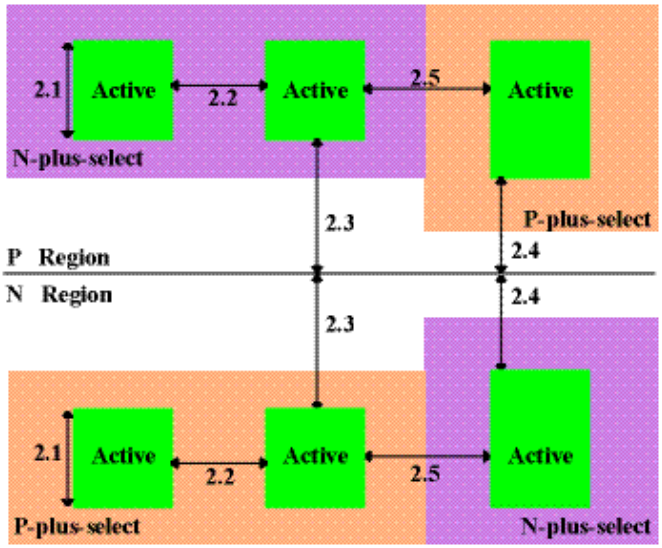
Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
POLY	46	CPG		3	
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
POLY2	56	CP2	CEL	11, 12, 13	Optional
HI_RES_IMPLANT	34	CHR		27	Optional
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
POLY2_CONTACT	55	CCE		13	Can be replaced by CONTACT.
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

MOSIS SCMOS_SUBM Layout Design Rules (3-Metal)

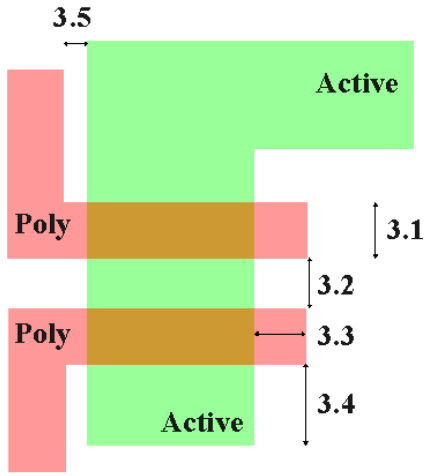
N-Well		
Rule	Description	Lambda
1.1	Minimum width	12
1.2	Minimum spacing between wells at different potential	18
1.3	Minimum spacing between wells at same potential	0 or 6
1.4	Minimum spacing between wells of different type (if both are drawn)	0



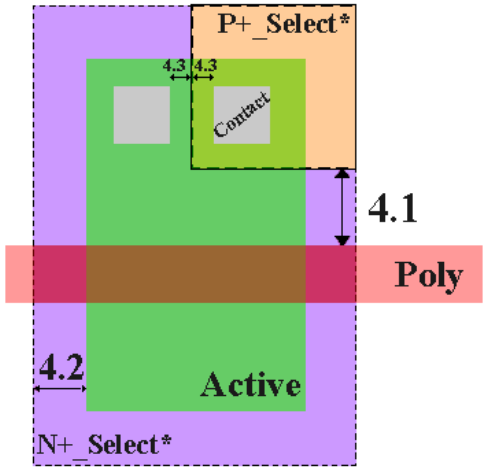
Active		
Rule	Description	Lambda
2.1	Minimum width	3
2.2	Minimum spacing	3
2.3	Source/drain active to well edge	6
2.4	Substrate/well contact active to well edge	3
2.5	Minimum spacing between active of different implant.	4



Poly		
Rule	Description	Lambda
3.1	Minimum width	2
3.2	Minimum spacing over field	3
3.2.a	Minimum spacing over active	3
3.3	Minimum gate extension of active	2
3.4	Minimum active extension of poly	3
3.5	Minimum field poly to active	1



n-select / p-select		
Rule	Description	Lambda
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3
4.2	Minimum select overlap of active	2
4.3	Minimum select overlap of contact	1
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2

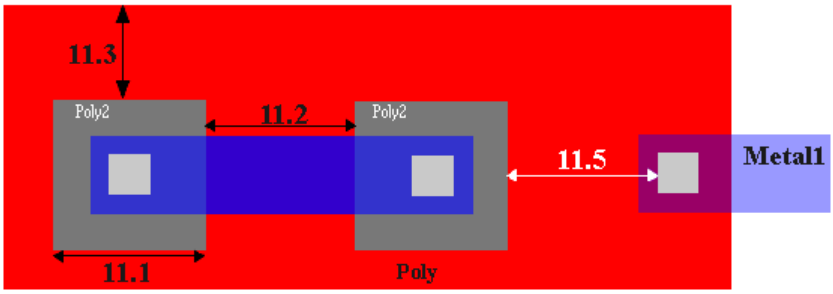


*The same rules apply with N+_Select and P+_Select reversed.

Poly2 for Capacitor

The poly2 layer is a second polysilicon layer (physically above the standard, or first, poly layer). The oxide between the two poly layers is the capacitor dielectric. The capacitor area is the area of coincident poly and electrode.

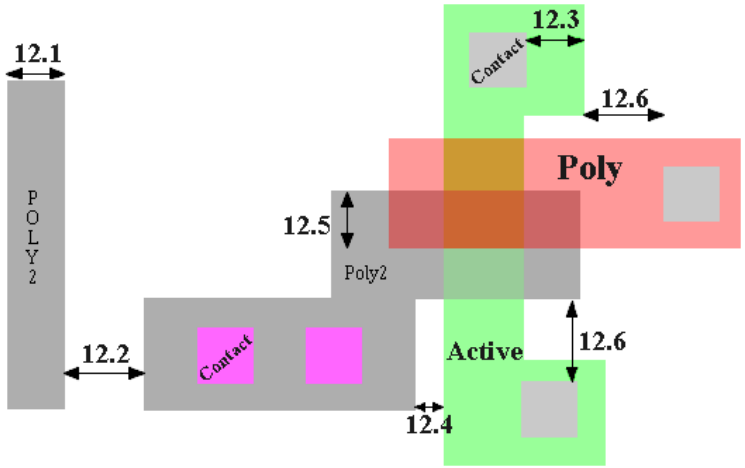
Rule	Description	Lambda
11.1	Minimum width	7
11.2	Minimum spacing	3
11.3	Minimum poly overlap	5
11.4	Minimum spacing to active or well edge (not illustrated)	2
11.5	Minimum spacing to poly contact	6
11.6	Minimum spacing to *unrelated* metal	2



Poly2 for Transistor

Same poly2 layer as for caps

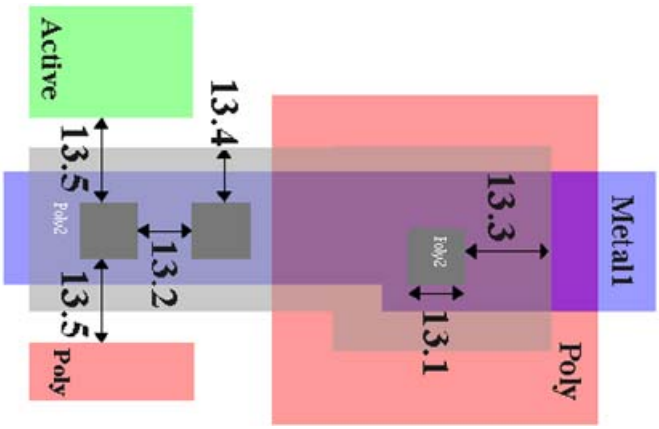
Rule	Description	Lambda
12.1	Minimum width	2
12.2	Minimum spacing	3
12.3	Minimum electrode gate overlap of active	2
12.4	Minimum spacing to active	1
12.5	Minimum spacing or overlap of poly	2
12.6	Minimum spacing to poly or active contact	3



Poly2 Contact

The poly2 is contacted through the standard contact layer, similar to the first poly. The overlap numbers are larger, however. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

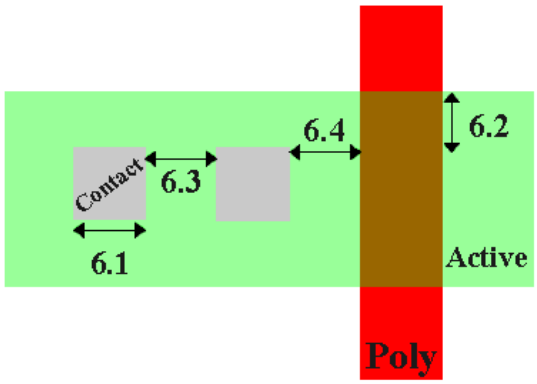
Rule	Description	Lambda
13.1	Exact contact size	2 x 2
13.2	Minimum contact spacing	3
13.3	Minimum electrode overlap (on capacitor)	3
13.4	Minimum electrode overlap (not on capacitor)	2
13.5	Minimum spacing to poly or active	3



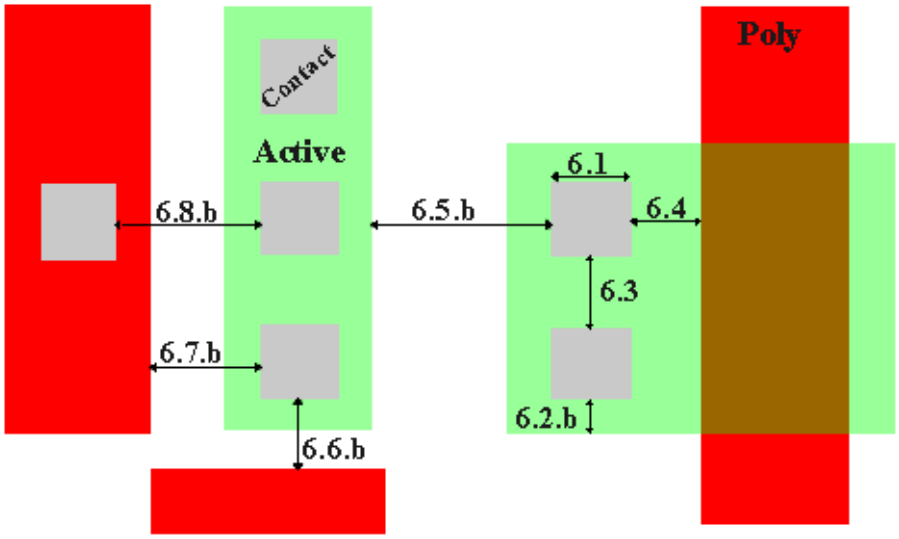
Simple Contact to Active

If your design cannot handle the 1.5 lambda contact overlap in 6.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 6.1, 6.3, and 6.4, still apply and are unchanged. Contacts must be drawn orthogonal to the grid of the layout.

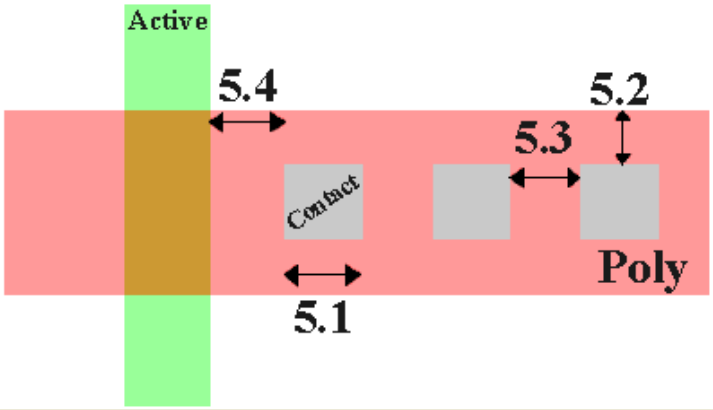
Rule	Description	Lambda
6.1	Exact contact size	2x2
6.2	Minimum active overlap	1.5
6.3	Minimum contact spacing	3
6.4	Minimum spacing to gate of transistor	2



Alternative Contact to Active		
Rule	Description	Lambda
6.2.b	Minimum active overlap	1
6.5.b	Minimum spacing to diffusion active	5
6.6.b	Minimum spacing to field poly (one contact)	2
6.7.b	Minimum spacing to field poly (many contacts)	3
6.8.b	Minimum spacing to poly contact	4

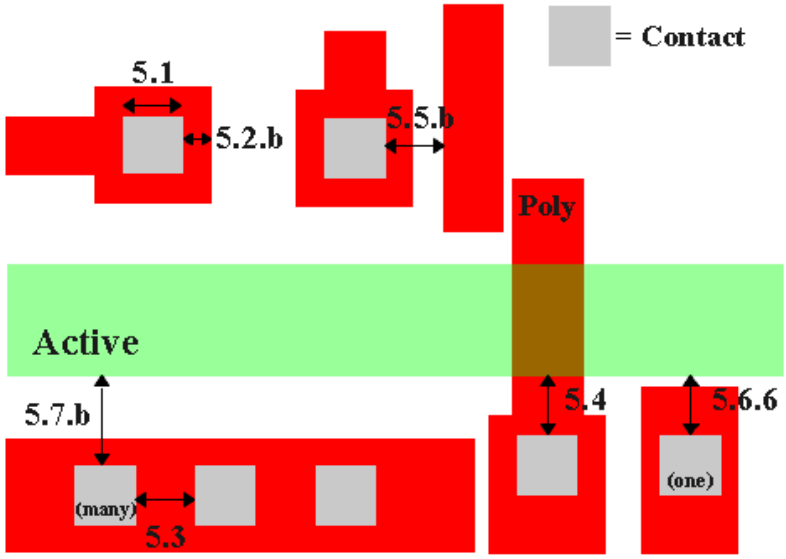


Simple Contact to Poly		
Rule	Description	Lambda
5.1	Exact contact size	2x2
5.2	Minimum poly overlap	1.5
5.3	Minimum contact spacing	3
5.4	Minimum spacing to gate of transistor	2

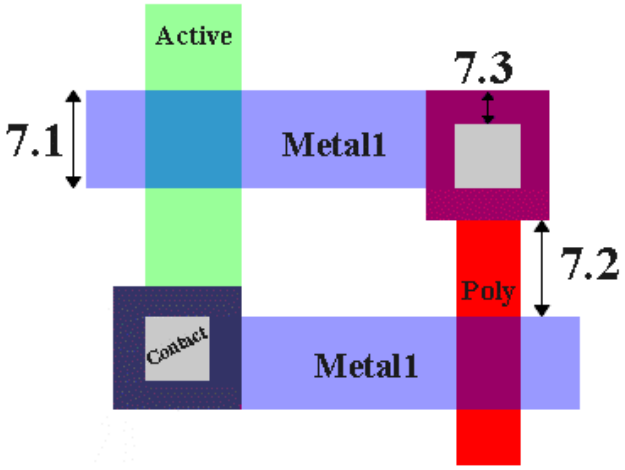


Alternative Contact to Poly

Rule	Description	Lambda
5.2.b	Minimum poly overlap	1
5.5.b	Minimum spacing to other poly	5
5.6.b	Minimum spacing to active (one contact)	2
5.7.b	Minimum spacing to active (many contacts)	3

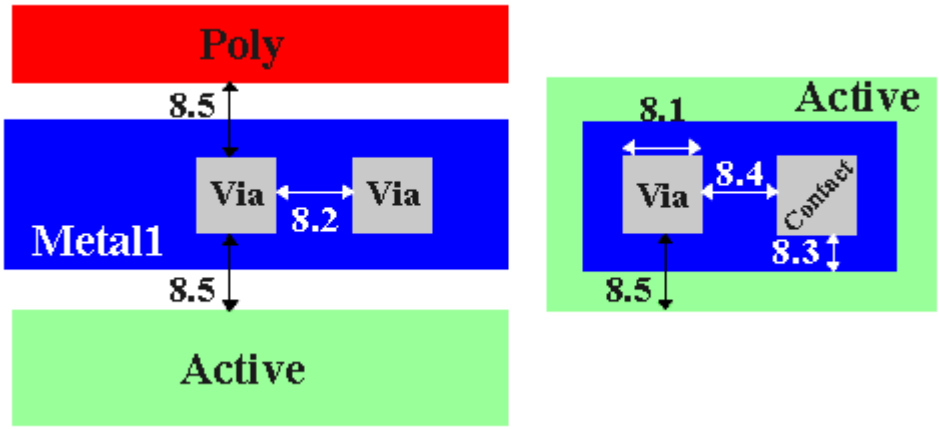


Metal1		
Rule	Description	Lambda
7.1	Minimum width	3
7.2	Minimum spacing	3
7.3	Minimum overlap of any contact	1
7.4	Minimum spacing when either metal line is wider than 10 lambda	6

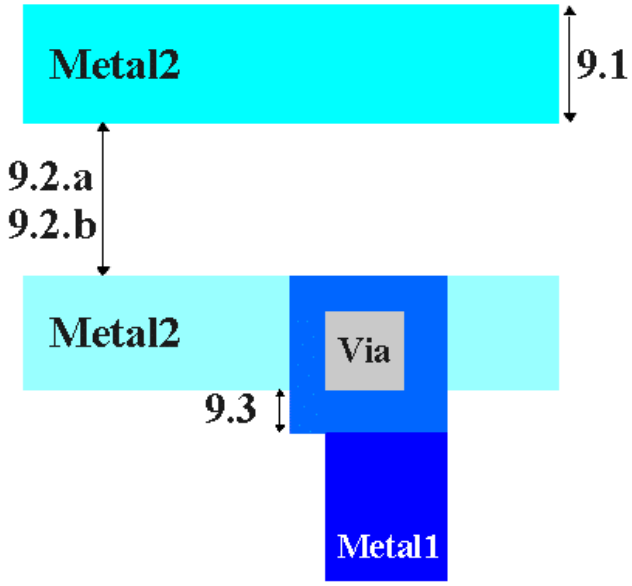


Via

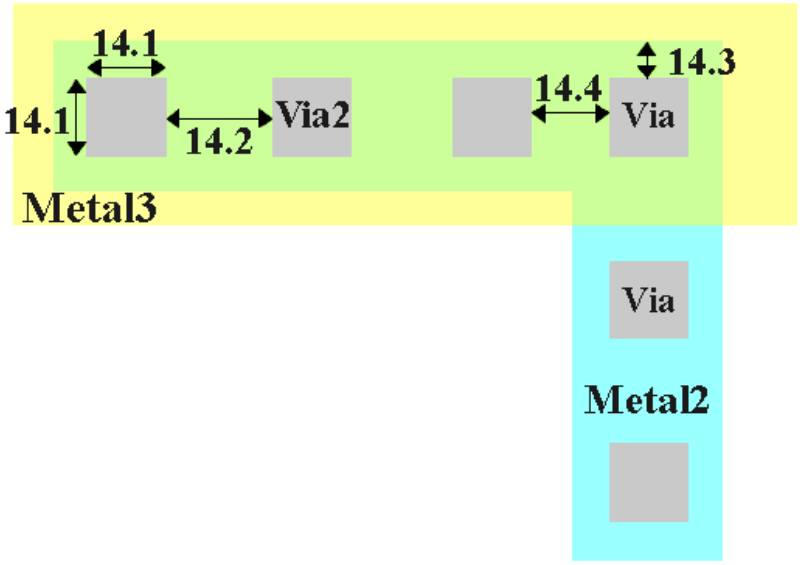
Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.		
Rule	Description	Lambda
8.1	Exact size	2 x 2
8.2	Minimum via1 spacing	3
8.3	Minimum overlap by metal1	1



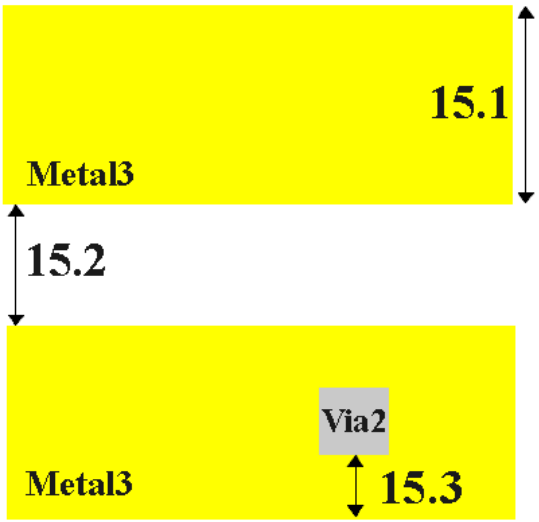
Metal2		
Rule	Description	Lambda
9.1	Minimum width	3
9.2	Minimum spacing	3
9.3	Minimum overlap of via1	1
9.4	Minimum spacing when either metal line is wider than 10 lambda	6



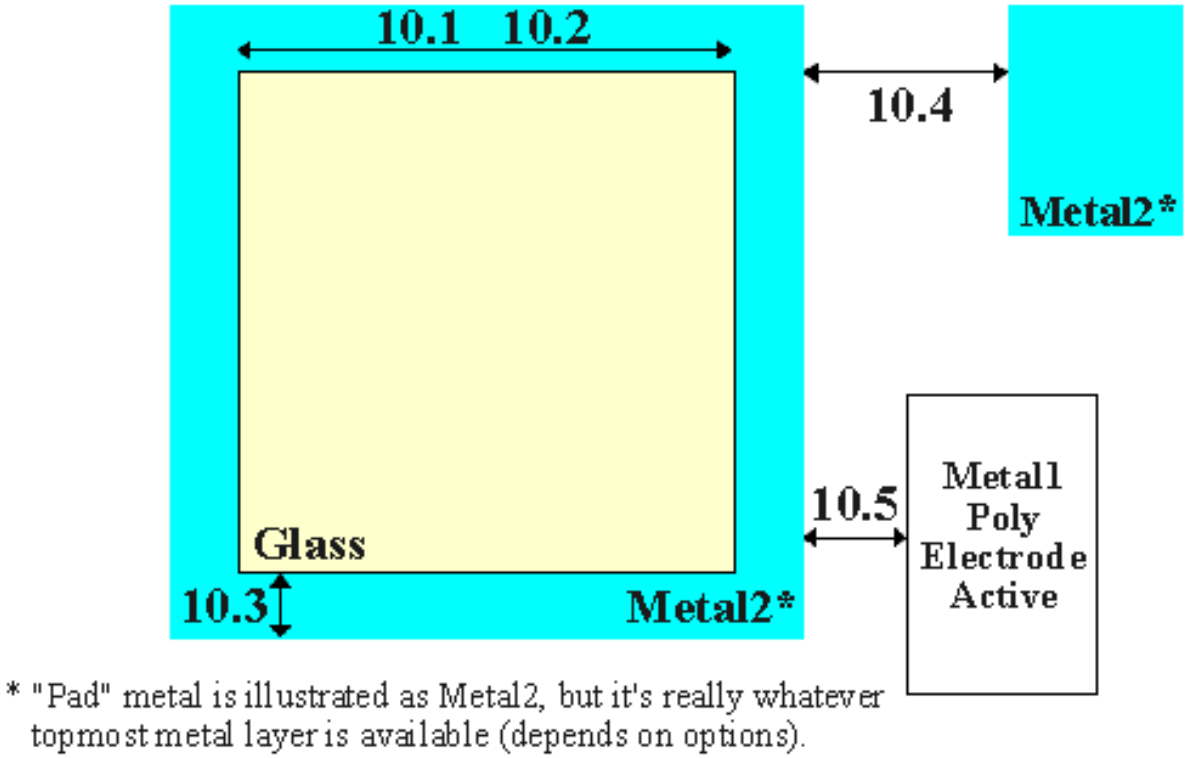
Via2 *Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.*		
Rule	Description	Lambda
14.1	Exact size	2x2
14.2	Minimum spacing	3
14.3	Minimum overlap by metal2	1



Metal3		
Rule	Description	Lambda
15.1	Minimum width	5
15.2	Minimum spacing to metal3	3
15.3	Minimum overlap of via2	2
15.4	Minimum spacing when either metal line is wider than 10 lambda	6



Overglass *Note that rules in this section are in units of microns. They are not "true" design rules, but they do make good practice rules. Unfortunately, there are no really good generic pad design rules since pads are process-specific.*		
Rule	Description	***Microns***
10.1	Minimum bonding passivation opening	60
10.2	Minimum probe passivation opening	20
10.3	Pad metal overlap of passivation	6
10.4	Minimum pad spacing to unrelated metal	30
10.5	Minimum pad spacing to active, poly or poly2	15



* "Pad" metal is illustrated as Metal2, but it's really whatever topmost metal layer is available (depends on options).